

IDT54/74FCT16501AT/CT/ET
IDT54/74FCT162501AT/CT/ET
IDT54/74FCT162H501AT/CT/ET

- **Common features:**

- CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB is the output enable for the B port. Data flow from the B port to the A port is similar but requires using $\overline{\text{OEBA}}$, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16501AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162501AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162501AT/CT/ET are plug-in replacements for the FCT16501AT/CT/ET and ABT16501 for on-board bus interface applications.

The FCT162H501AT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

The FCT16501AT/CT/ET and FCT162501AT/CT/ET 18-bit registered transceivers are built using advanced dual metal

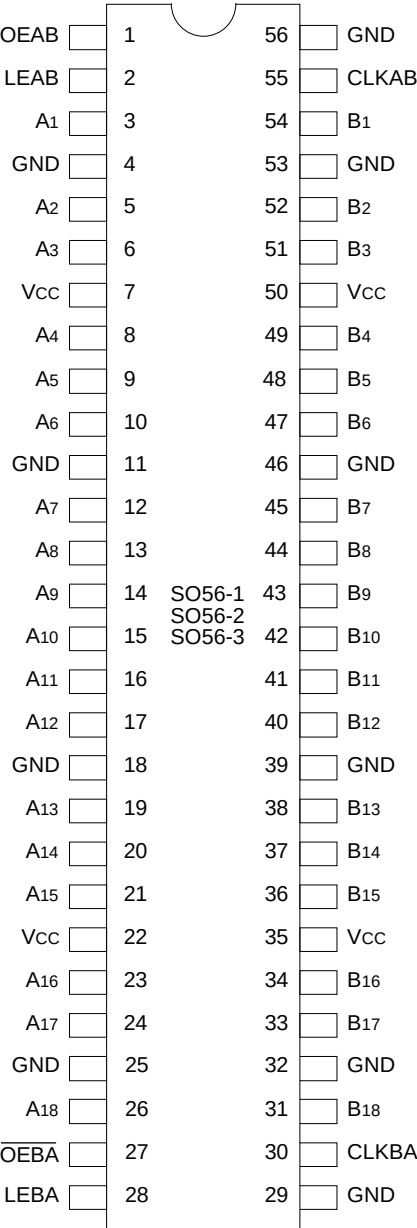
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TO 17 OTHER CHANNELS

2547 dnrw 01

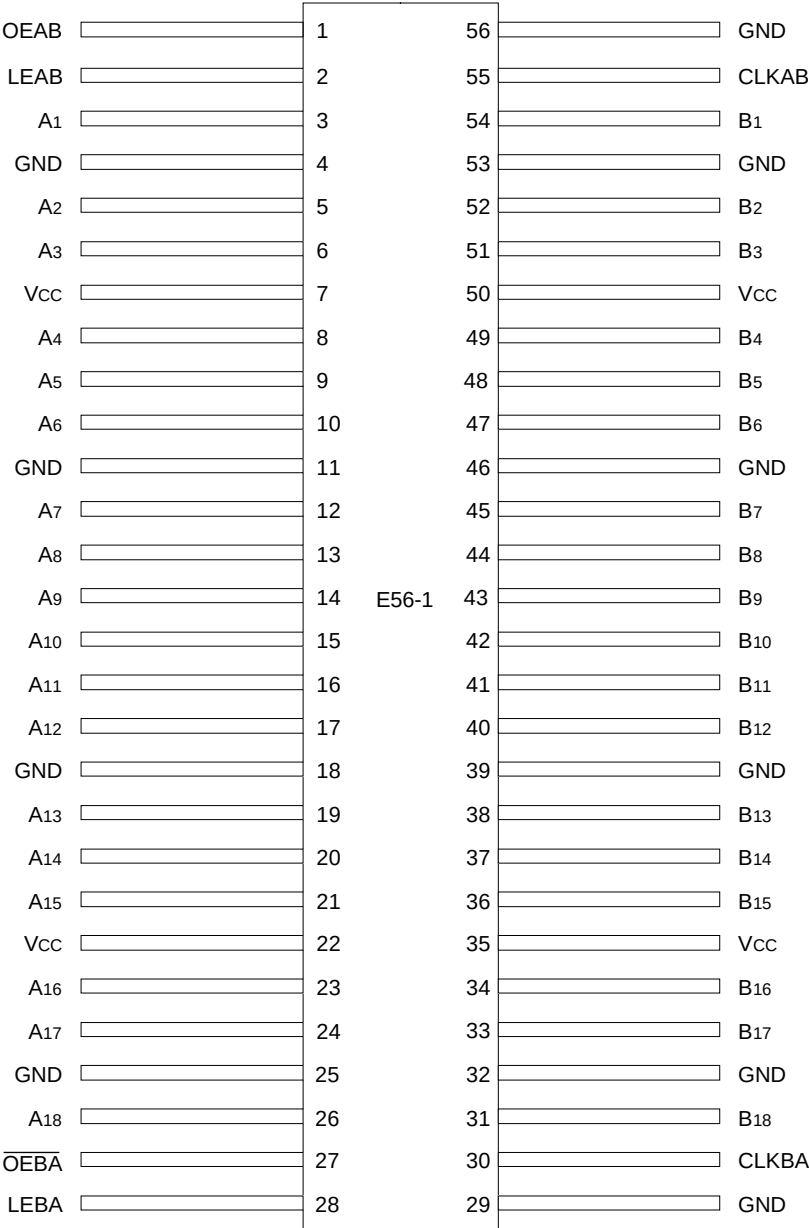
AUGUST 1996

PIN CONFIGURATIONS



SSOP/
TSSOP/TVSOP
TOP VIEW

2547 drw 02



CERPACK
TOP VIEW

2547 drw 03

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

2547 tbl 01

1. On FCT16xH501T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +120	mA

NOTES:

2547 lnk 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE^(1,4)

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B ⁽²⁾
H	L	H	X	B ⁽³⁾

NOTES:

2547 tbl 02

- A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance
↑ = LOW-to-HIGH Transition

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	3.5	8.0	pF

NOTE:

2547 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾		-80	-140	-225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}		—	5	500	μA

2547 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16501T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_O	Output Drive Current	$V_{CC} = \text{Max.}$, $V_O = 2.5\text{V}$ ⁽³⁾		-50	—	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.5	—	V
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}$ ⁽⁴⁾	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$		—	—	± 1	μA

2547 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162501T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

NOTES:

2547 Ink 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus-Hold Input			—	—	±100	
		Bus-Hold I/O			—	—	±100	
I _{IL}	Input LOW Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _I = GND	—	—	±1		
		Standard I/O ⁽⁵⁾		—	—	±1		
		Bus-Hold Input		—	—	±100		
		Bus-Hold I/O		—	—	±100		
I _{BHH} I _{BHL}	Bus Hold Sustain Current ⁽⁴⁾	Bus-Hold Input	V _{CC} = Min.	V _I = 2.0V V _I = 0.8V	−50 +50	— —	— —	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins) ^(5,6)		V _{CC} = Max.	V _O = 2.7V V _O = 0.5V	— —	— —	±1 ±1	μA
V _{IK}				Clamp Diode Voltage		V _{CC} = Min., I _{IN} = −18mA		
I _{OS}	Short Circuit Current		V _{CC} = Max., V _O = GND ⁽³⁾		−80	−140	−225	mA
V _H	Input Hysteresis		—		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current		V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA

NOTES:

2547 Ink 08

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Pins with Bus Hold are identified in the pin description.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
- Does not include Bus Hold I/O pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $OEAB = \overline{OEBA} = V_{CC}$ or GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.5	20.8 ⁽⁵⁾	

NOTES:

2547 tbl 09

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16501AT/162501AT				FCT16501CT/162501CT				FCT16501ET/162501ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
fMAX	CLKAB or CLKBA frequency ⁽⁴⁾	CL = 50pF RL = 500Ω	—	150	—	150	—	150	—	150	—	150	—	—	MHz
tPLH tPHL	Propagation Delay Ax to Bx or Bx to Ax		1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.6	1.5	4.2	—	—	ns
tPLH tPHL	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.4	1.5	4.2	—	—	ns
tPZH tPZL	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6.0	1.5	6.4	1.5	5.6	1.5	6.0	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	6.0	1.5	5.2	1.5	5.6	1.5	5.2	—	—	ns
tsu	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		3.0	—	3.0	—	3.0	—	3.0	—	2.4	—	—	—	ns
th	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	0	—	—	—	ns
tsu	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW	3.0	—	3.0	—	3.0	—	3.0	—	2.0	—	—	—	ns
		Clock HIGH	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
th	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	1.5	—	0.5	—	—	—	ns
tw	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
tw	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

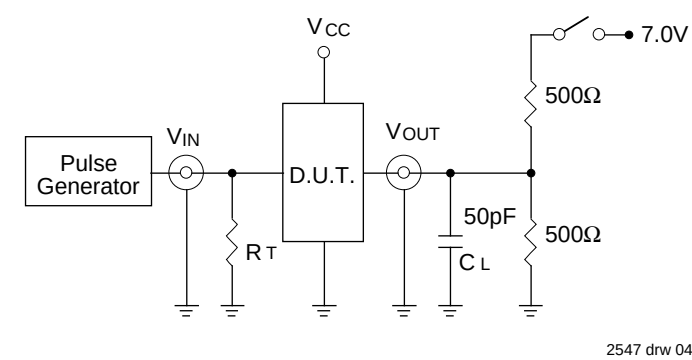
NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- This parameter is guaranteed but not tested.

2547 tbl 10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

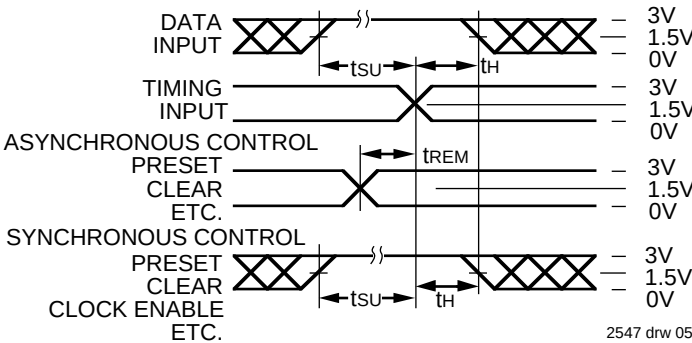


SWITCH POSITION

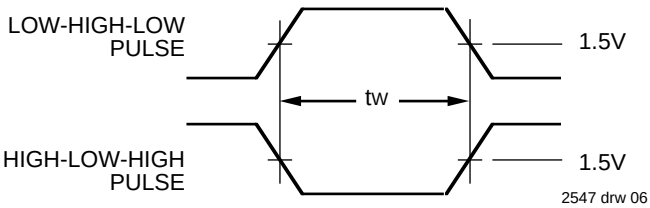
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS: 2547 Ink 11
CL= Load capacitance: includes jig and probe capacitance.
RT= Termination resistance: should be equal to ZOUT of the Pulse Generator.

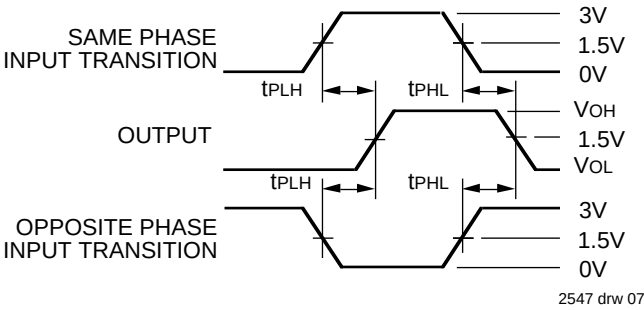
SET-UP, HOLD AND RELEASE TIMES



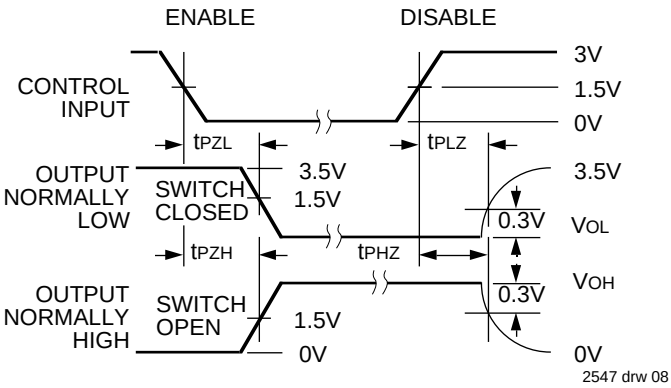
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



- NOTES:**
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
 - Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

ORDERING INFORMATION

<u>IDT</u> <u>X</u>	<u>FCT</u>	<u>X</u>	<u>X</u>	<u>XXXX</u>	<u>X</u>	<u>X</u>		
Temperature Range	Drive	Bus Hold	Device Type	Package	Process			
						Blank		Commercial
						B		MIL-STD-883, Class B
						PV		Shrink Small Outline Package (SO56-1)
						PA		Thin Shrink Small Outline Package (SO56-2)
						PF		Thin Very Small Outline Package (SO56-3)
						E		CERPACK (E56-1)
						501AT		Non-Inverting 18-Bit Registered Transceiver
						501CT		
						501ET		
						Blank		Standard
						H		
						16		16-Bit High Drive
						162		16-Bit Balanced Drive
						54		–55°C to +125°C
						74		–40°C to +85°C

2547 drw 09