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LC03-6

Low Capacitance TVS for High-Speed Date interfaces

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Features

- Low capacitance for high speed interfaces
- Ultra low leakage: nA level
- Low operating voltage
- Low clamping voltage
- Protects two lines in common and differential mode
- JEDEC SO-8 package
- Complies with following standards:
  – IEC 61000-4-2 (ESD) immunity test
    Air discharge: ±30kV
    Contact discharge: ±30kV
  – IEC61000-4-5 (Lightning) 100A (8/20μs)
- RoHS Compliant

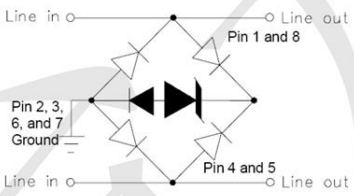
Mechanical Characteristics

- Package: SO-8
- Lead Finish: Matte Tin
- Case Material: “Green” Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below
- Shipping Qty :2500pcs/7Inch Tape & Reel

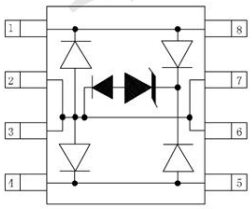
Applications

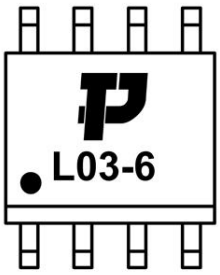
- T1/E1 Line Cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet
- Set Top Box
- ISDN Interfaces
- Low Voltage Interfaces

Dimensions and Pin Configuration



Circuit and Pin Schematic





SO-8 Outline

Absolute Maximum Ratings (Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power(8/20μs)	Ppk	2000	W
Peak Pulse Current(8/20μs)	I_{PP}	100	A
Lead Soldering Temperature	T_L	260(10 sec.)	°C
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Electrical Characteristics (TA=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			5	V	
Reverse Breakdown Voltage	V_{BR}	6 .8			V	I_T = 1mA
Reverse Leakage Current	I_R			25	μA	V_{RWM} = 5V,T=25°C
Clamping Voltage	V_C			10	V	I_{PP} = 1A (8 x 20μs pulse) Line to Ground
Clamping Voltage	V_C			15	V	I_{PP} = 55A (8 x 20μs pulse) Line to Ground
Clamping Voltage	V_C			20	V	I_{PP} = 100A (8 x 20μs pulse) Line to Ground
Junction Capacitance	C_J			25	pF	VR = 0V, f = 1MHz Between I/O pins and Ground
			9	14	pF	VR = 0V, f = 1MHz Between I/O pins

Typical Performance Characteristics (T_A=25°C unless otherwise Specified)

Fig1. 8/20μs Pulse Waveform

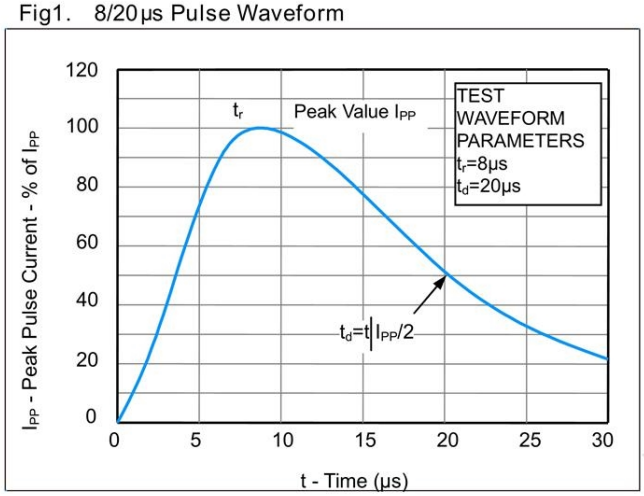


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

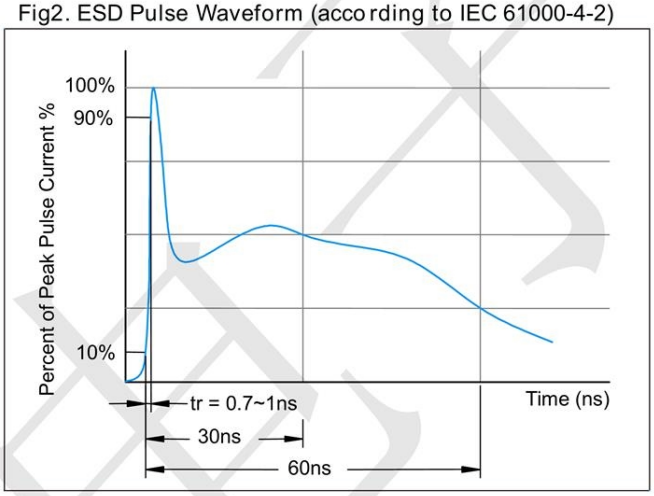
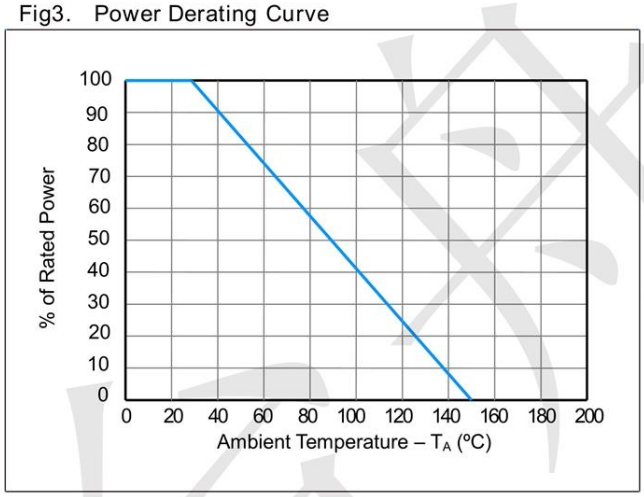
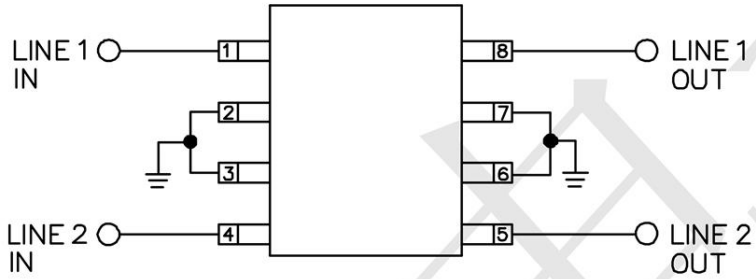


Fig3. Power Derating Curve

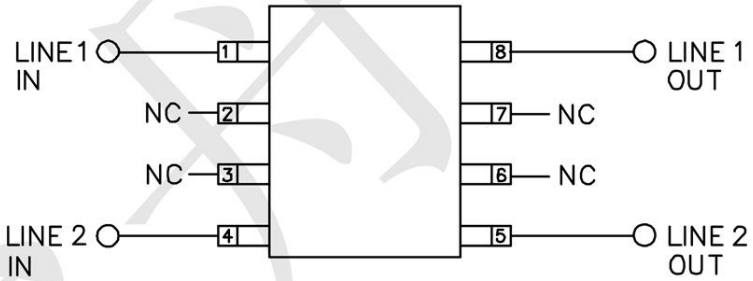


Typical Application

The LC03-6 is designed to protect two high speed data lines (one differential pair) from transient over - voltages which result from lightning and ESD. The device can be configured to protect in differential (Line to Line) and common (Line to Ground) mode. Data line inputs/outputs are connected at pins 1 to 8, and 4 to 5 as shown below. Pins 2, 3, 6, 7 are connected to ground. These pins should be connected directly to a ground plane on the board for the best results, the path length is kept as short as possible to minimize parasitic inductance. In applications where high common voltages are present, differential protection is achieved by leaving pins 2, 3, 6, and 7 not connected.

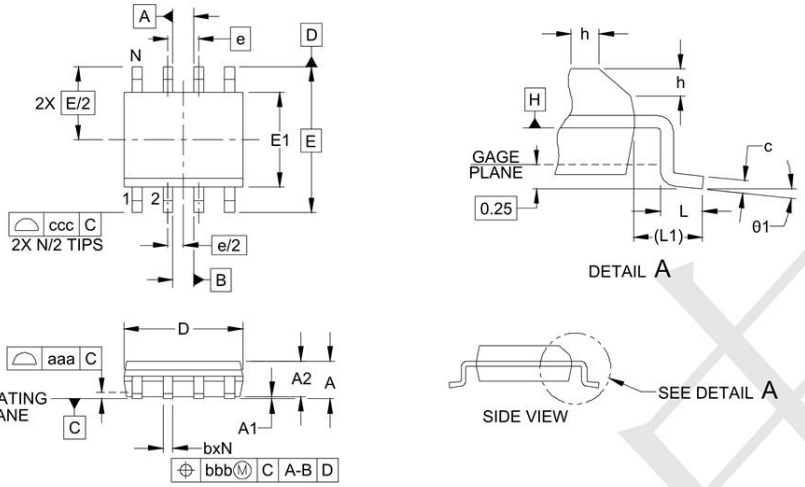


Connection for differential (Line to Line) and common mode protection (Line to Ground)



Connection for differential protection (Line to Line)

SOP-8 Package Outline Drawing



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

Suggested Land Pattern