

DESCRIPTION

The M5M5V108DFP,VP,KV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple-polysilicon and double metal CMOS technology. The use of thin film transistor (TFT) load cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M5V108DVP,KV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD).

FEATURES

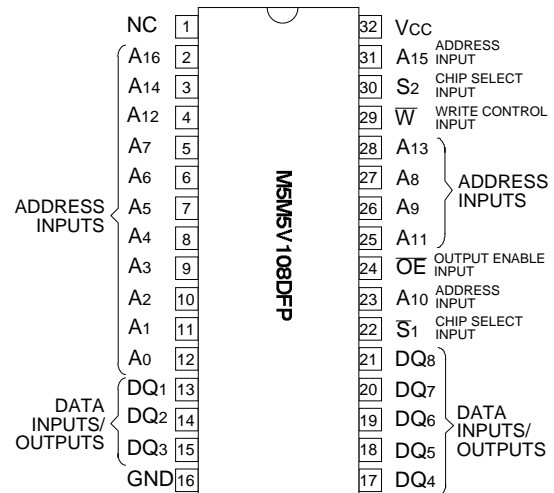
Type name	Access time (max)	V _{CC}	Power supply current	
			Active (1MHz) (max)	stand-by (max)
M5M5V108DFP,VP,KV-70H	70ns	2.7~3.6V	5mA	12μA

- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by \overline{S}_1, S_2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- \overline{OE} prevents data contention in the I/O bus
- Common data I/O
- Package

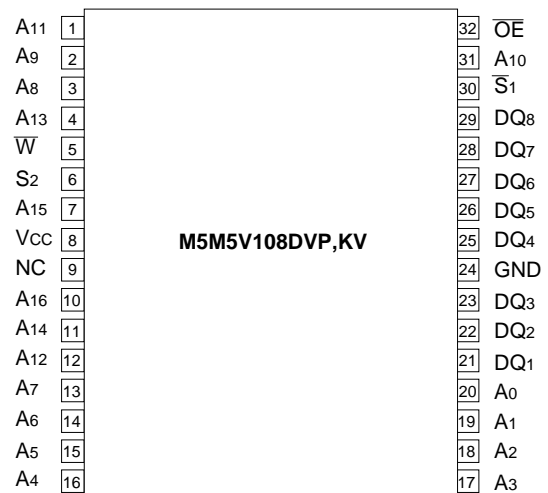
M5M5V108DFP 32pin 525mil SOP
 M5M5V108DVP,RV 32pin 8 X 20 mm² TSOP
 M5M5V108DKV,KR 32pin 8 X 13.4 mm² TSOP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)

Outline 32P2M-A



Outline 32P3H-E(VP), 32P3K-B(KV)

NC : NO CONNECTION

MITSUBISHI LSIs
M5M5V108DFP,VP,KV -70H

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5V108D series are determined by a combination of the device control inputs $\overline{S1}$, $S2$, \overline{W} and \overline{OE} .

Each mode is summarized in the function table.

A write cycle is executed whenever the low level \overline{W} overlaps with the low level $\overline{S1}$ and the high level $S2$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , $\overline{S1}$ or $S2$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

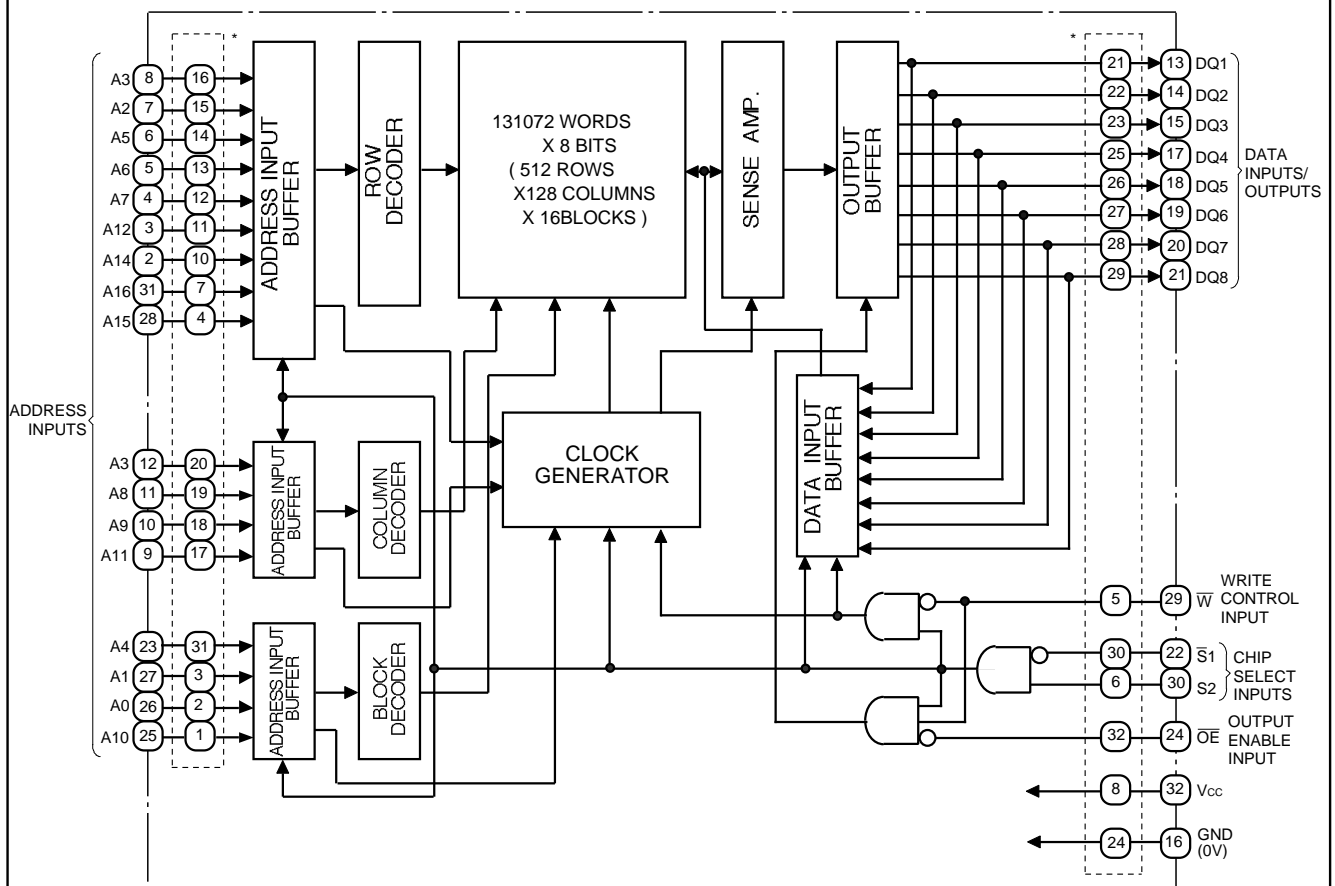
A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{S1}$ and $S2$ are in an active state ($\overline{S1}=L, S2=H$).

When setting $\overline{S1}$ at a high level or $S2$ at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and $S2$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	$S2$	\overline{W}	\overline{OE}	Mode	DQ	I _{CC}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP

7th.July.2000 Ver. 1.0
MITSUBISHI LSIs
M5M5V108DFP,VP,KV -70H
1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	-0.3*~4.6	V
V _I	Input voltage		-0.3*~V _{cc} + 0.3 (Max 4.6)	V
V _O	Output voltage		0~V _{cc}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width 30ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{cc}=2.7~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{cc} + 0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.6	V
V _{OH1}	High-level output voltage 1	I _{OH} = -0.5mA	2.4			V
V _{OH2}	High-level output voltage 2	I _{OH} = -0.05mA	V _{cc} - 0.5			V
V _{OL}	Low-level output voltage	I _{OL} = 2mA			0.4	V
I _I	Input current	V _I =0~V _{cc}			±1	µA
I _O	Output current in off-state	S ₁ =V _{IH} or S ₂ =V _{IL} or OE=V _{IH} V _{I/O} =0~V _{cc}			±1	µA
I _{CC1}	Active supply current	S ₁ =V _{IL} , S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} Output-open(duty 100%)	70ns		35	
I _{CC2}	Active supply current		1MHz		5	
I _{CC3}	Stand-by current	1) S ₂ 0.2V other inputs=0~V _{cc} 2) S ₁ V _{cc} -0.2V, S ₂ V _{cc} -0.2V other inputs=0~V _{cc}	-H	~25°C	1.2	µA
				~40°C	3.6	
				~70°C	12	
I _{CC4}	Stand-by current	S ₁ =V _{IH} or S ₂ =V _{IL} , other inputs=0~V _{cc}			0.33	mA

* -3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (T_a=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{cc} = 3V, T_a = 25°C

AC ELECTRICAL CHARACTERISTICS ($T_a=0\sim 70^\circ\text{C}$, unless otherwise noted)**(1) MEASUREMENT CONDITIONS**

VCC	2.7~3.6V
Input pulse level	$V_{IH}=2.2\text{V}, V_{IL}=0.4\text{V}$
Input rise and fall time	5ns
Reference level	$V_{OH}=V_{OL}=1.5\text{V}$
Output loads	Fig.1, $C_L=30\text{pF}$ $C_L=5\text{pF}$ (for t_{en}, t_{dis}) Transition is measured $\pm 500\text{mV}$ from steady state voltage. (for t_{en}, t_{dis})

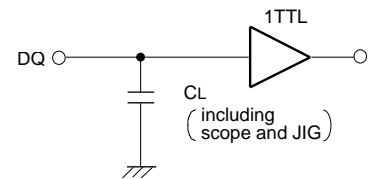


Fig.1 Output load

(2) READ CYCLE

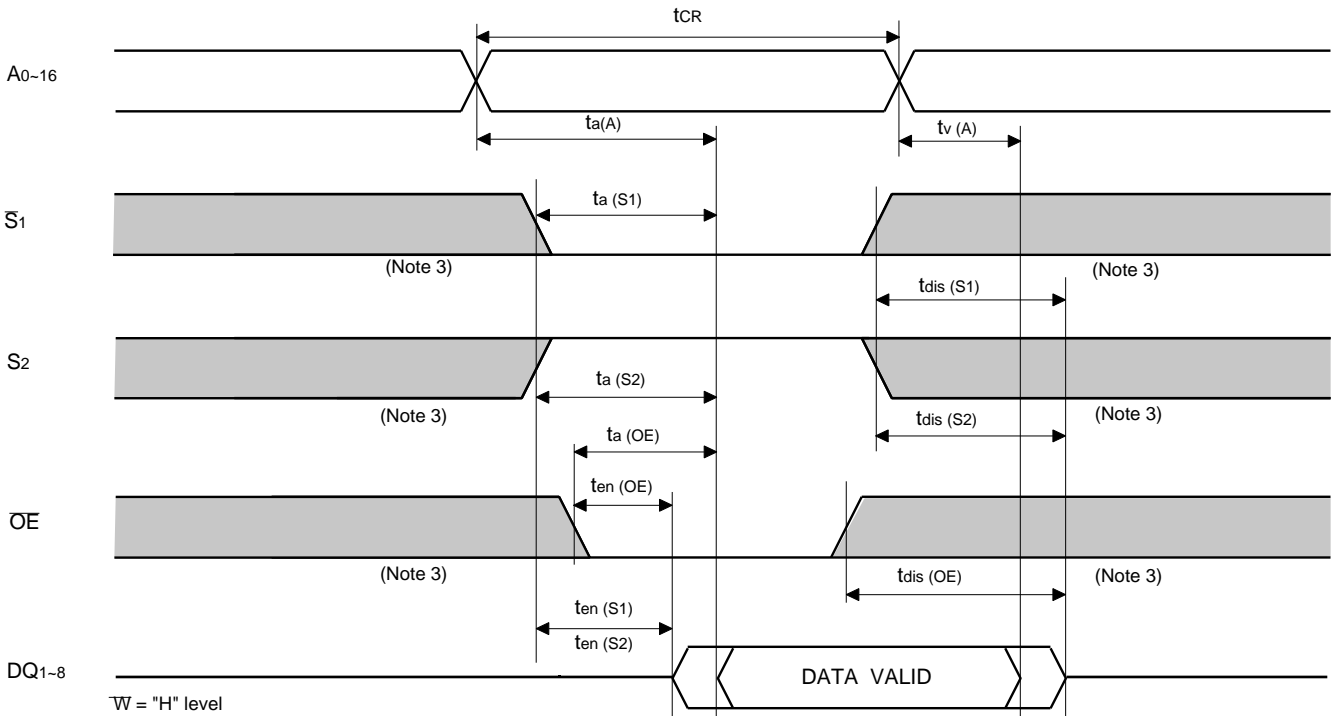
Symbol	Parameter	Limits		Unit
		-70H		
		Min	Max	
t_{CR}	Read cycle time	70		ns
$t_{a(A)}$	Address access time		70	ns
$t_{a(S1)}$	Chip select 1 access time		70	ns
$t_{a(S2)}$	Chip select 2 access time		70	ns
$t_{a(OE)}$	Output enable access time		35	ns
$t_{dis(S1)}$	Output disable time after $\overline{S1}$ high		25	ns
$t_{dis(S2)}$	Output disable time after $S2$ low		25	ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high		25	ns
$t_{en(S1)}$	Output enable time after $\overline{S1}$ low	10		ns
$t_{en(S2)}$	Output enable time after $S2$ high	10		ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	5		ns
$t_{v(A)}$	Data valid time after address	10		ns

(3) WRITE CYCLE

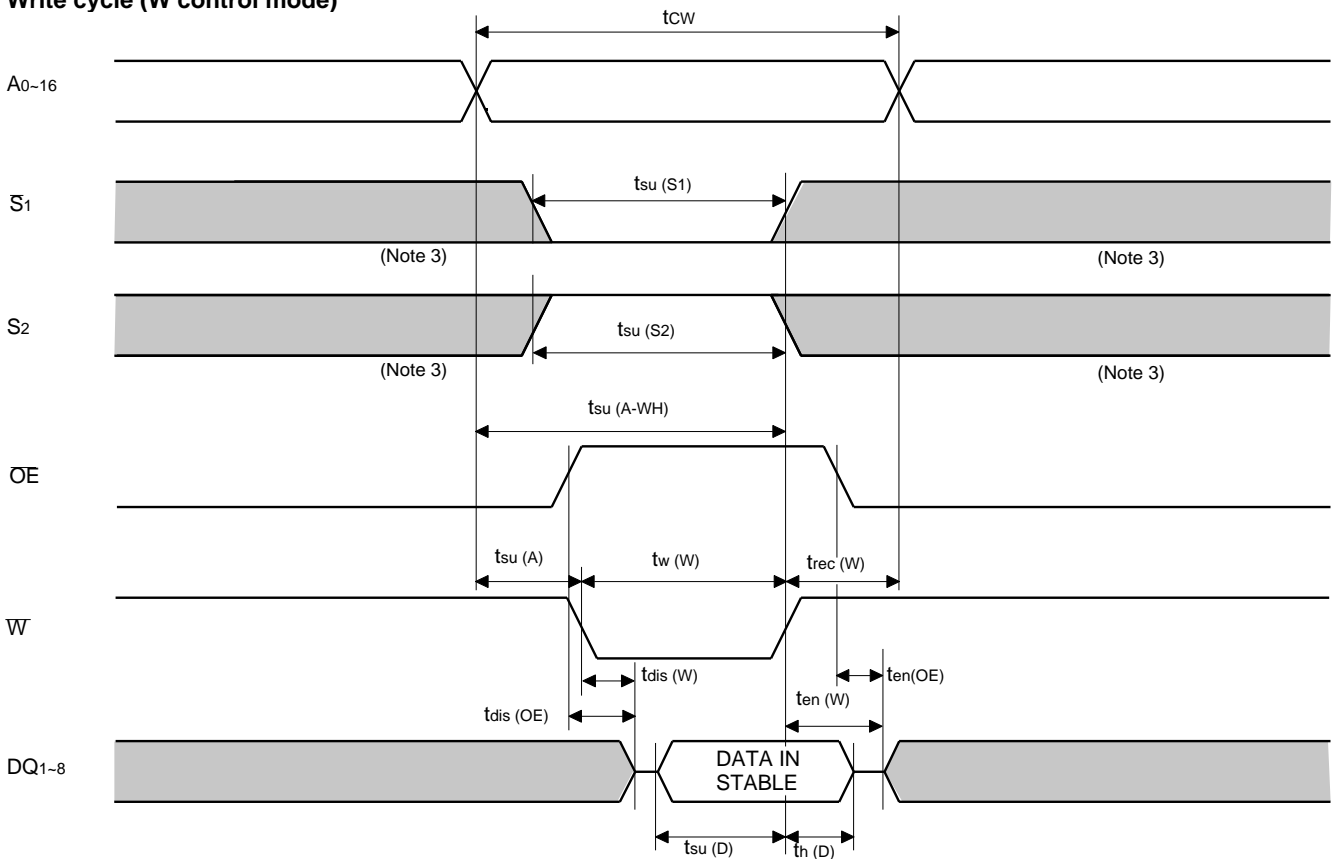
Symbol	Parameter	Limits		Unit
		-70H		
		Min	Max	
t_{CW}	Write cycle time	70		ns
$t_{w(W)}$	Write pulse width	55		ns
$t_{su(A)}$	Address setup time	0		ns
$t_{su(A-WH)}$	Address setup time with respect to \overline{W}	65		ns
$t_{su(S1)}$	Chip select 1 setup time	65		ns
$t_{su(S2)}$	Chip select 2 setup time	65		ns
$t_{su(D)}$	Data setup time	30		ns
$t_{h(D)}$	Data hold time	0		ns
$t_{rec(W)}$	Write recovery time	0		ns
$t_{dis(W)}$	Output disable time from \overline{W} low		25	ns
$t_{dis(OE)}$	Output disable time from \overline{OE} high		25	ns
$t_{en(W)}$	Output enable time from \overline{W} high	5		ns
$t_{en(OE)}$	Output enable time from \overline{OE} low	5		ns

(4) TIMING DIAGRAMS

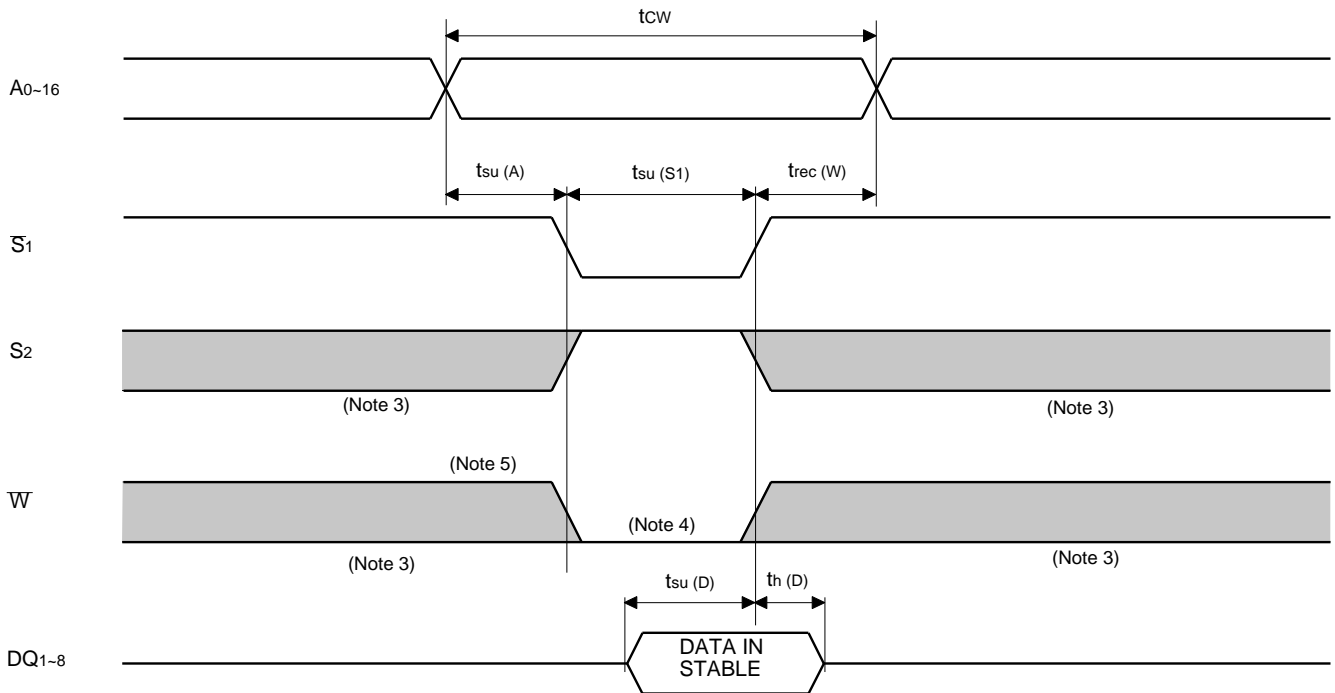
Read cycle



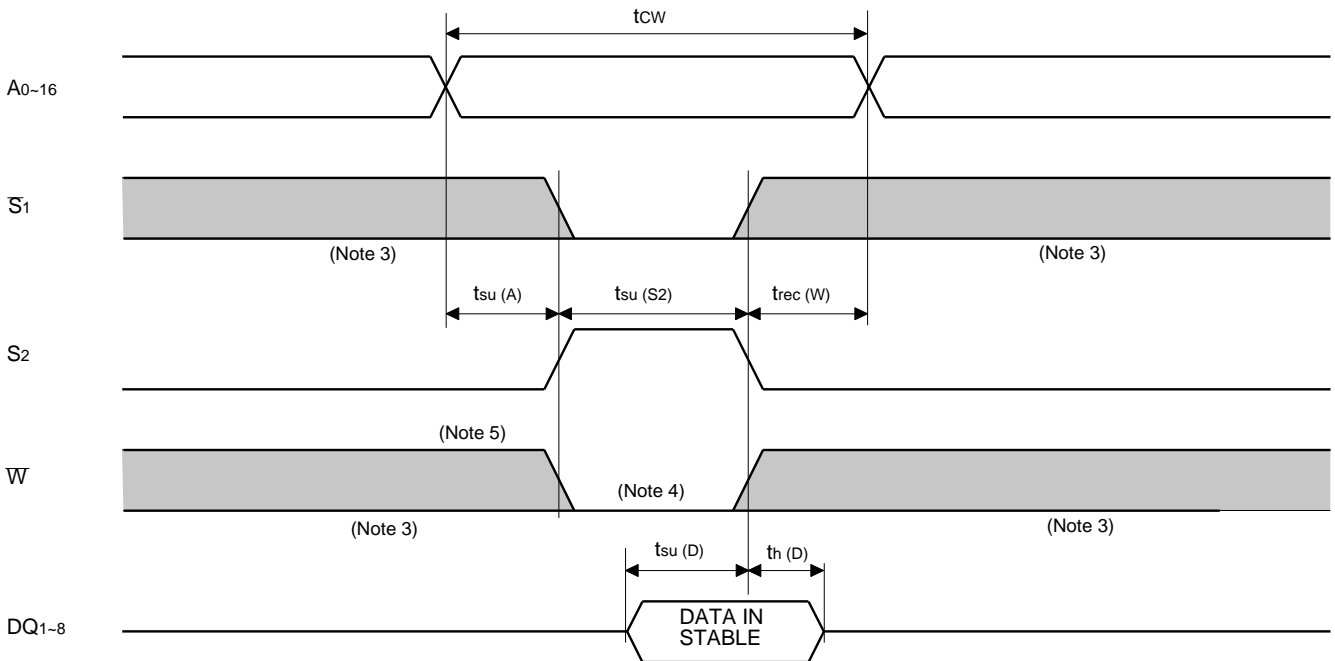
Write cycle (\bar{W} control mode)



Write cycle ($\overline{S1}$ control mode)



Write cycle (S_2 control mode)



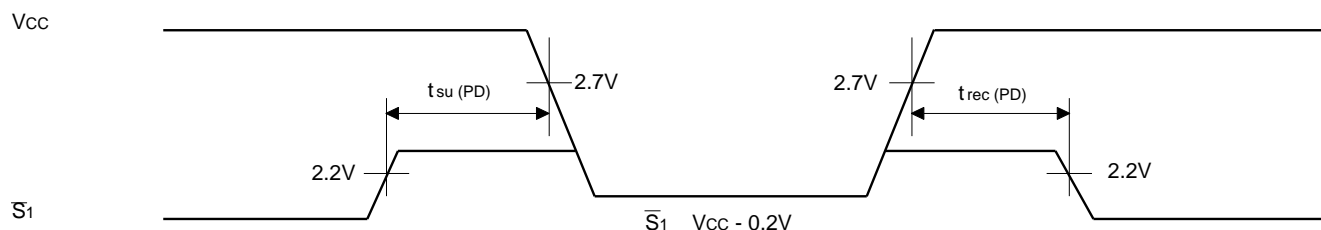
- Note 3: Hatching indicates the state is "don't care".
 4: Writing is executed while S_2 high overlaps $\overline{S_1}$ and \overline{W} low.
 5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{S_1}$ or rising edge of S_2 , the outputs are maintained in the high impedance state.
 6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS**(1) ELECTRICAL CHARACTERISTICS** ($T_a=0\sim 70^\circ\text{C}$, unless otherwise noted)

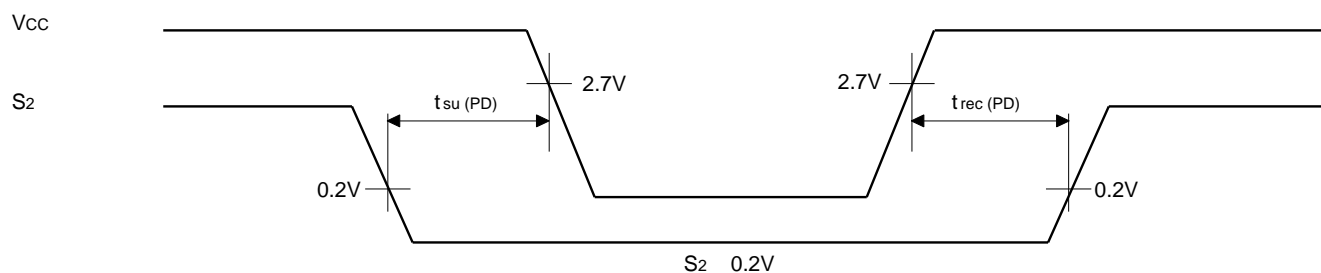
Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V_{CC} (PD)	Power down supply voltage		2			V	
V_I (S1)	Chip select input \overline{S}_1		2.0	$V_{CC}(\text{PD})$		V	
V_I (S2)	Chip select input S2	$2.7V \leq V_{CC}(\text{PD})$			0.6	V	
		$V_{CC}(\text{PD}) < 2.7V$			0.2	V	
I_{CC} (PD)	Power down supply current	$V_{CC} = 3V$ 1) $S_2 = 0.2V$, other inputs = $0\sim 3V$ 2) $\overline{S}_1 = V_{CC}-0.2V$, $S_2 = V_{CC}-0.2V$ other inputs = $0\sim 3V$	-H	$\sim 25^\circ\text{C}$		1	μA
				$\sim 40^\circ\text{C}$		3	
				$\sim 70^\circ\text{C}$		10	

(2) TIMING REQUIREMENTS ($T_a=0\sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{su} (PD)	Power down set up time		0			ns
t_{rec} (PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS **\overline{S}_1 control mode**

Note 7: On the power down mode by controlling \overline{S}_1 , the input level of S2 must be $S_2 = V_{CC} - 0.2V$ or $S_2 = 0.2V$. The other pins(Address,I/O, \overline{WE} , \overline{OE}) can be in high impedance state.

S2 control mode

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