HM53461 Series

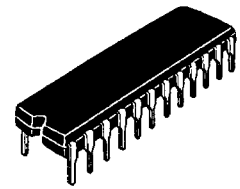
65,536-word x 4-bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM53461 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

Utilizing the Hitachi 2 μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

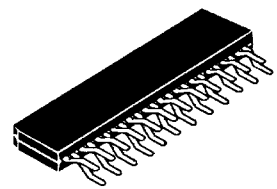
HM53461P Series



3DDP24A

(DP-24A)

HM53461ZP Series



3DZP24

(ZP-24)

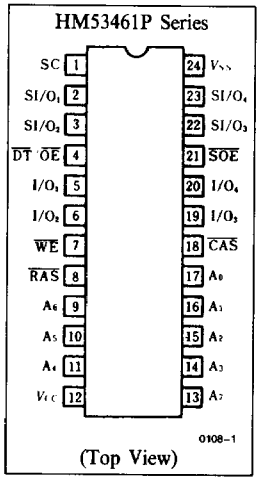
■ FEATURES

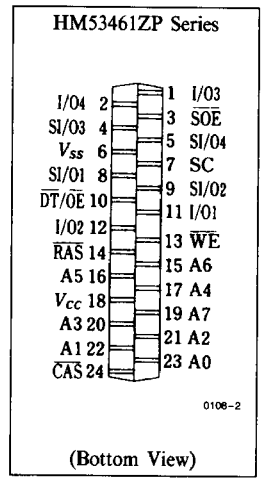
- Multiport Organization
  (RAM; 64k-word x 4-bit and SAM; 256 word x 4-bit)
- Double Layer Polysilicon/Polyicide n-Well CMOS Process
- Single 5V (±10%)
- Low Power
  - Active
    - RAM ..... 380 mW (max)
    - SAM ..... 220 mW (max)
  - Standby ..... 40 mW (max)
- Access Time
  - RAM ..... 100 ns/120 ns/150 ns
  - SAM ..... 40 ns/40 ns/60 ns
- Cycle Time Random Read or Write Cycle Time (RAM) ..... 190 ns/220 ns/260 ns
  Serial Read or Write Cycle Time (SAM) ..... 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles ..... 4 ms
- Refresh Function
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Data Transfer Operation (RAM ⟷ SAM)
- Fast Serial Access Operation Asynchronized with RAM Port Except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53461P-10	100 ns	400 mil 24-pin Plastic DIP (DP-24A)
HM53461P-12	120 ns	
HM53461P-15	150 ns	
HM53461ZP-10	100 ns	24-pin Plastic ZIP (ZP-24)
HM53461ZP-12	120 ns	
HM53461ZP-15	150 ns	

■ PIN OUT

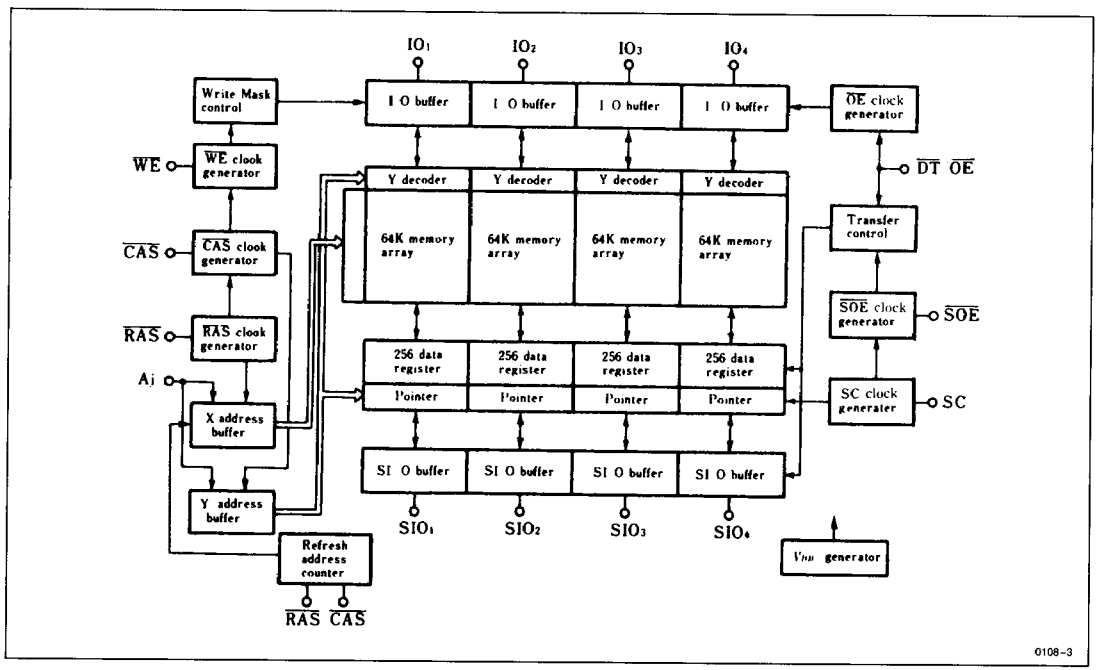




■ PIN DESCRIPTION

Pin Name	Function
A_0–A_7	Address Inputs
I/O_1–I/O_4	RAM Port Data Input/Output
SI/O_1–SI/O_4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Power Supply Voltage Relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Operating Temperature, T_A (Ambient)	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	SAM PORT		HM53461-10	HM53461-12	HM53461-15	Unit	RAM PORT	Note
		Standby	Active					Test Conditions	
Operating Current	I_{CC1}	—	×	70	60	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	
	I_{CC7}	×	—	110	100	80	mA		
Standby Current	I_{CC2}	—	×	7	7	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	
	I_{CC8}	×	—	40	40	30	mA		
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	×	60	50	40	mA	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling t_{RC} = Min	
	I_{CC9}	×	—	100	90	70	mA		
Page Mode Current	I_{CC4}	—	×	50	40	35	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling t_{PC} = Min	
	I_{CC10}	×	—	90	80	65	mA		
CBR Refresh Current	I_{CC5}	—	×	60	50	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	
	I_{CC11}	×	—	100	90	70	mA		
Data Transfer Current	I_{CC6}	—	×	75	65	55	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	
	I_{CC12}	×	—	115	105	85	mA		

Parameter	Symbol	Min	Max	Unit	Test Conditions	Note
Input Leakage	I_{LI}	−10	10	μA		
Output Leakage	I_{LO}	−10	10	μA		
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = −2 mA	
Output Low Voltage	V_{OL}	—	0.4	V	I_{OL} = 4.2 mA	

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	Typ	Max	Unit	Note
Address	C_{I1}	—	5	pF	
Clocks	C_{I2}	—	5	pF	
I/O, SI/O	$C_{I/O}$	—	7	pF	

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 10, 11]

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t_{PC}	70	—	85	—	105	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	3, 4
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	—	100	—	125	—	ns	8
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	—	40	—	45	—	ns	
Serial Clock Cycle Time	t_{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	40	—	40	—	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	—	25	—	30	—	40	ns	10

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

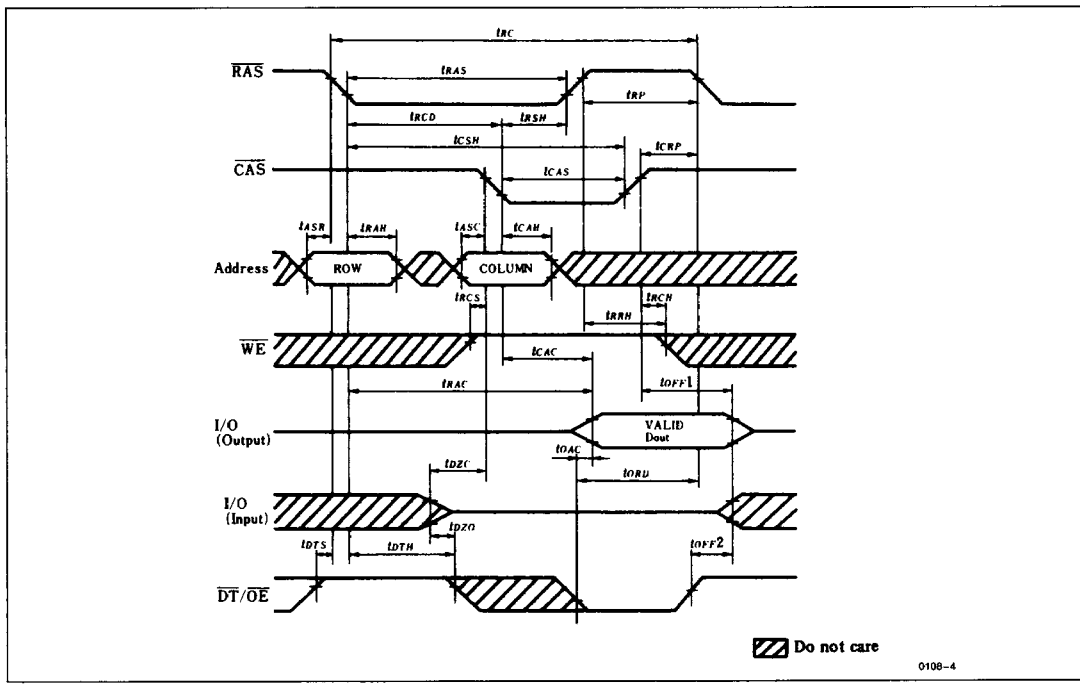
(T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 10, 11] (continued)

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup TIme	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Transfer Cycle)	t_{RDH}	80	—	90	—	110	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	—	10	—	10	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ms	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
$\overline{SC}$ to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	35	—	35	—	55	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	—	35	—	55	—	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	—	10	—	10	—	ns	

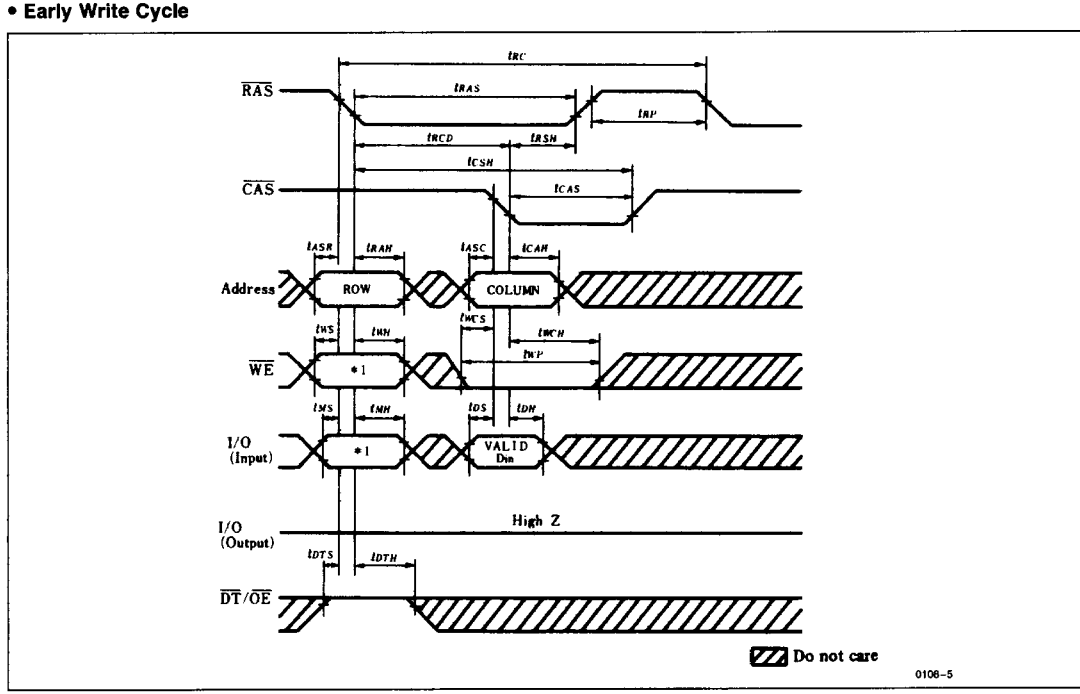
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
10. Measured with a load circuit equivalent to 2 TTL and 50 pF.
11. An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.

■ TIMING WAVEFORMS

• Read Cycle

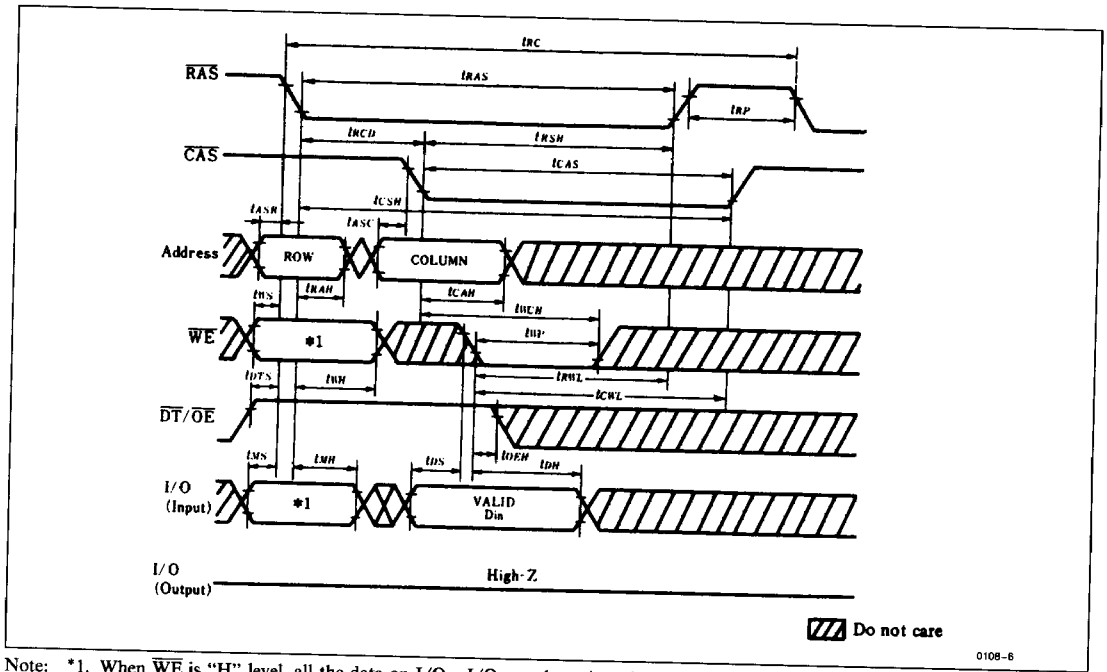


• Early Write Cycle



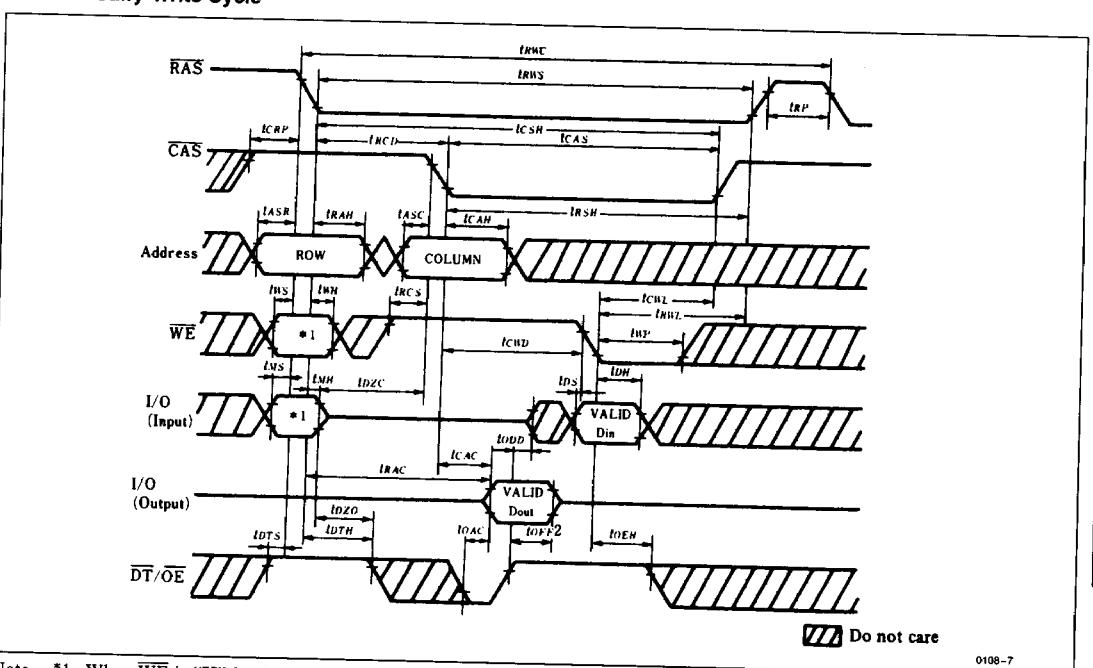
Note: *1. When $\overline{WE}$ is "H" level, all the data on the I/O can be written into the cell.
When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



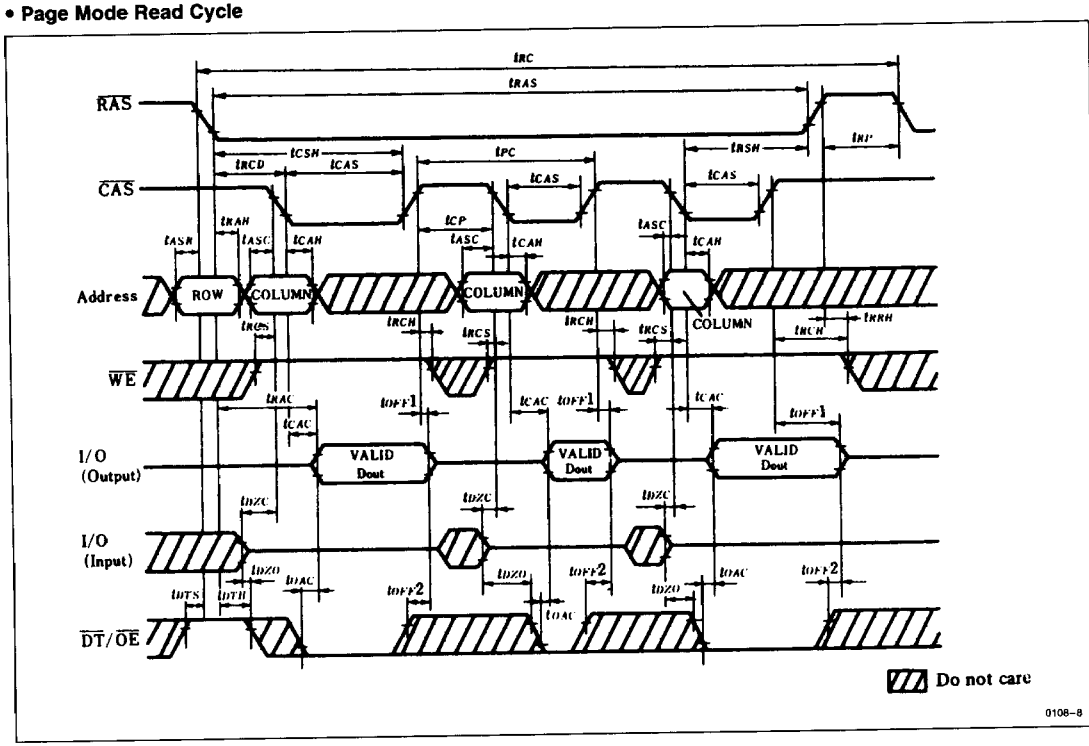
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

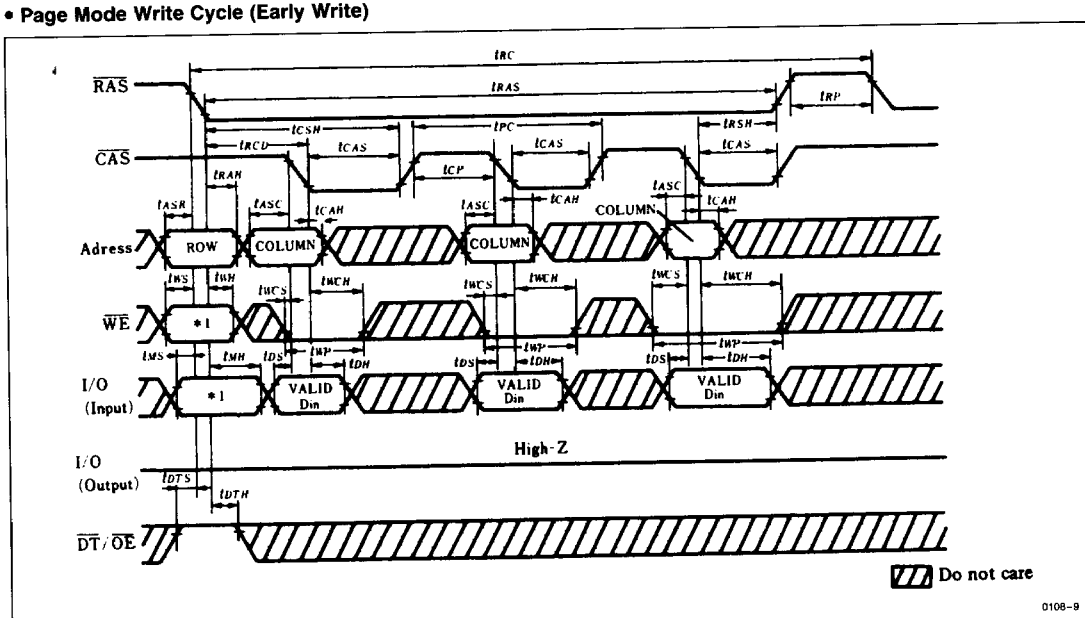


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

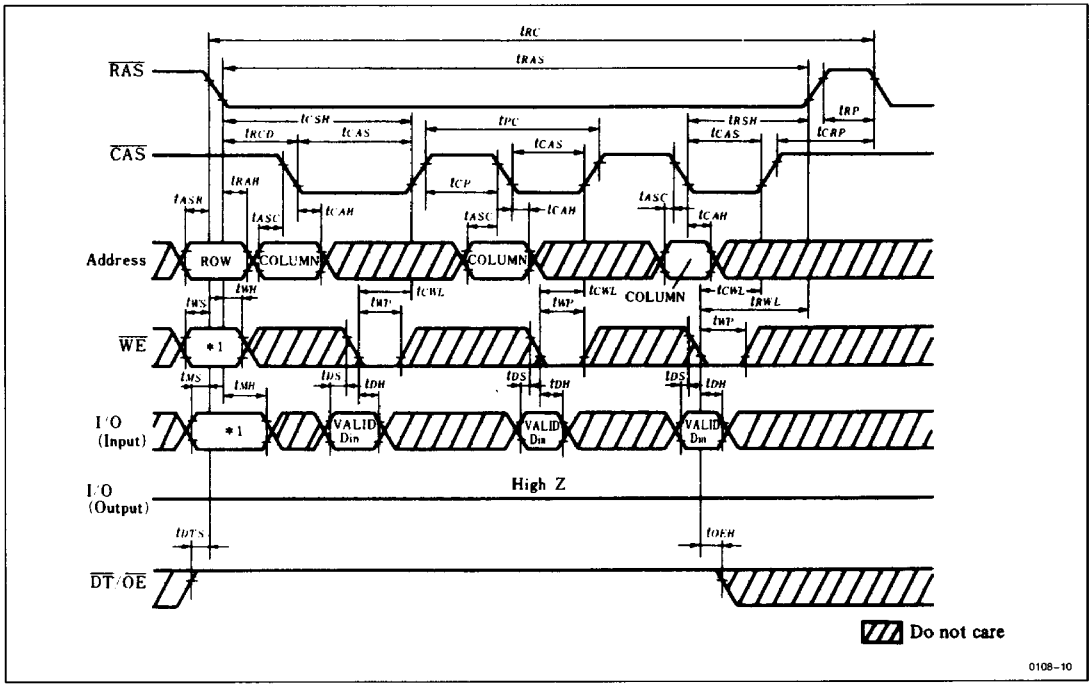


• **Page Mode Write Cycle (Early Write)**



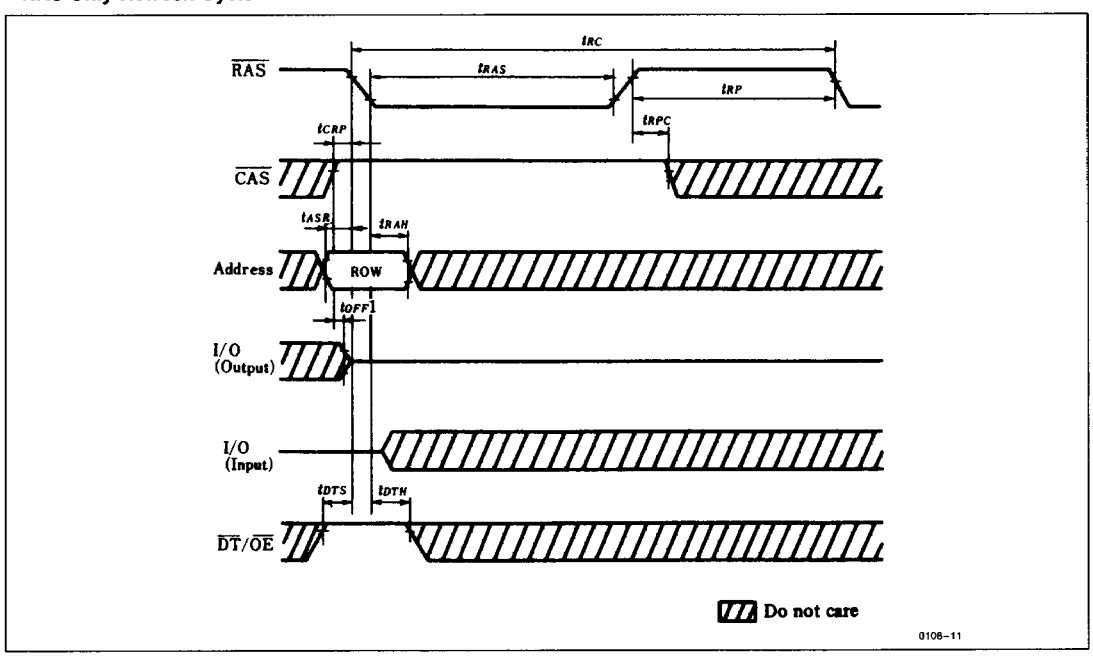
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Delayed Write)**

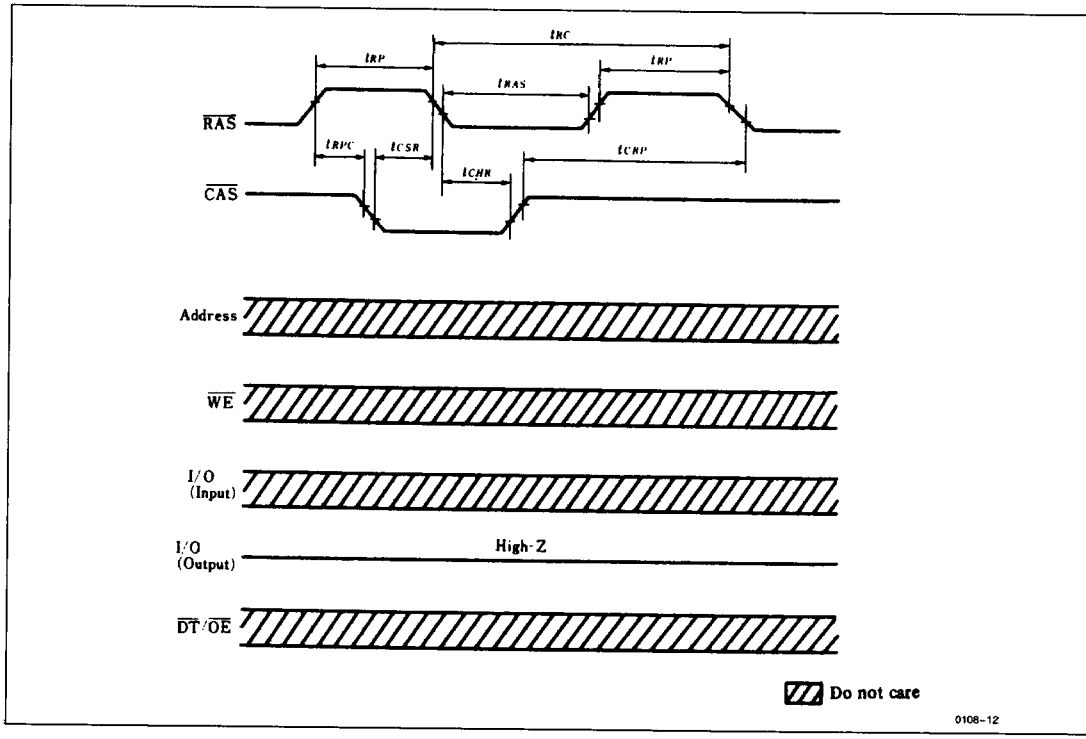


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

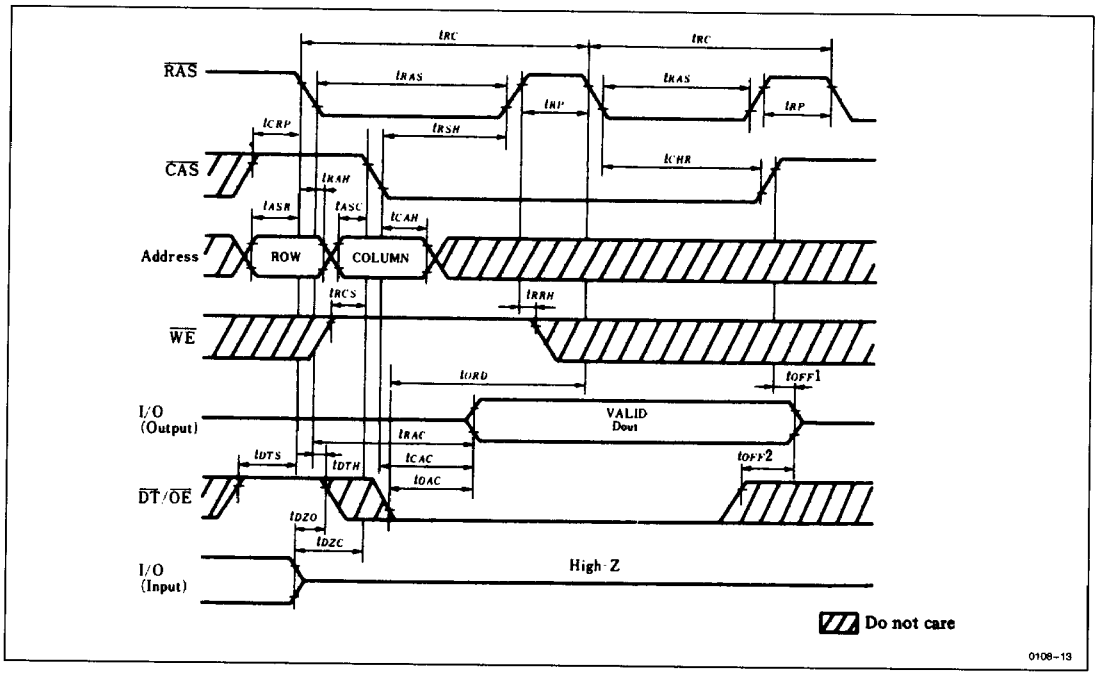
• **$\overline{RAS}$ Only Refresh Cycle**



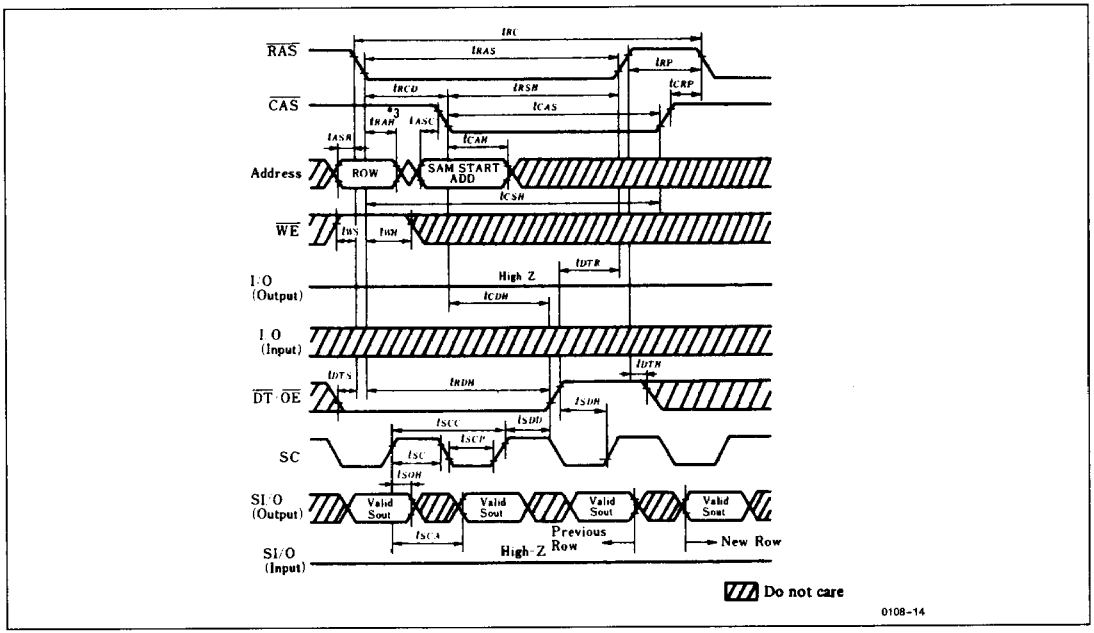
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle

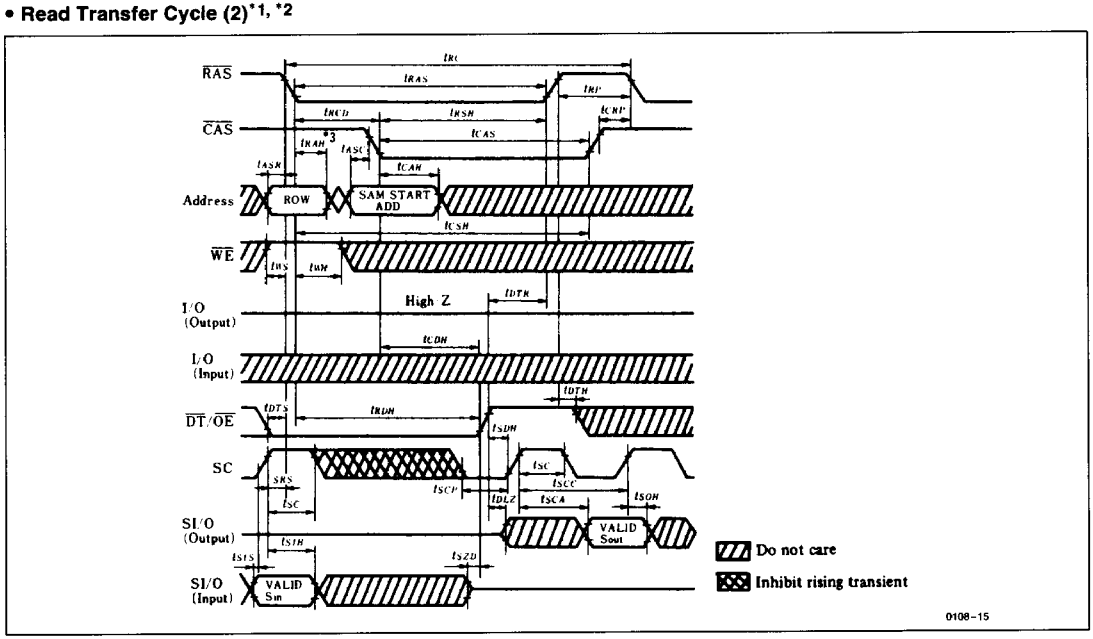


• Read Transfer Cycle (1)*1, *2



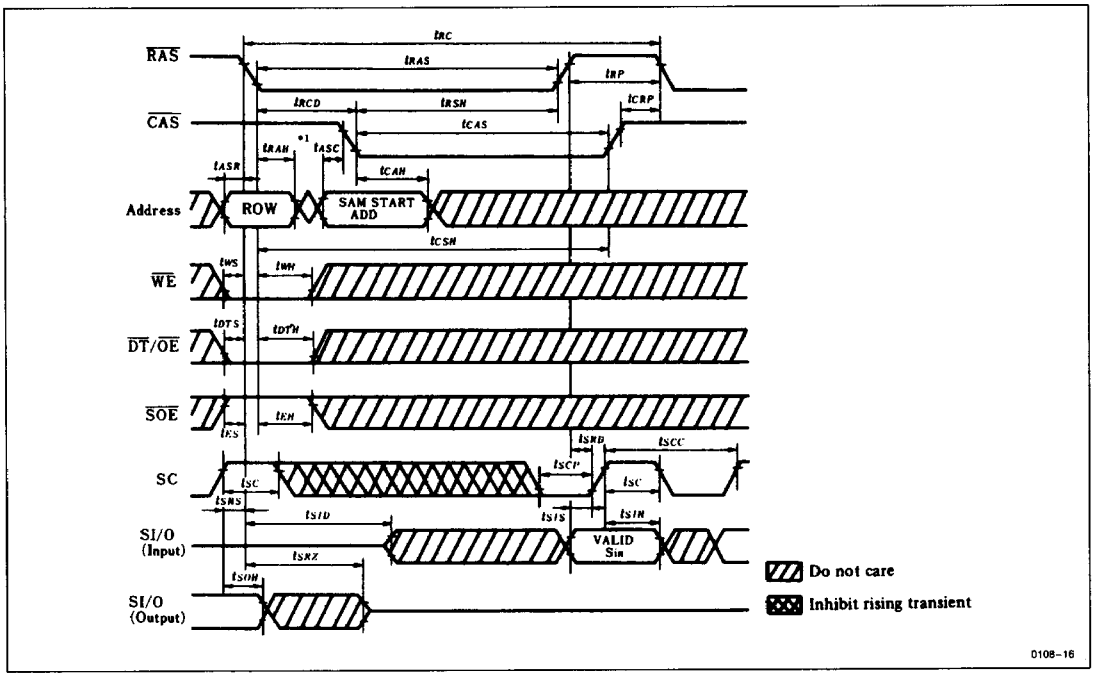
Notes: *1. In the case that the previous data transfer cycle was read transfer.
*2. Assume that $\overline{SOE}$ is "L" level.
*3. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• Read Transfer Cycle (2)*1, *2



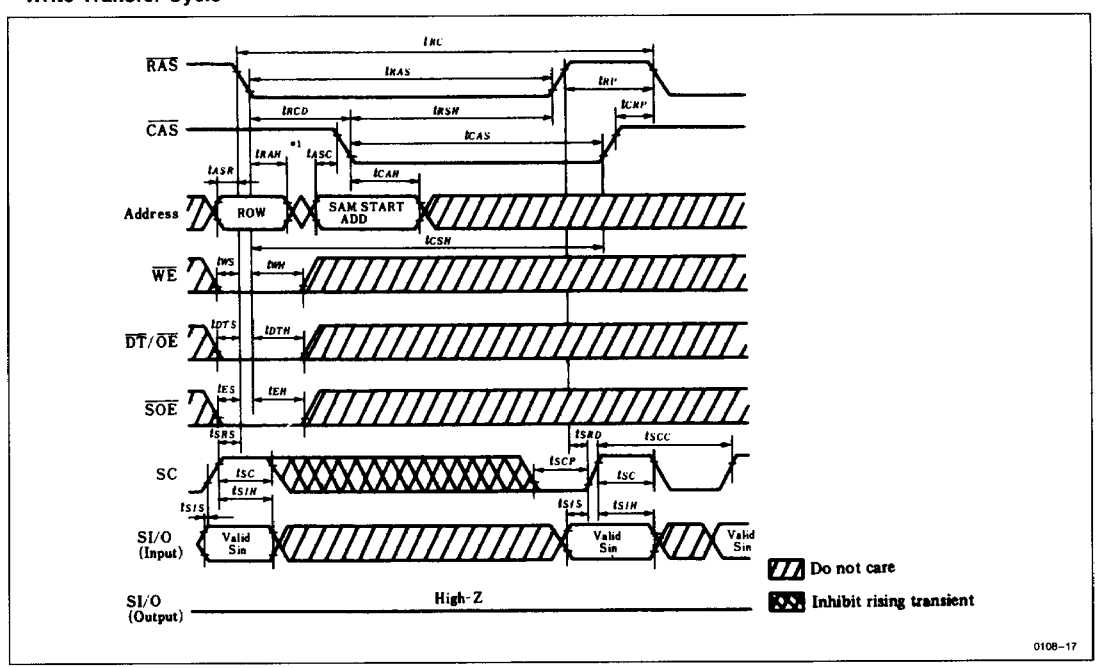
Notes: *1. In the case that the previous data transfer cycle was write transfer or pseudo transfer.
*2. Assume that $\overline{SOE}$ is "L" level.
*3. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Pseudo Transfer Cycle**



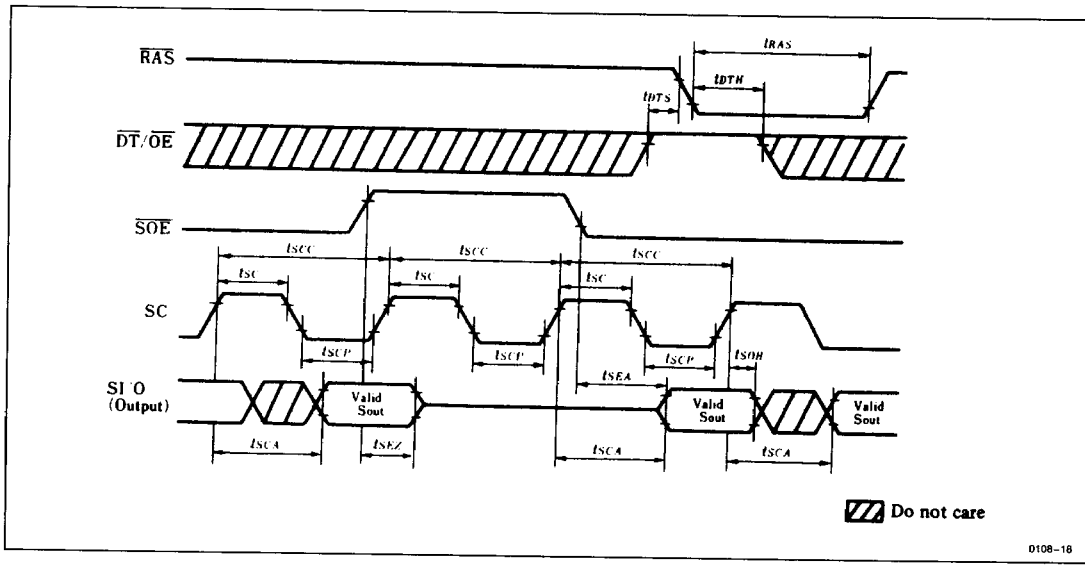
Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Write Transfer Cycle**



Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Serial Read Cycle**



• **Serial Write Cycle**

