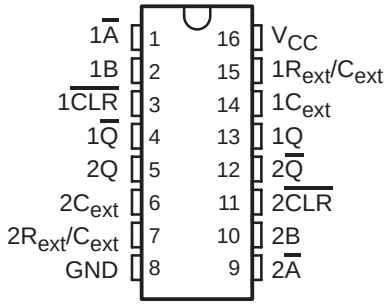
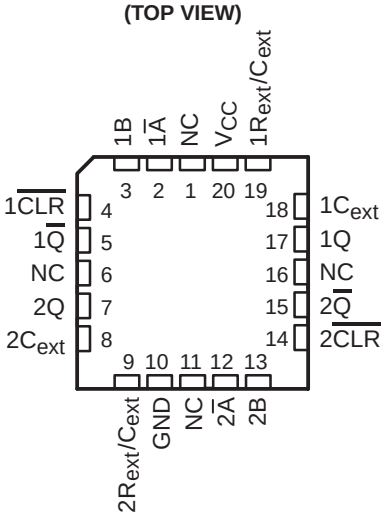
- **2-V to 5.5-V $V_{CC}$ Operation**
- **Max $t_{pd}$ of 11 ns at 5 V**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Input Transition Rates**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**SN54LV221A . . . J OR W PACKAGE**
**SN74LV221A . . . D, DB, DGV, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54LV221A . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SOIC − D | Tube of 40 | SN74LV221AD | LV221A |
| | | Reel of 2500 | SN74LV221ADR | |
| | SOP − NS | Reel of 2000 | SN74LV221ANSR | 74LV221A |
| | SSOP − DB | Reel of 2000 | SN74LV221ADBR | LV221A |
| | TSSOP − PW | Tube of 90 | SN74LV221APW | LV221A |
| | | Reel of 2000 | SN74LV221APWR | |
| | | Reel of 250 | SN74LV221APWT | |
| | TVSOP − DGV | Reel of 2000 | SN74LV221ADGVR | LV221A |
| −55°C to 125°C | CDIP − J | Tube of 25 | SNJ54LV221AJ | SNJ54LV221AJ |
| | CFP − W | Tube of 150 | SNJ54LV221AW | SNJ54LV221AW |
| | LCCC − FK | Tube of 55 | SNJ54LV221AFK | SNJ54LV221AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## description/ordering information (continued)

The ’LV221A devices are dual multivibrators designed for 2-V to 5.5-V $V_{CC}$ operation. Each multivibrator has a negative-transition-triggered ($\overline{A}$) input and a positive-transition-triggered (B) input, either of which can be used as an inhibit input.

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low and the B input goes high. In the second method, the B input is high and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between $C_{ext}$ and $R_{ext}/C_{ext}$(positive) and an external resistor connected between $R_{ext}/C_{ext}$ and $V_{CC}$. To obtain variable pulse durations, connect an external variable resistor between $R_{ext}/C_{ext}$ and $V_{CC}$. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not related directly to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the outputs are independent of further transitions of the $\overline{A}$ and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse duration can be varied by choosing the appropriate timing components. Output rise and fall times are TTL compatible and independent of pulse duration. Typical triggering and clearing sequences are illustrated in the input/output timing diagram.

The variance in output pulse duration from device to device typically is less than ±0.5% for given external timing components. An example of this distribution for the ’LV221A is shown in Figure 8. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 5.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

Pin assignments are identical to those of the ’AHC123A and ’AHCT123A devices, so the ’LV221A can be substituted for those devices not using the retrigger feature.

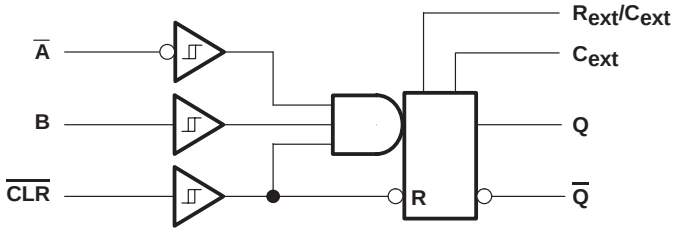
For additional application information on multivibrators, see the application report *Designing With The SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

**FUNCTION TABLE**
**(each multivibrator)**

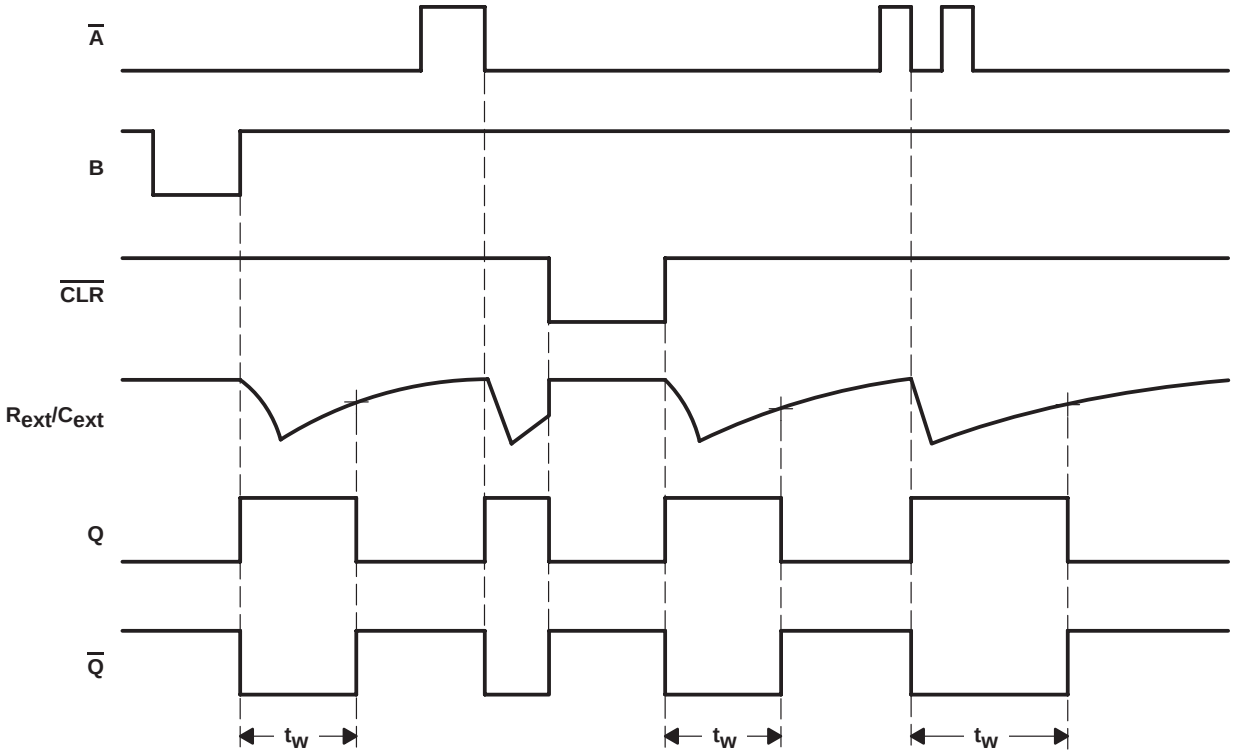
| INPUTS | | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{A}$ | B | Q | $\overline{Q}$ | |
| L | X | X | L | H | Reset |
| H | H | X | L | H | Inhibit |
| H | X | L | L | H | Inhibit |
| H | L | ↑ | ⎍ | ⎎ | Outputs enabled |
| H | ↓ | H | ⎍ | ⎎ | Outputs enabled |
| ↑† | L | H | ⎍ | ⎎ | Outputs enabled |

† This condition is true only if the output of the latch formed by the NAND gate has been conditioned to the logic 1 state prior to $\overline{CLR}$ going high. This latch is conditioned by taking either $\overline{A}$ high or B low while $\overline{CLR}$ is inactive (high).

## logic diagram, each multivibrator (positive logic)




## input/output timing diagram



### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | −0.5 V to 7 V |
| Output voltage range in high or low state, $V_O$ (see Notes 1 and 2) | −0.5 V to $V_{CC}$ + 0.5 V |
| Output voltage range in power-off state, $V_O$ (see Note 1) | −0.5 V to 7 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | −20 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0) | −50 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±25 mA |
| Continuous current through $V_{CC}$ or GND | ±50 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package | 73°C/W |
| DB package | 82°C/W |
| DGV package | 120°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | SN54LV221A | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | −50 | | −50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | −2 | | −2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | −6 | | −6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | −12 | | −12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | | 12 | |
| $R_{ext}$ | External timing resistance | $V_{CC}$ = 2 V | 5k | | 5k | | Ω |
| | | $V_{CC} \geq$ 3 V | 1k | | 1k | | |
| $C_{ext}$ | External timing capacitance | | No restriction | | No restriction | | pF |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 1 | | 1 | | ms/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |



NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | SN54LV221A | | | SN74LV221A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | | $I_{OH}$ = −50 μA | 2 V to 5.5 V | $V_{CC}$−0.1 | | | $V_{CC}$−0.1 | | | V |
| | | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | 2 | | | |
| | | $I_{OH}$ = −6 mA | 3 V | 2.48 | | | 2.48 | | | |
| | | $I_{OH}$ = −12 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.44 | |
| | | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $R_{ext}/C_{ext}$† | $V_I$ = 5.5 V or GND | 2 V to 5.5 V | | | ±2.5 | | | ±2.5 | μA |
| | $\overline{A}$, B, and $\overline{CLR}$ | $V_I$ = 5.5 V or GND | 0 | | | ±1 | | | ±1 | |
| | | | 0 to 5.5 V | | | ±1 | | | ±1 | |
| $I_{CC}$ | Quiescent | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | μA |
| $I_{CC}$ | Active state (per circuit) | $V_I = V_{CC}$ or GND, $R_{ext}/C_{ext}$ = 0.5 $V_{CC}$ | 2.3 V | | | 220 | | | 220 | μA |
| | | | 3 V | | | 280 | | | 280 | |
| | | | 4.5 V | | | 650 | | | 650 | |
| | | | 5.5 V | | | 975 | | | 975 | |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | | | | 5 | μA |
| $C_i$ | | $V_I = V_{CC}$ or GND | 3.3 V | | 1.9 | | | 1.9 | | pF |
| | | | 5 V | | 1.9 | | | 1.9 | | |

† This test is performed with the terminal in the off-state condition.

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54LV221A | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ | 6 | | 6.5 | | 6.5 | | ns |
| | | $\overline{A}$ or B trigger | 6 | | 6.5 | | 6.5 | | |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54LV221A | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ | 5 | | 5 | | 5 | | ns |
| | | $\overline{A}$ or B trigger | 5 | | 5 | | 5 | | |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | SN54LV221A | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ | 5 | | 5 | | 5 | | ns |
| | | $\overline{A}$ or B trigger | 5 | | 5 | | 5 | | |

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN54LV221A | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 14.6* | 31.4* | 1* | 37* | 1 | 37 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 13.2* | 25* | 1* | 29.5* | 1 | 29.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 15.2* | 33.4* | 1* | 39* | 1 | 39 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 16.7 | 36 | 1 | 42 | 1 | 42 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 15 | 32.8 | 1 | 34.5 | 1 | 34.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 17.4 | 38 | 1 | 44 | 1 | 44 | |
| $t_w$† | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 203 | 260 | | 320 | | 320 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | 110 | 90 | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | ms |
| $\Delta t_w$‡ | | | $C_L$ = 50 pF | | ±1 | | | | | | % |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† $t_w$ = Pulse duration at Q and $\overline{Q}$ outputs
‡ $\Delta t_w$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN54LV221A | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 10.2* | 20.6* | 1* | 24* | 1 | 24 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 9.3* | 15.8* | 1* | 18.5* | 1 | 18.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 10.6* | 22.4* | 1* | 26* | 1 | 26 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 11.8 | 24.1 | 1 | 27.5 | 1 | 27.5 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 10.6 | 19.3 | 1 | 22 | 1 | 22 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 12.3 | 25.9 | 1 | 29.5 | 1 | 29.5 | |
| $t_w$† | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 186 | 240 | | 300 | | 300 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | 110 | 90 | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | ms |
| $\Delta t_w$‡ | | | $C_L$ = 50 pF | | ±1 | | | | | | % |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† $t_w$ = Pulse duration at Q and $\overline{Q}$ outputs
‡ $\Delta t_w$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN54LV221A | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.1* | 12* | 1* | 14* | 1 | 14 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 6.5* | 9.4* | 1* | 11* | 1 | 11 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 7.3* | 12.9* | 1* | 15* | 1 | 15 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 8.2 | 14 | 1 | 16 | 1 | 16 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 7.4 | 11.4 | 1 | 13 | 1 | 13 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 8.6 | 14.9 | 1 | 17 | 1 | 17 | |
| $t_w$† | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 171 | 200 | | 240 | | 240 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | 110 | 90 | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | ms |
| $\Delta t_w$‡ | | | $C_L$ = 50 pF | | ±1 | | | | | | % |

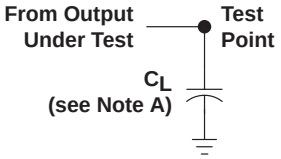


* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† $t_w$ = Pulse duration at Q and $\overline{Q}$ outputs
‡ $\Delta t_w$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

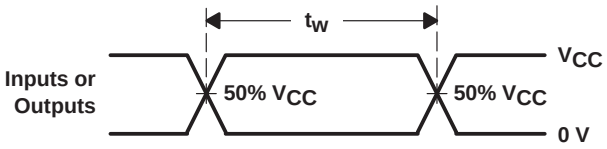
## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 10 MHz | 3.3 V | 50 | pF |
| | | | 5 V | 51 | |

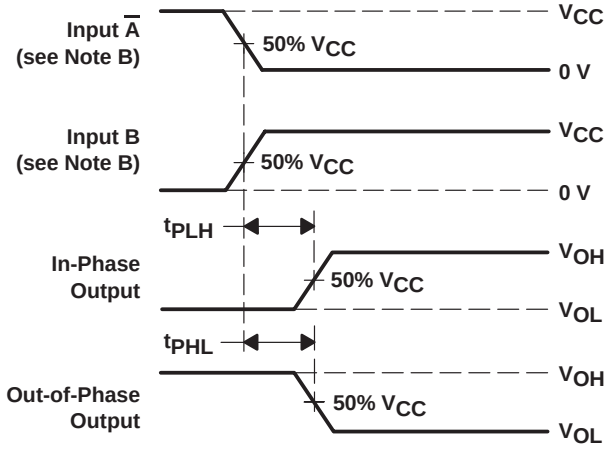
## PARAMETER MEASUREMENT INFORMATION



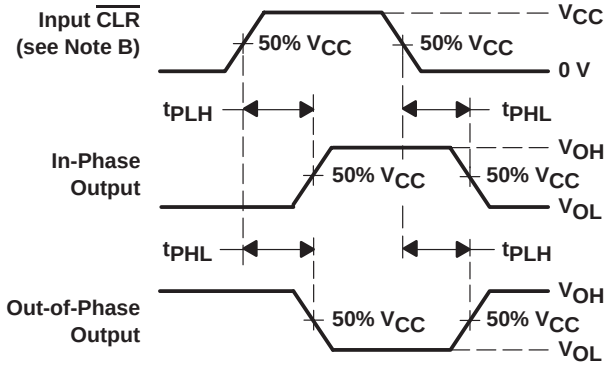

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## APPLICATION INFORMATION

### caution in use

To prevent malfunctions due to noise, connect a high-frequency capacitor between $V_{CC}$ and GND, and keep the wiring between the external components and $C_{ext}$ and $R_{ext}/C_{ext}$ terminals as short as possible.

### power-down considerations

Large values of $C_{ext}$ can cause problems when powering down the ’LV221A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from $V_{CC}$ through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the $V_{CC}$ power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if $V_{CC}$ = 5 V and $C_{ext}$ = 15 pF, the $V_{CC}$ supply must turn off no faster than $t = (5\ V) \times (15\ pF)/30\ mA = 2.5$ ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of $V_{CC}$ to zero occurs, the ’LV221A can sustain damage. To avoid this possibility, use external clamping diodes.

### output pulse duration

The output pulse duration, $t_w$, is determined primarily by the values of the external capacitance ($C_T$) and timing resistance ($R_T$). The timing components are connected as shown in Figure 2.

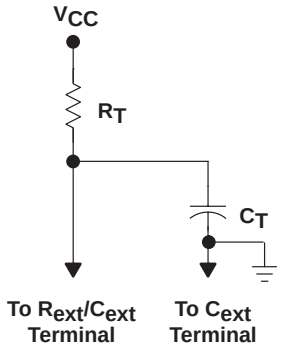



**Figure 2. Timing-Component Connections**

The pulse duration is given by:

$$t_w = K \times R_T \times C_T \quad (1)$$

if $C_T$ is ≥ 1000 pF, K = 1.0

or

if $C_T$ is < 1000 pF, K can be determined from Figure 7

where:

$t_w$ = pulse duration in ns
$R_T$ = external timing resistance in kΩ
$C_T$ = external capacitance in pF
K = multiplier factor

Equation 1 and Figure 3 or 4 can be used to determine values for pulse duration, external resistance, and external capacitance.

## APPLICATION INFORMATION†

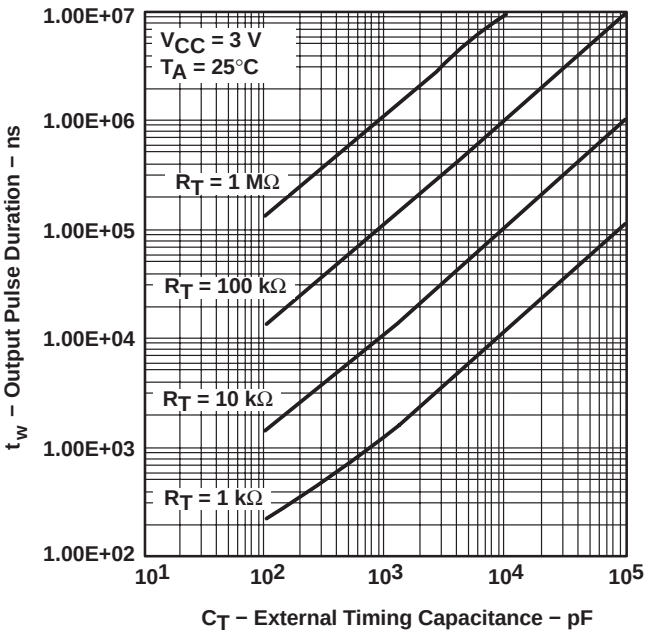



**Figure 3**

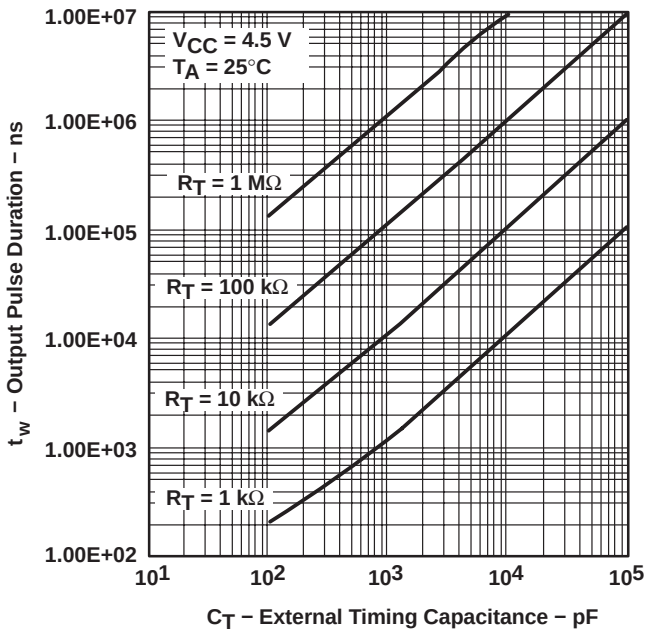



**Figure 4**

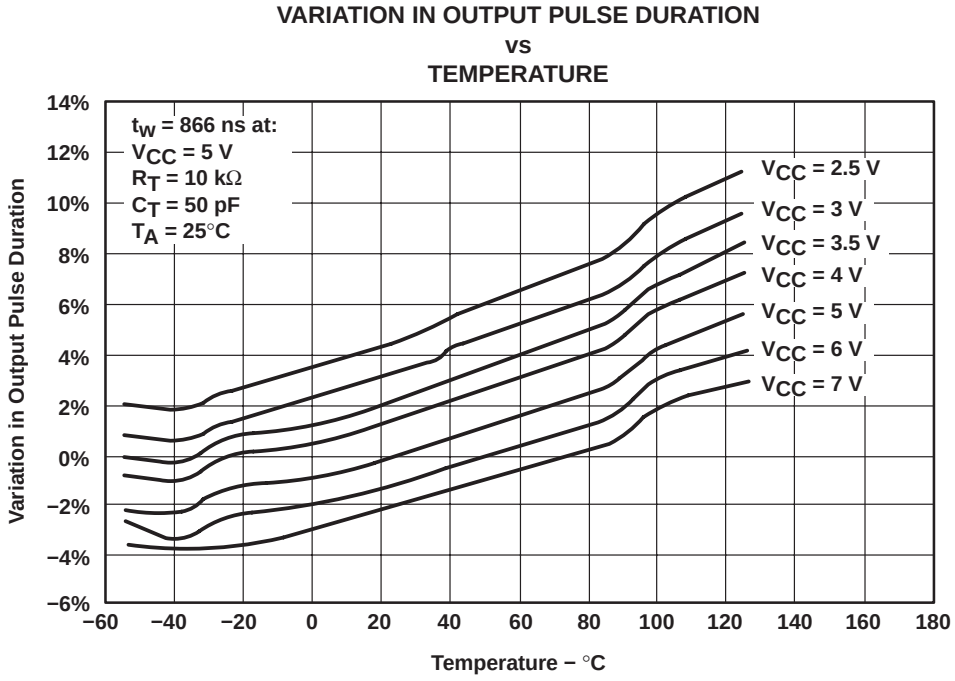



**Figure 5**

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

## APPLICATION INFORMATION†

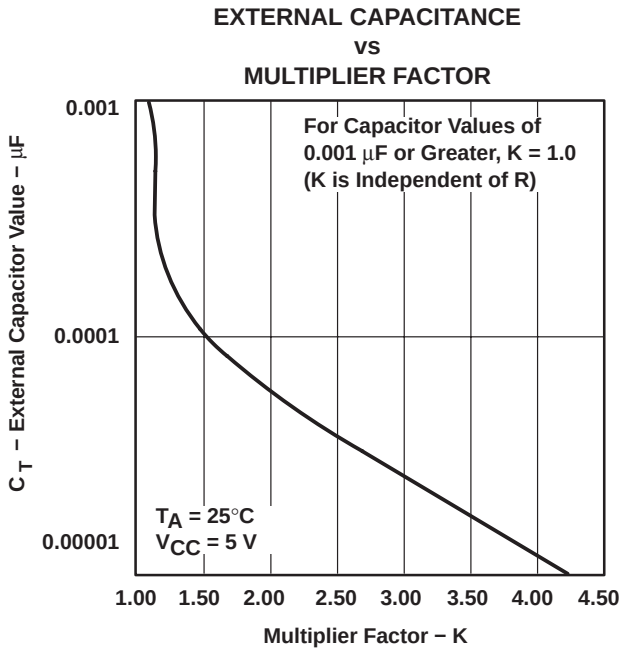



**Figure 6**

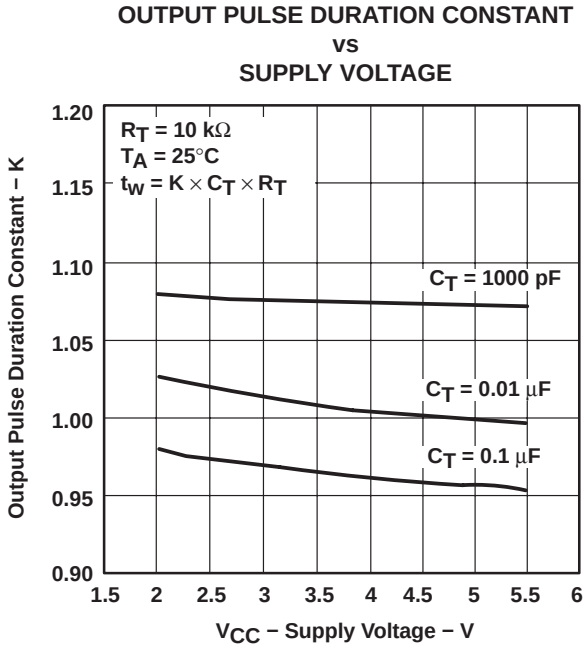



**Figure 7**

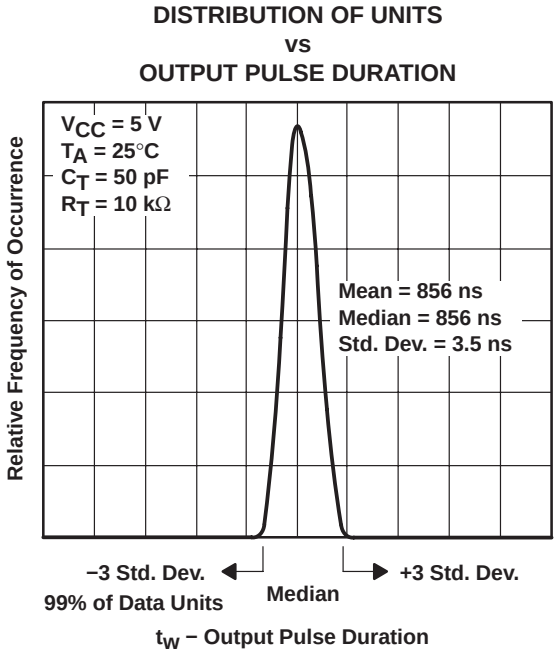



**Figure 8**

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74LV221AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADGVRE4 | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADGVRG4 | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221APWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV221AQPWRG4Q1 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

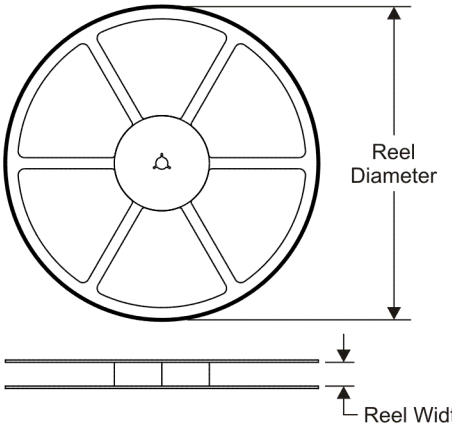
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

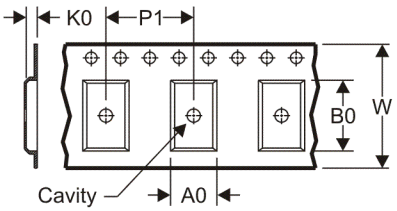
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

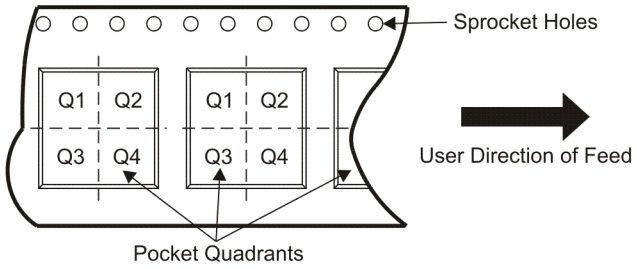



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

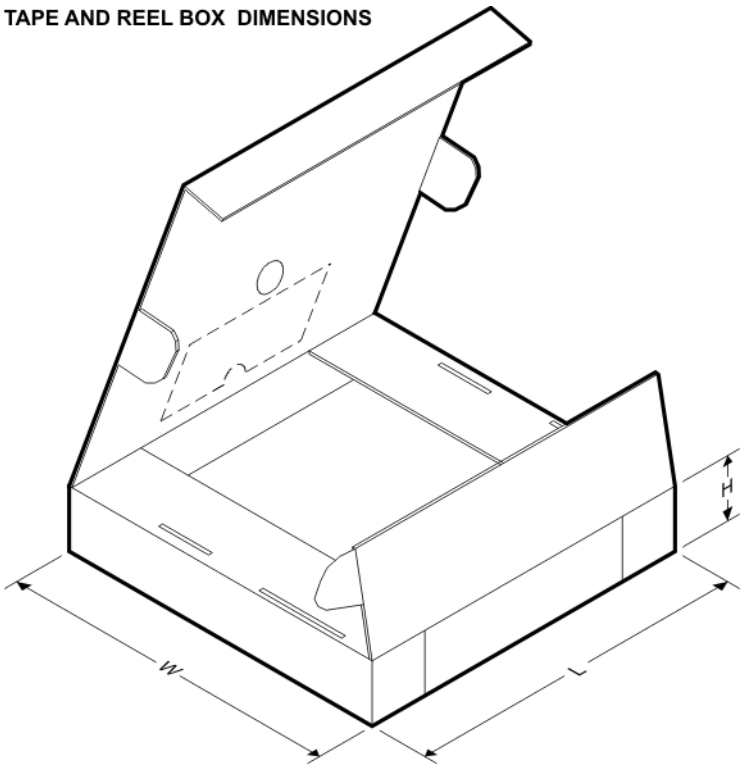
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV221ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV221ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV221ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV221ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV221APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



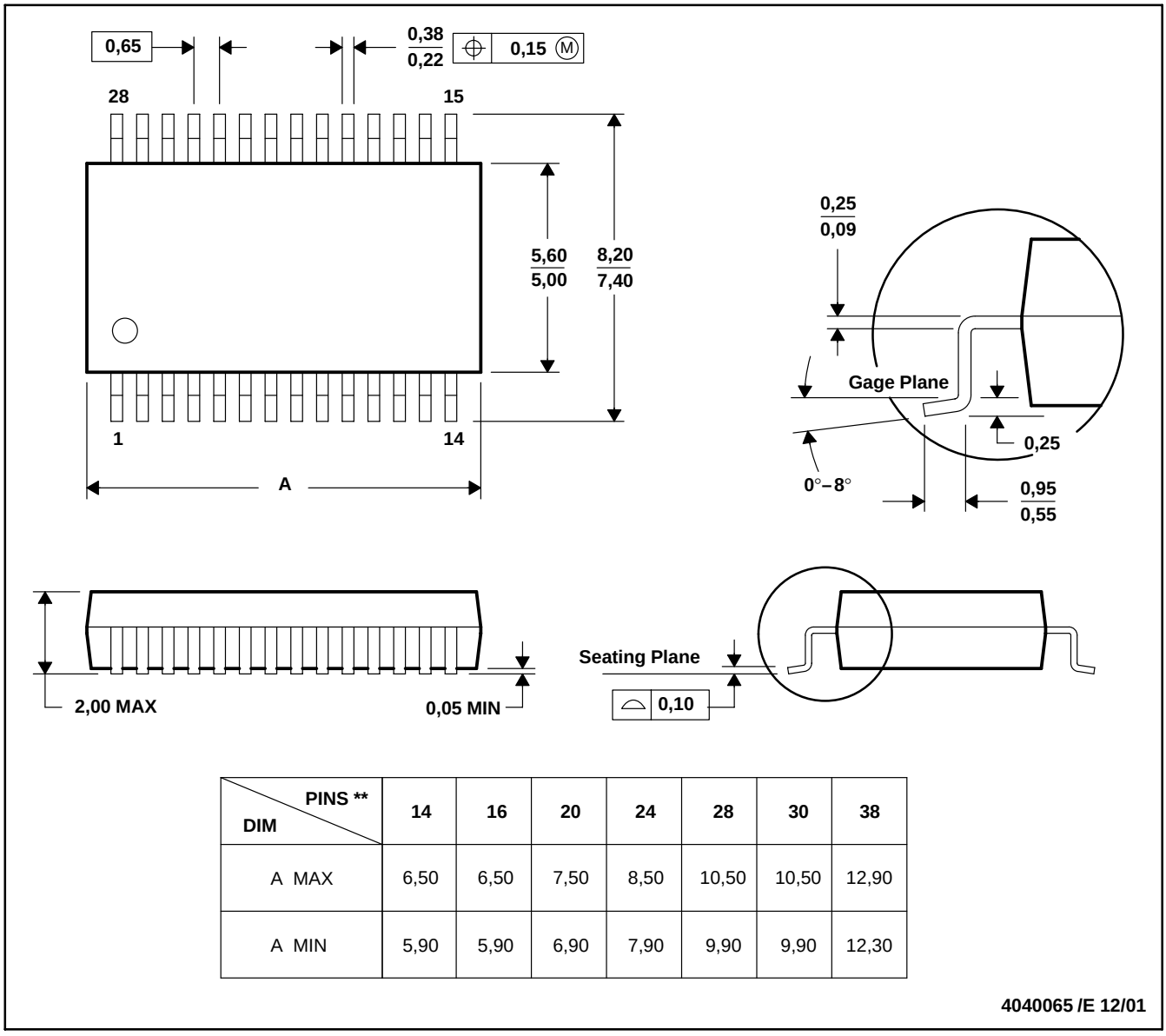

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV221ADBR | SSOP | DB | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LV221ADGVR | TVSOP | DGV | 16 | 2000 | 346.0 | 346.0 | 29.0 |
| SN74LV221ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LV221ANSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LV221APWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

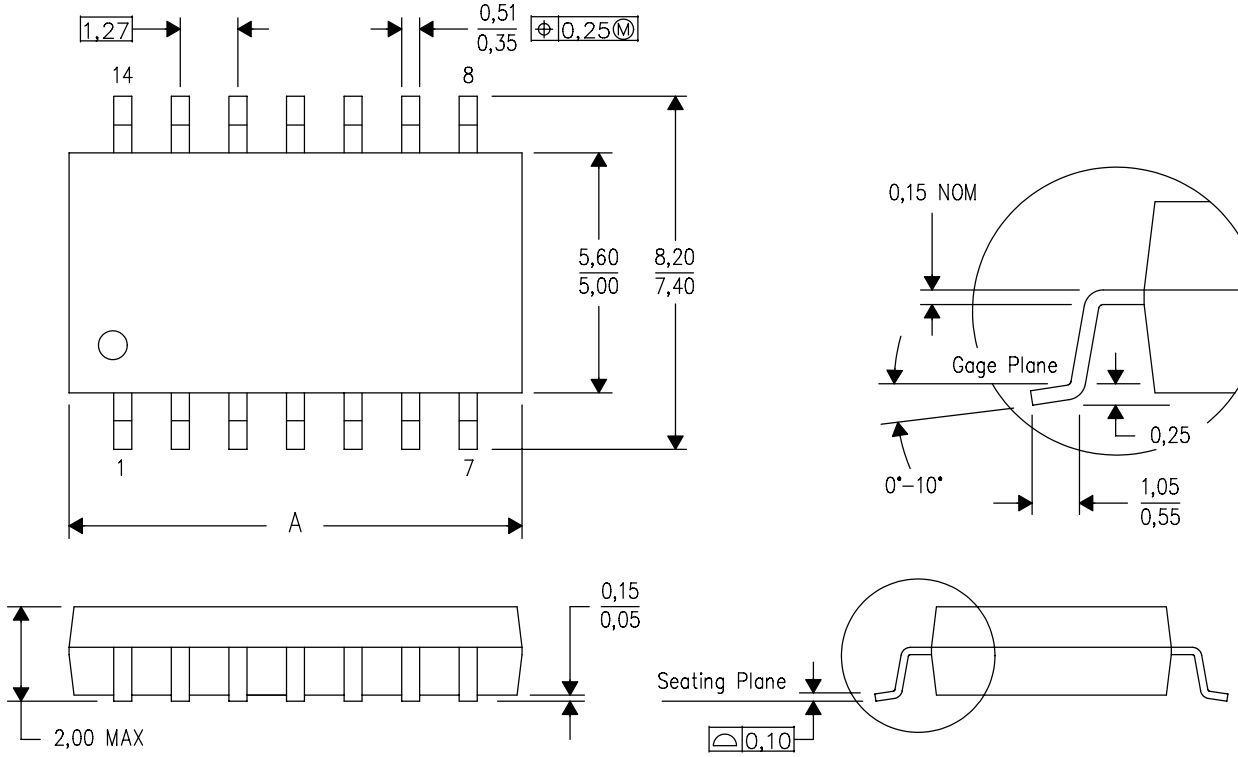
**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



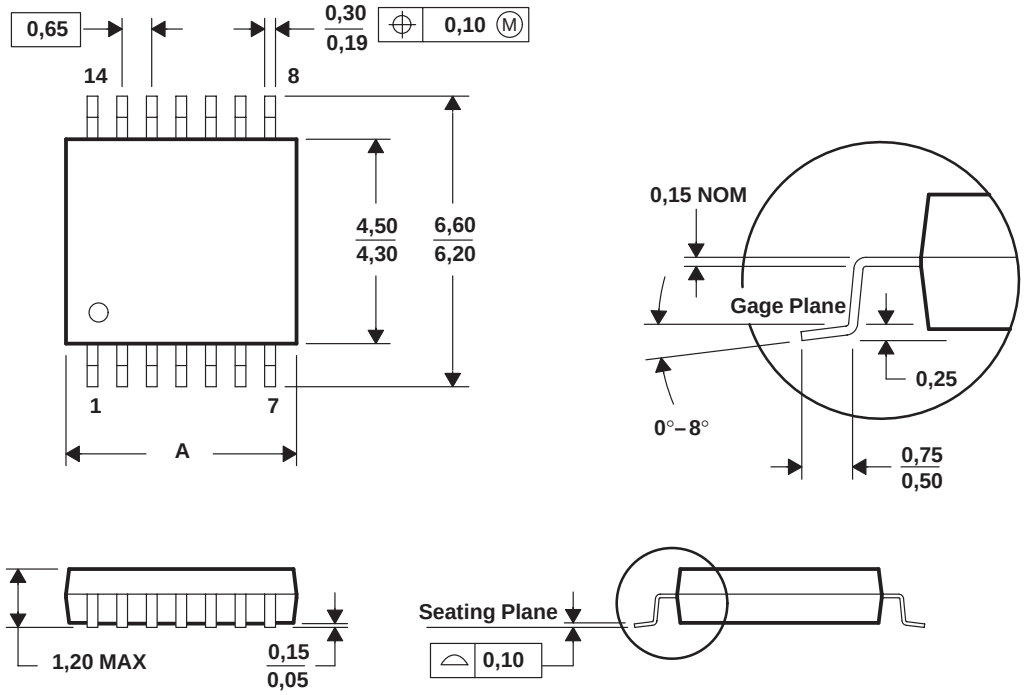

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**



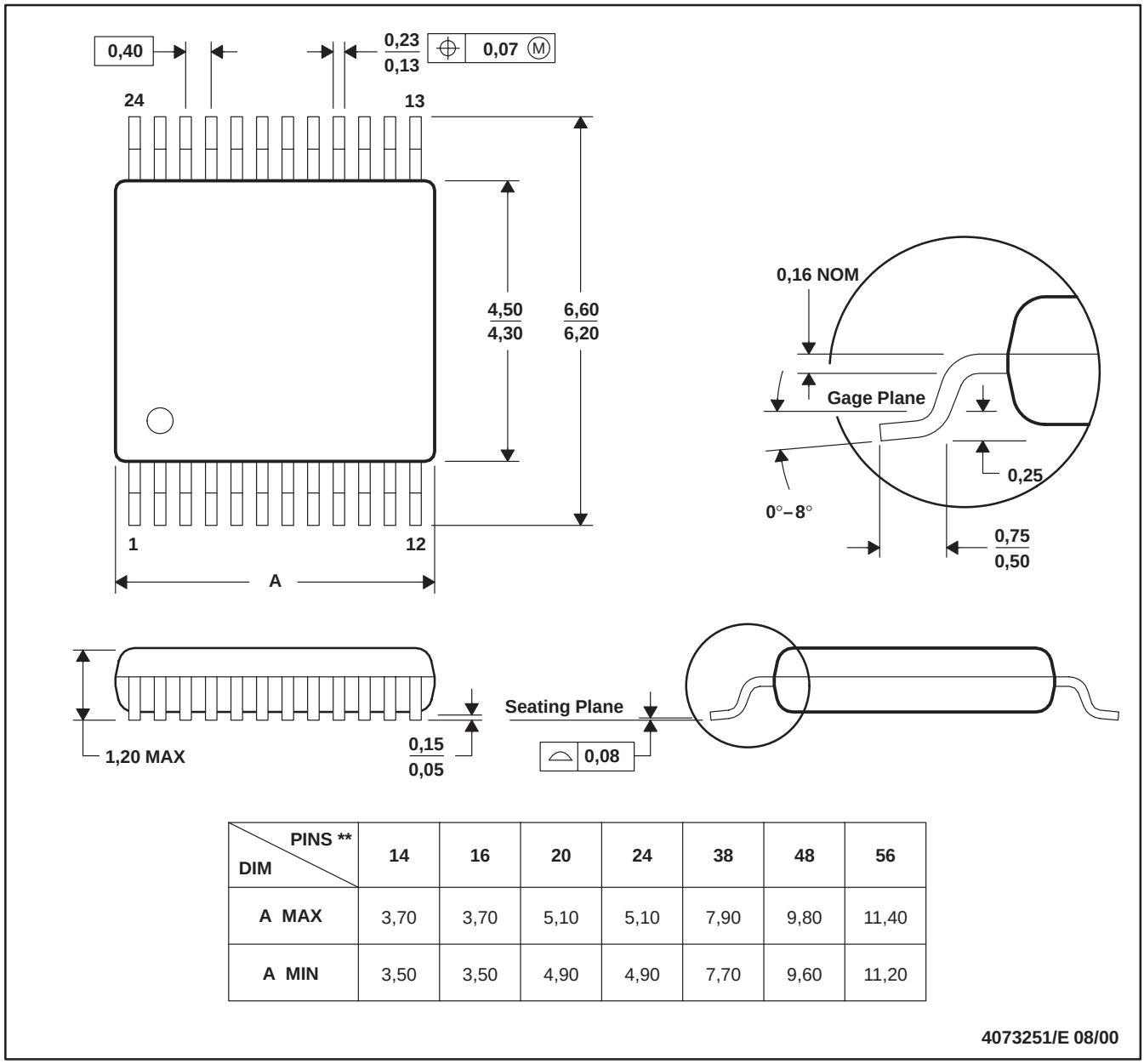

| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

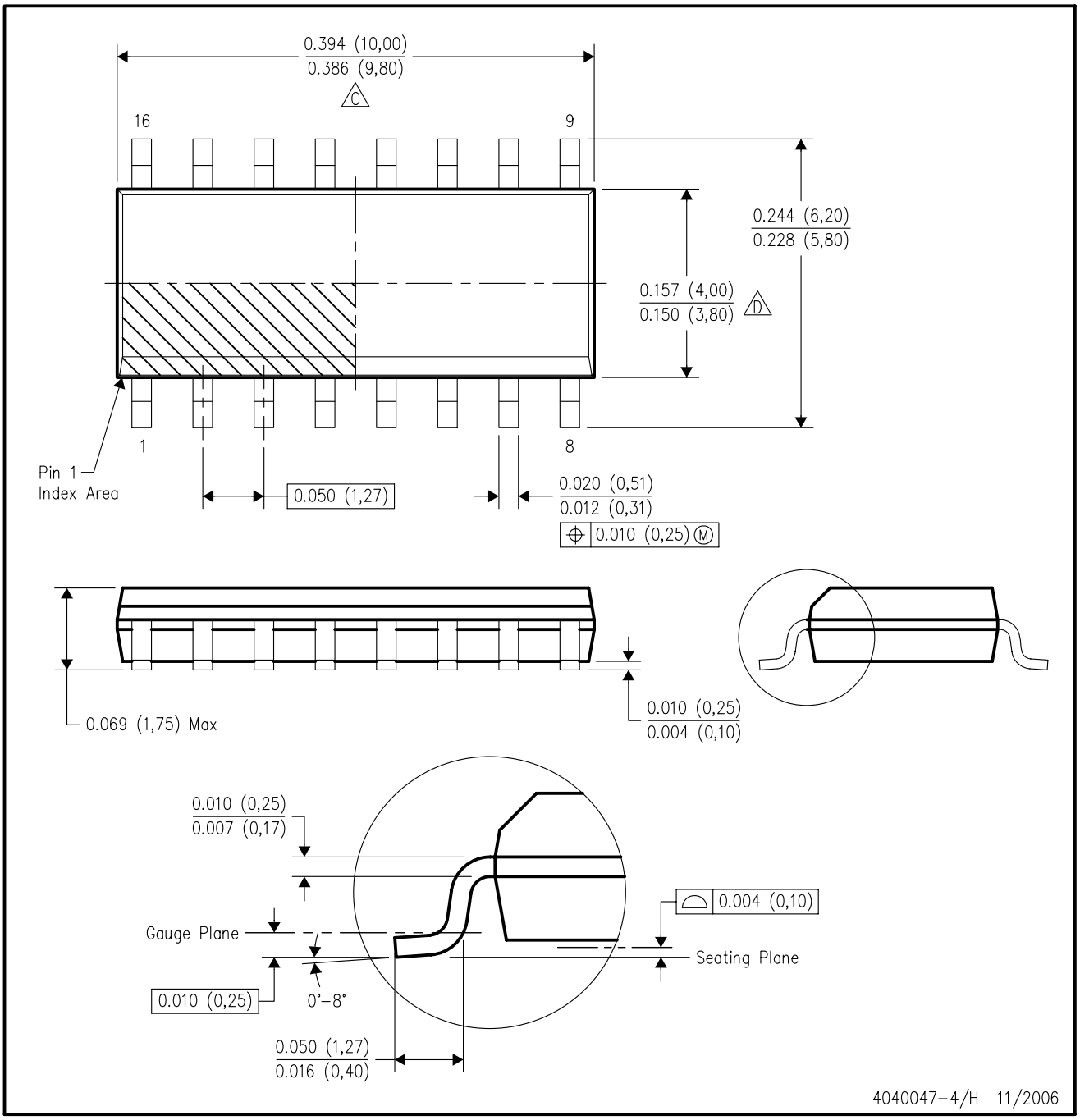



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

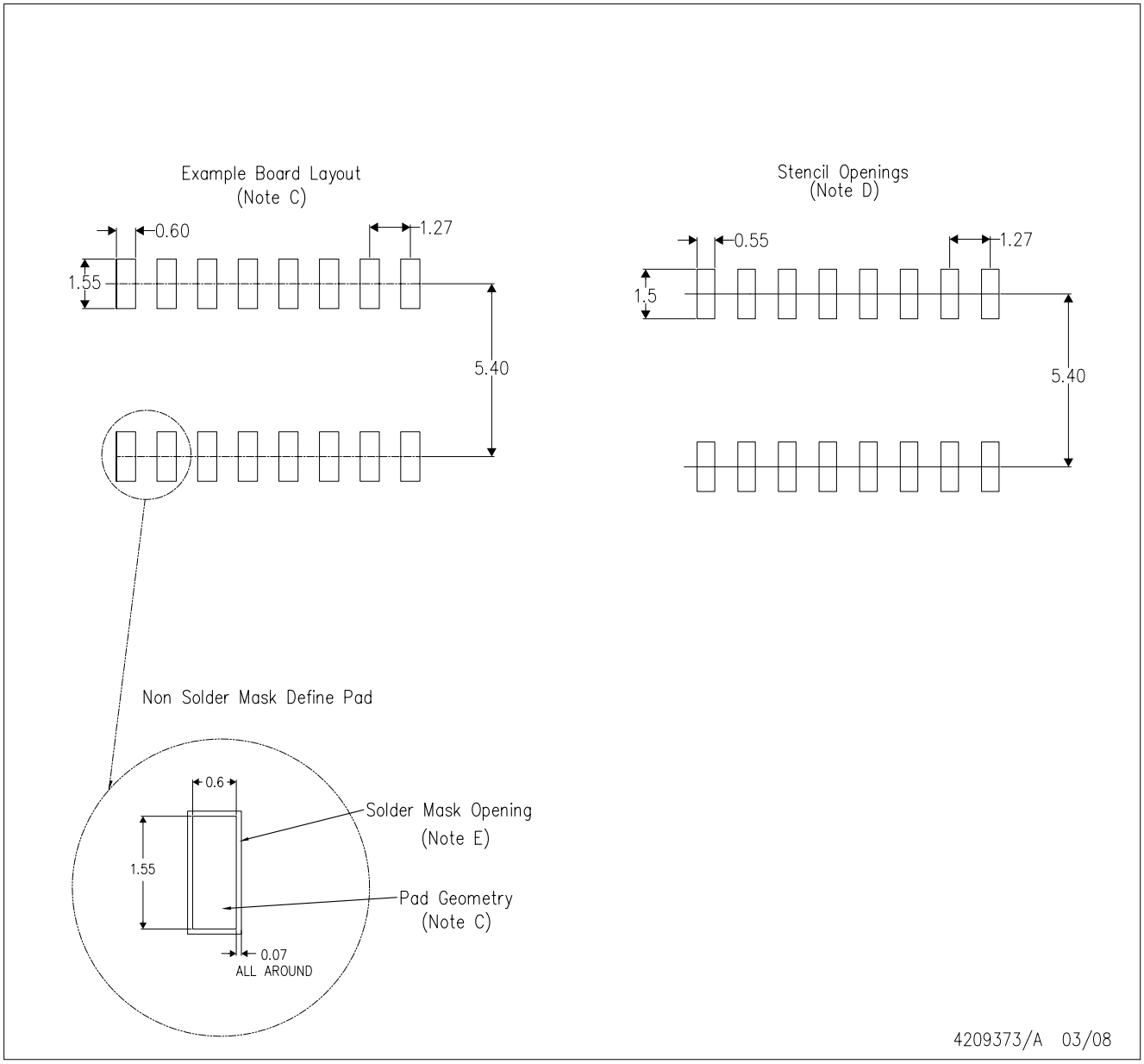
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video & Imaging | www.ti.com/video |
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