To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M62428FP

DIGITAL SOUND CONTROLLER

FEATURES

•Capable of controlling each function by serial data

Electric volume

•Volume level..... 32step (0dB ~ -∞)

•Low noise.....-100dBv(JIS-A)

Bass/Treble.....(0dB,±3dB,1±6dB,±10dB)

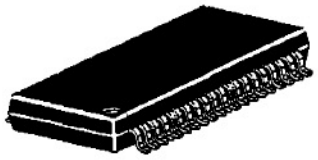
Bass boost.....(ON/OFF)

Surround..... (ON/OFF)

Input selector .....4 - Inputs (A,B,C,D)

MIC mixing

PACKAGE



Outline 42P2R

APPLICATION

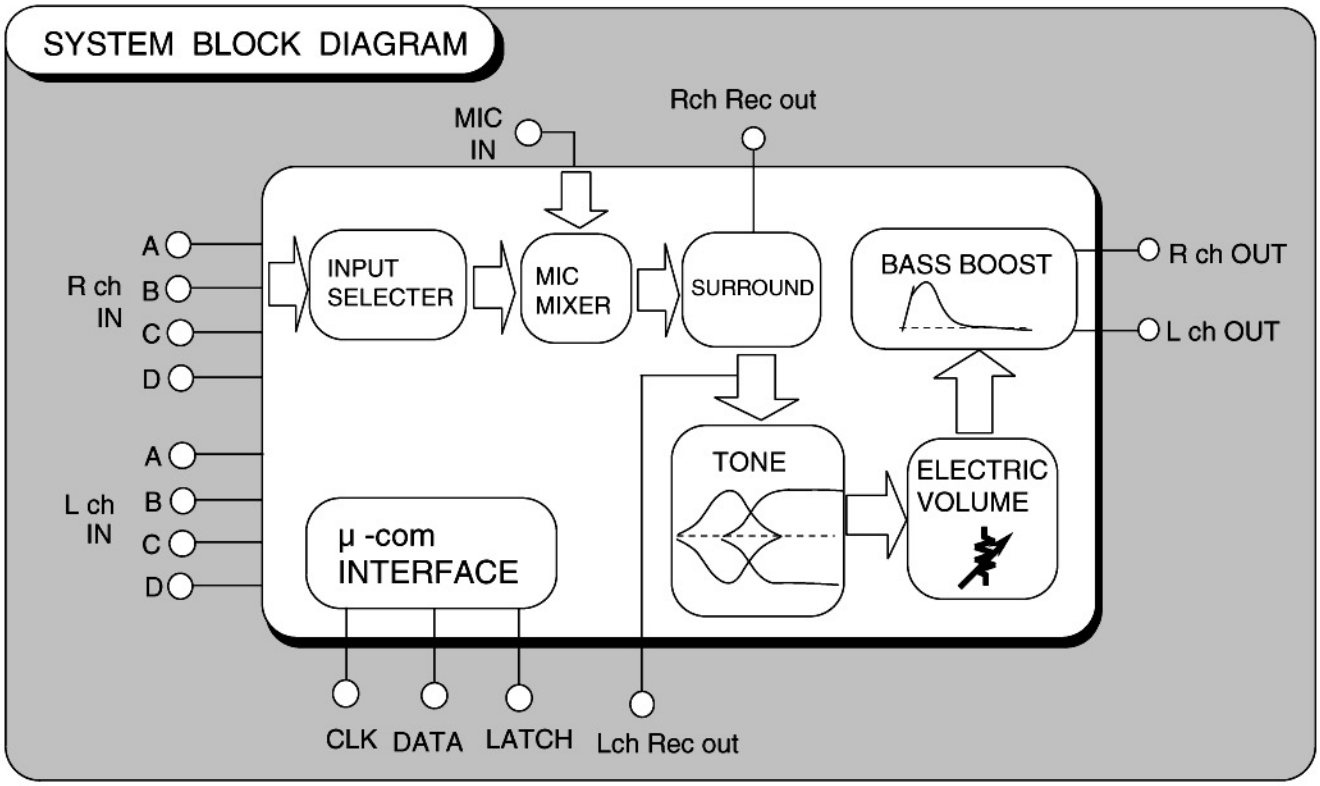
Mini-Stereo,Radio-Cassette tape recorder,TV

RECOMMENDED OPERATING CONDITIONS

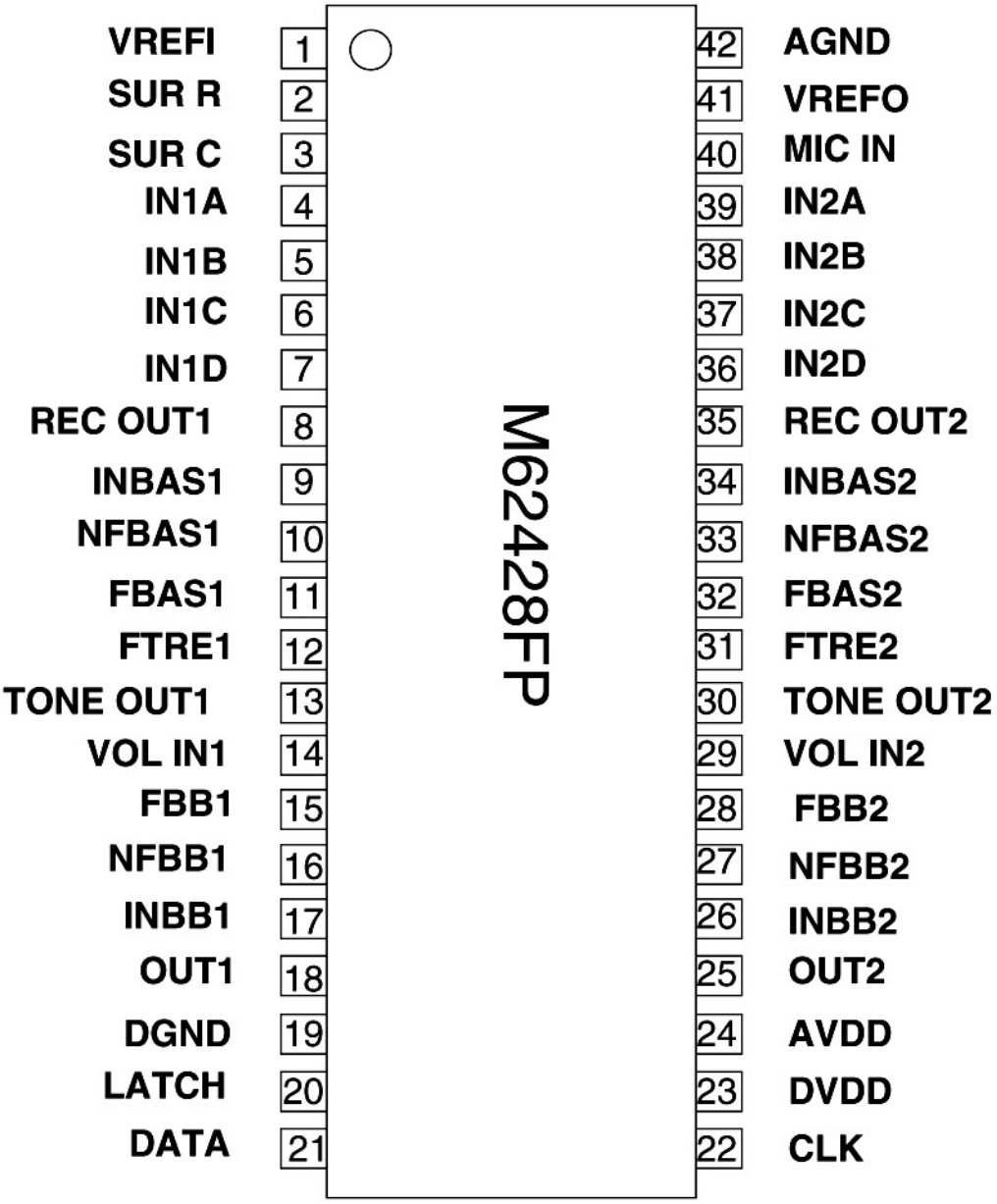
Supply voltage range ..... AVDD:7.0~8.0V DVDD:4.5~5.5V

Rated supply voltage AVDD:7.5V DVDD:5.0V

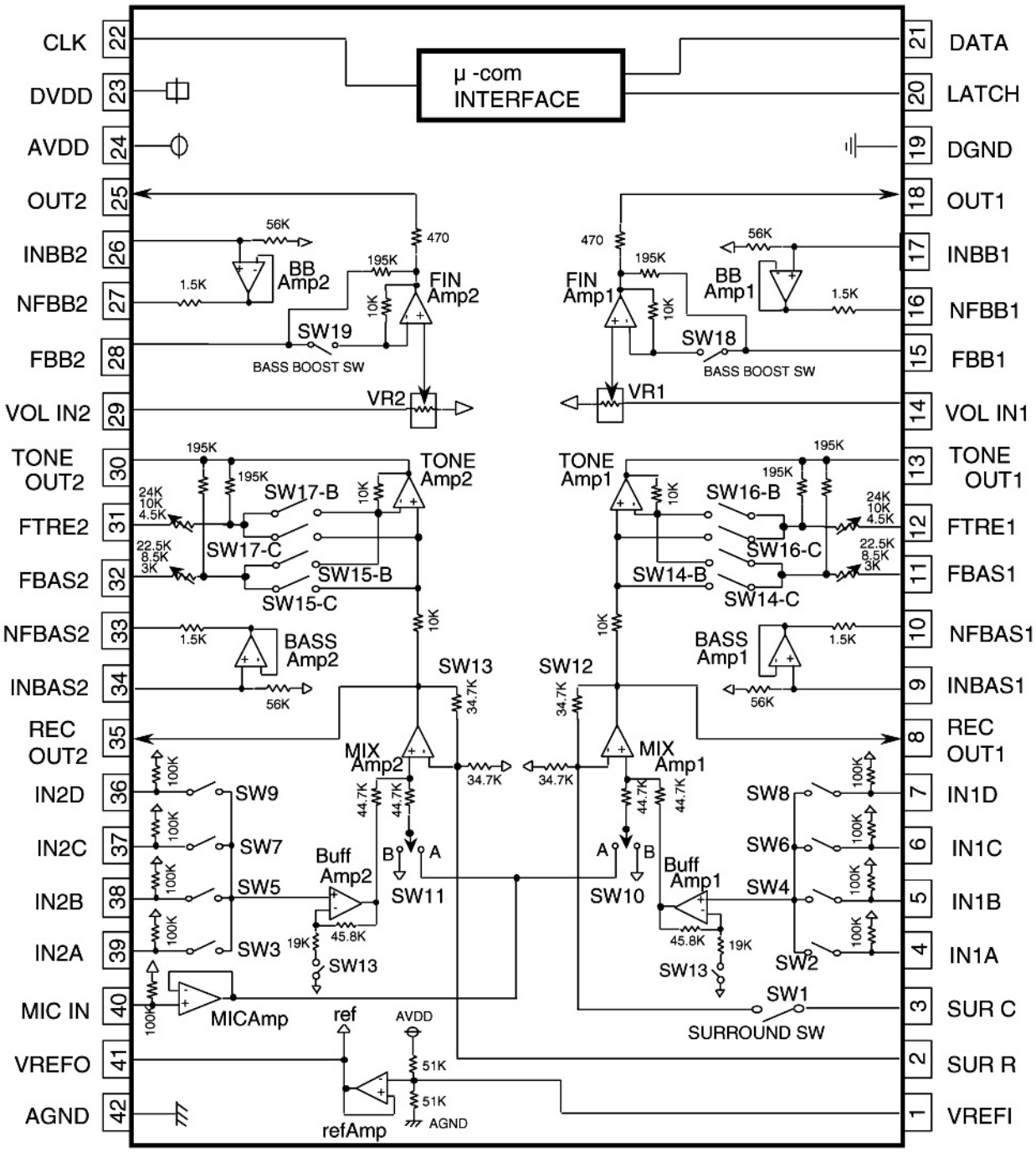
SYSTEM BLOCK DIAGRAM



PIN CONFIGURATION



BLOCK DIAGRAM



Units Resistance :Ω
Capacitance :F

PIN DESCRIPTION

Pin No.	Symbol	Function
1	VREFI	RefAmp input
2	SUR R	External R connection pin for setting time constant for surround
3	SUR C	External C connection pin for setting time constant for surround
4	IN1A	Channel 1 input
5	IN1B	
6	IN1C	
7	IN1D	
8	RECOUT1	REC output of channel 1
9	INBAS1	Input of BASS Amp in bass section
10	NFBAS1	Output of BASS Amp in bass section
11	FBAS1	Resonant impedance (band-pass filter) connection pin for bass section
12	FTRE1	Resonant impedance (band-pass filter) connection pin for treble section
13	TONEOUT1	TONE output of channel 1
14	VOLIN1	R-rudder volume input of channel 1
15	FBB1	Input of bass boosting resonant buffer amp
16	NFBB1	Output of bass boosting resonant buffer amp
17	INBB1	Resonant impedance (band-pass filter) connection pin for bass boost section
18	OUT1	Channel 1 output
19	DGND	Ground of the internal logic circuit
20	LATCH	Input pin of latch signal. Changes the circuit status at the rising edge of the latch signal
21	DATA	Input pin of control data. Reads data at the rising edge of clock

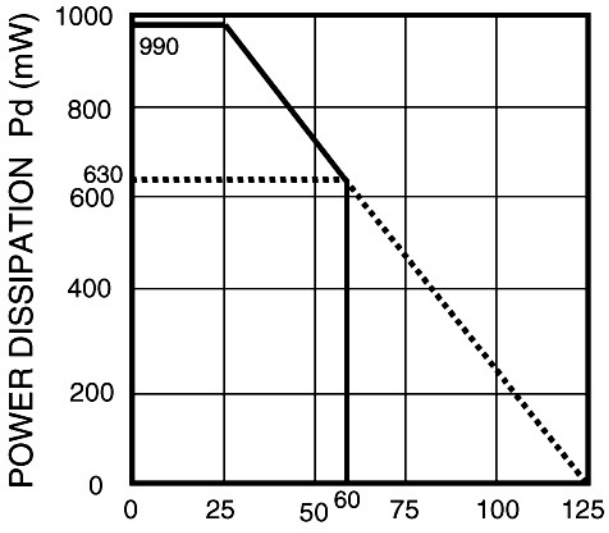
Pin No.	Symbol	Function
22	CLOCK	Clock input pin for serial data transfer
23	DVDD	Power supply of internal logic circuit
24	AVDD	Power supply of internal analog circuit
25	OUT2	Channel 2 output
26	INBB2	Resonant impedance (band-pass filter) connection pin for bass boost section
27	NFBB2	Output of bass boosting resonant buffer amp
28	FBB2	Input of bass boosting resonant buffer amp
29	VOLIN2	R-rudder volume input of channel 2
30	TONEOUT2	TONE output of channel 2
31	FTRE2	Resonant impedance (band-pass filter) connection pin for treble section
32	FBAS2	Resonant impedance (band-pass filter) connection pin for bass section
33	NFBAS2	Output of BASS Amp in bass section
34	INBAS2	Input of BASS Amp in bass section
35	RECOUT2	REC output of channel 2
36	IN2D	Channel 2 input
37	IN2C	
38	IN2B	
39	IN2A	
40	MIC IN	Microphone input
41	VREFO	RefAmp output
42	AGND	Ground of the internal analog circuit

ABSOLUTE MAXIMUM RATINGS

(Ta=25°C,unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
AVdd	Analog supply voltage		9.0	V
DVdd	Digital supply voltage		7.0	V
Pd	Power dissipation	Ta ≤ 25°C	990	mW
K_θ	Thermal derating	Ta > 25°C	9.9	mW/°C
Topr	Operating temperature		-20~+75	°C
Tstg	Storage temperature		-40~+125	°C

THERMAL DERATING
(MAXIMUM RATING)



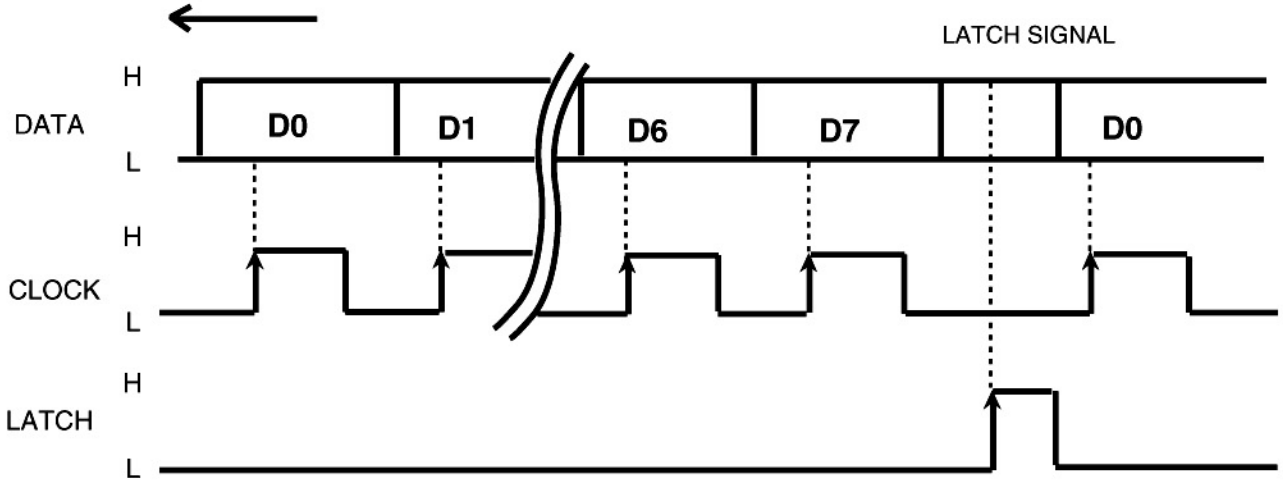
RECOMMENDED OPERATING CONDITIONS

(Ta=25°C,unless otherwise noted)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Analog supply voltage	AVdd	(Note 1)	7.0	7.5	8.0	V
Digital supply voltage	DVdd	(Note 1) DVdd≤AVdd	4.5	5.0	5.5	V
Logic "H" level input voltage	VIH		0.8DVdd	—	Vdd	V
Logic "L" level input voltage	VIL		0	—	0.2DVdd	V

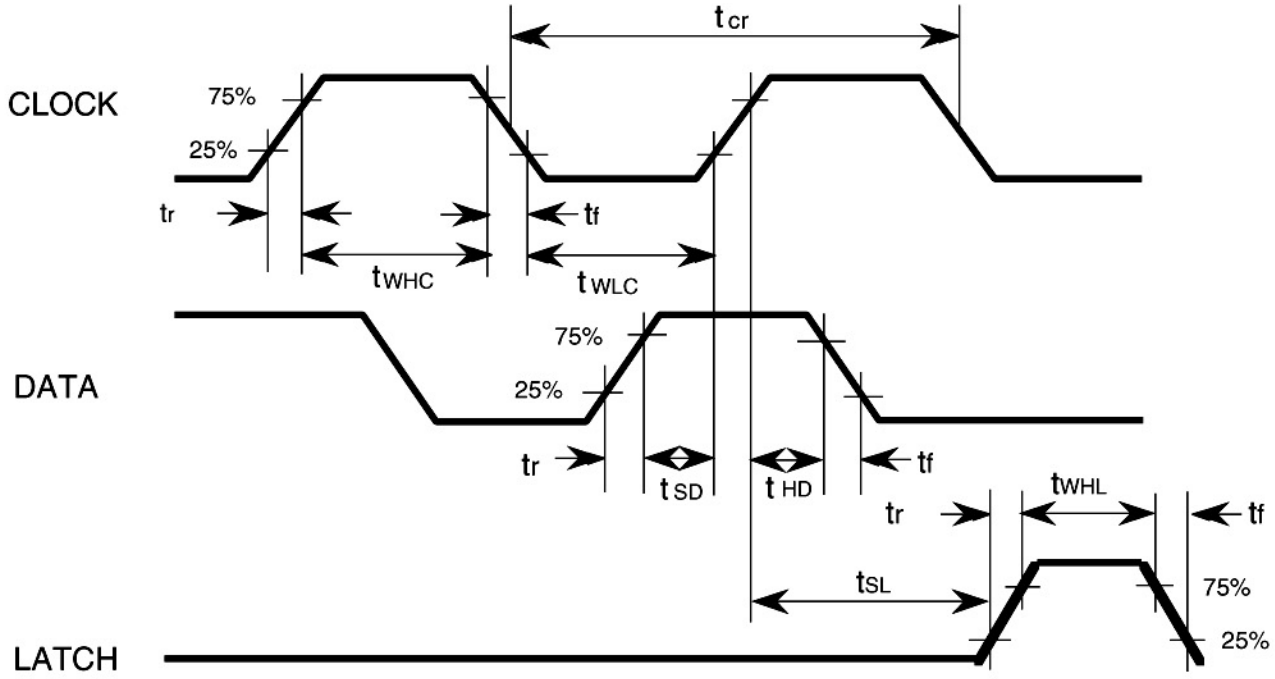
Note 1:After applying AVdd,Apply supply voltages in the order of DVdd for the IC.

RELATIONSHIP BETWEEN DATA AND CLOCK



Data signal is read at the rising edge of clock.
Signal is latched at the rising edge of the latch signal.

CLOCK AND DATA TIMINGS



TIMING DEFINITION OF DIGITAL BLOCK

Symbol	Parameter	Limits			Unit
		Min	typ	Max	
t_{cr}	Clock cycle time	4	–	–	μ sec
t_{WHC}	Clock pulse width ("H" level)	1.6	–	–	
t_{WLC}	Clock pulse width ("L" level)	1.6	–	–	
t_r	Rising time of clock,data and latch	–	–	0.4	
t_f	Falling time of clock,data and latch	–	–	0.4	
t_{SD}	Data setup time	0.8	–	–	
t_{HD}	Data hold time	0.8	–	–	
t_{SL}	Latch setup time	1	–	–	
t_{WHL}	Latch pulse width	1.6	–	–	

DATA INPUT FORMAT

2 types of input formats can be selected by changing the D7 slot setting status.
(Initialize all data of the 2 formats when power is turned on.)

← Input direction

Input format selection slot

(1)

DO1	D11	D21	D31	D41	D51	D61	D7
* Refer to the slot setting code list (3) for master volume					Surround 1 : ON 0 : OFF	MIC MIX 1 : Side A 0 : Side B	0

(2)

DO2	D12	D22	D32	D42	D52	D62	D7
* Refer to the slot setting code list (4) for tone control Bass boost SW18,19 ON/OFF				* Refer to the slot setting code list (5) for Input selector		Through gain +10dB 1 : OFF 0 : ON	1

(3) Setting code (master volume)

Amount of ATT	D01	D11	D21	D31	D41
-0.0dB	0	0	0	0	0
-2.0dB	1	0	0	0	0
-4.0dB	0	1	0	0	0
-6.0dB	1	1	0	0	0
-8.0dB	0	0	1	0	0
-10.0dB	1	0	1	0	0
-12.0dB	0	1	1	0	0
-14.0dB	1	1	1	0	0
-16.0dB	0	0	0	1	0
-18.0dB	1	0	0	1	0
-20.0dB	0	1	0	1	0
-22.0dB	1	1	0	1	0
-24.0dB	0	0	1	1	0
-26.0dB	1	0	1	1	0
-28.0dB	0	1	1	1	0
-30.0dB	1	1	1	1	0
-32.0dB	0	0	0	0	1
-34.0dB	1	0	0	0	1
-36.0dB	0	1	0	0	1
-38.0dB	1	1	0	0	1
-40.0dB	0	0	1	0	1
-42.0dB	1	0	1	0	1
-44.0dB	0	1	1	0	1
-48.0dB	1	1	1	0	1
-52.0dB	0	0	0	1	1
-56.0dB	1	0	0	1	1
-60.0dB	0	1	0	1	1
-64.0dB	1	1	0	1	1
-68.0dB	0	0	1	1	1
-72.0dB	1	0	1	1	1
-76.0dB	0	1	1	1	1
-∞	1	1	1	1	1

(4) Setting code (bass•treble cut / boost and bass boost on / off)

<bass>

		D02	D12	D22	D32
cut	-3 dB	0	0	0	1
	-6 dB	0	0	1	1
	-10 dB	0	1	0	1
	0 dB	0	1	1	1
boost	+3 dB	1	0	0	1
	+6 dB	1	0	1	1
	+10 dB	1	1	0	1

<treble>

		D02	D12	D22	D32
cut	-3 dB	0	0	0	0
	-6 dB	0	0	1	0
	-10 dB	0	1	0	0
	0 dB	0	1	1	0
boost	+3 dB	1	0	0	0
	+6 dB	1	0	1	0
	+10 dB	1	1	0	0

<bass boost ON / OFF>

	D02	D12	D22	D32
bass boost ON	1	1	1	1
bass boost OFF	1	1	1	0

(5) Setting code (input selector)

	D42	D52
IN1A,2A (SW2,3 ON)	0	0
IN1B,2B (SW4,5 ON)	0	1
IN1C,2C (SW6,7 ON)	1	0
IN1D,2D (SW8,9 ON)	1	1

ELECTRICAL CHARACTERISTICS

(Ta=25°C,AVdd=7.5V,DVdd=5.0V ,f=1kHz
Tone control & Bass Boost setting :0dB , unless otherwise noted)

(1)Power Supply

Parameter	Symbol	Conditions	Limits			Unit
			Min	typ	Max	
Analog supply circuit current	AIdd	With AVdd=7.5V, pin 24 current, when no signal is provided	–	40	60	mA
Digital supply circuit current	DIdd	With DVdd=5.0V, pin 23 current, when no signal is provided	-50	0	50	μA

(2)Input/Output

Parameter	Symbol	Conditions		Limits			Unit
				Min	typ	Max	
Input impedance	Rin	Pins 4,5,6,7 and 39,38,37,36,Ta=25°C		50	100	200	KΩ
Maximum output voltage	VOM	(input to pin 4 and 39),(input to pin 5 and 38), (input to pin 6 and 37),(input to pin 7 and 36) Output from pin 18 and 25 ,RL=10KΩ,THD=1%		1.3	1.8	—	Vrms
Output terminal voltage	Vodc	Difference in voltage between pin18,25-pin41, when no signal is provided		-0.1	0	0.1	V
	Vrecdc	Difference in voltage between pin 8,35-pin41, when no signal is provided		-0.1	0	0.1	V
Pass gain	Gv	Vin=0.5Vrms, Pin(4,39),(5,38),(6,37),(7,36)-(18,25) gains		-2.0	0	2.0	dB
Output noise voltage	Vono	JIS-A filter Rg=10KΩ When no signal is provided	Pin18,25	—	3.0	15.0	μ Vrms
	Vrecno		Pin 8,35	—	10.0	20.0	μ Vrms
Total harmonic distortion	THD	Pin 18,25, BW=400~30kHz Vi= 0.3Vrms , RL=10KΩ		—	0.02	0.10	%
	THDrec	Pin 8,35, BW=400~30kHz Vi=0.3Vrms, RL=30KΩ		—	0.02	0.10	%
Channel separation	CS	Vo=0.5Vrms , Rg=0KΩ Between pin 18-25 line ,JIS-A		—	-80	-60	dB
	CSrec	Vo=0.5Vrms , Rg=0KΩ Between pin 8-35 line ,JIS-A		—	-80	-60	dB

(3) MIC AMP characteristics

Parameter	Symbol	Conditions	Limits			Unit
			Min	typ	Max	
Pass gain	GvM	Vin=0.5Vrms,FLAT, Pin 40 -18,25 gains	-2.0	0	2.0	dB
Output noise voltage	VNOM	Pin18,25 ,JIS-A filter ,Rg=10K ,FLAT When no signal is provided	-	3.0	15.0	μ Vrms
Total harmonic distortion	THDM	Input to pin 40, output from pin18,25, BW=400~30kHz Vi=0.3Vrms , RL=10KΩ	-	0.02	0.1	%

(4) Tone control characteristics

Parameter	Symbol	Conditions			Limits			Unit
					Min	typ	Max	
Tone control voltage gain(bass)	Gbboost	10dB	f=150Hz	(input to pin 4 and 39), (input to pin 5 and 38), (input to pin 6 and 37), (input to pin 7 and 36), output from pin 13 and 30	7	10	13	dB
	Gbcut	-10dB			-13	-10	-7	dB
Tone control voltage gain(treble)	Gtboost	10dB	f=10kHz		7	10	13	dB
	Gtcut	-10dB			-13	-10	-7	dB

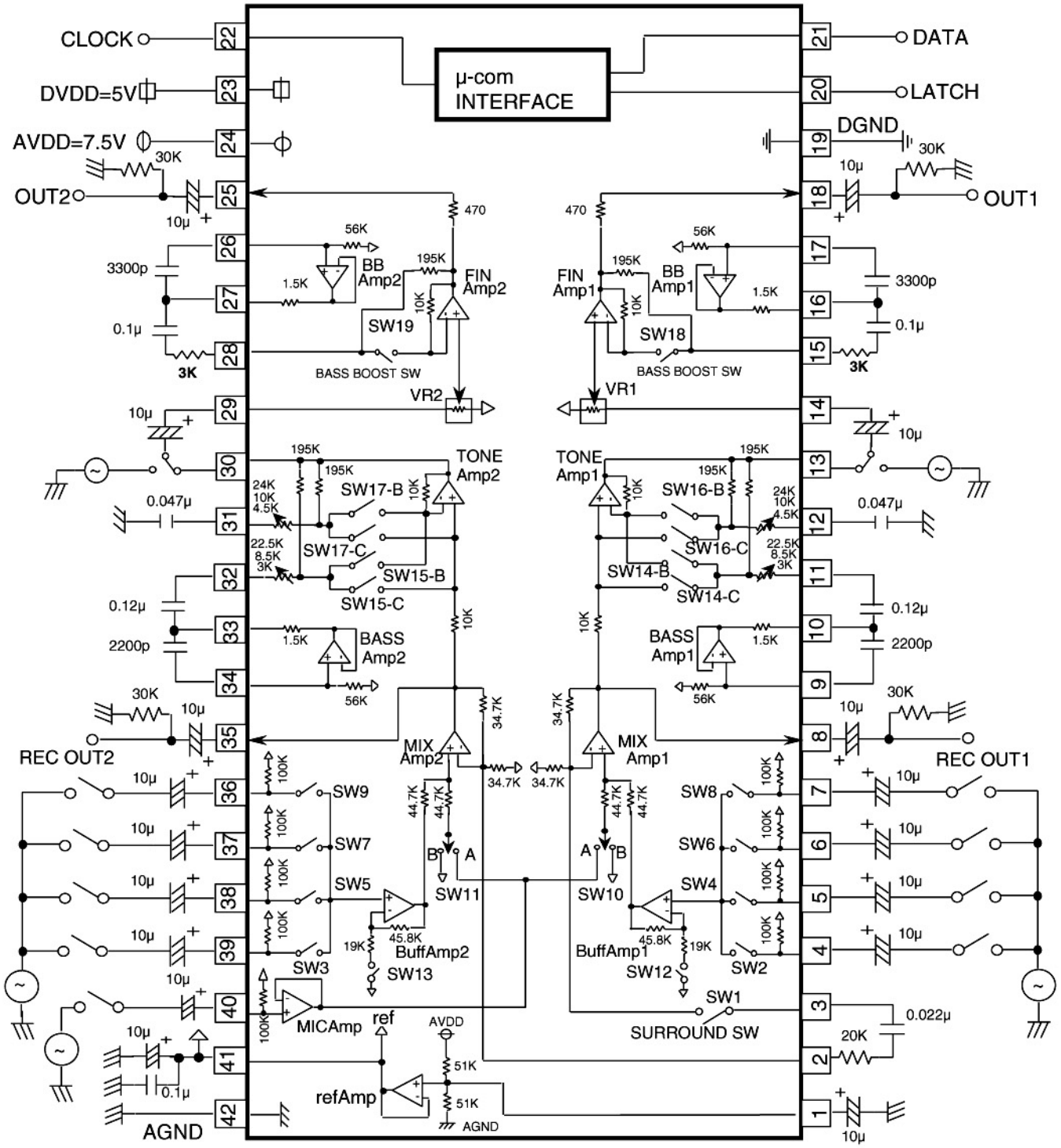
(5) Bass boost characteristics

Parameter	Symbol	Conditions	Limits			Unit
			Min	typ	Max	
Bass boost voltage gain	Gboost	Input to pin 14 and 29 , output from pin 13 and 30 f=100Hz	7	10	13	dB

(6) Volume characteristics

Parameter	Symbol	Conditions	Limits			Unit
			Min	typ	Max	
Maximum attenuation	ATTmav	Input to pins 14 and 29 , output from pin 18 and 25 f=1kHz ,JIS-A filter ,ATT=-∞	-	-83	-75	dB

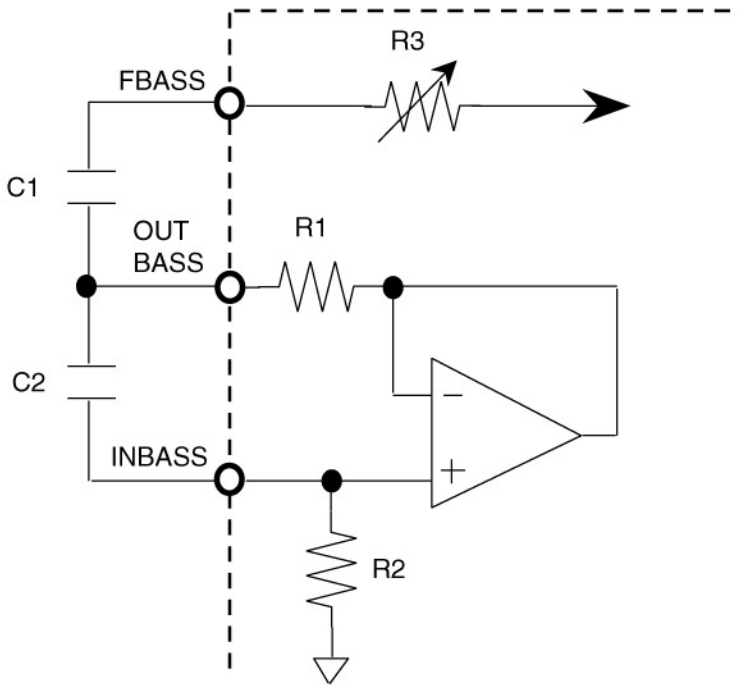
TEST CIRCUIT



Units Resistance :Ω
Capacitance :F

FUNCTION DESCRIPTION

(1) Tone controller equivalent circuit



CENTER FREQUENCY

$f0 = 1 / 2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}$ [Hz]

$Q = \sqrt{(C2 \cdot R2)/(C1 \cdot R1)}$

EXAMPLE : BASS BAND (f=150Hz)
R1=1.5KΩ , R2=56KΩ
C1=0.82μ, C2=0.015μ

Fig.1 A circuit equivalent to the inside of the tone controller

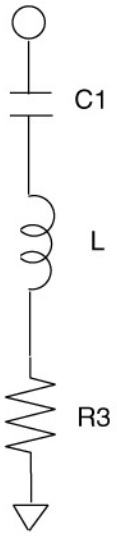
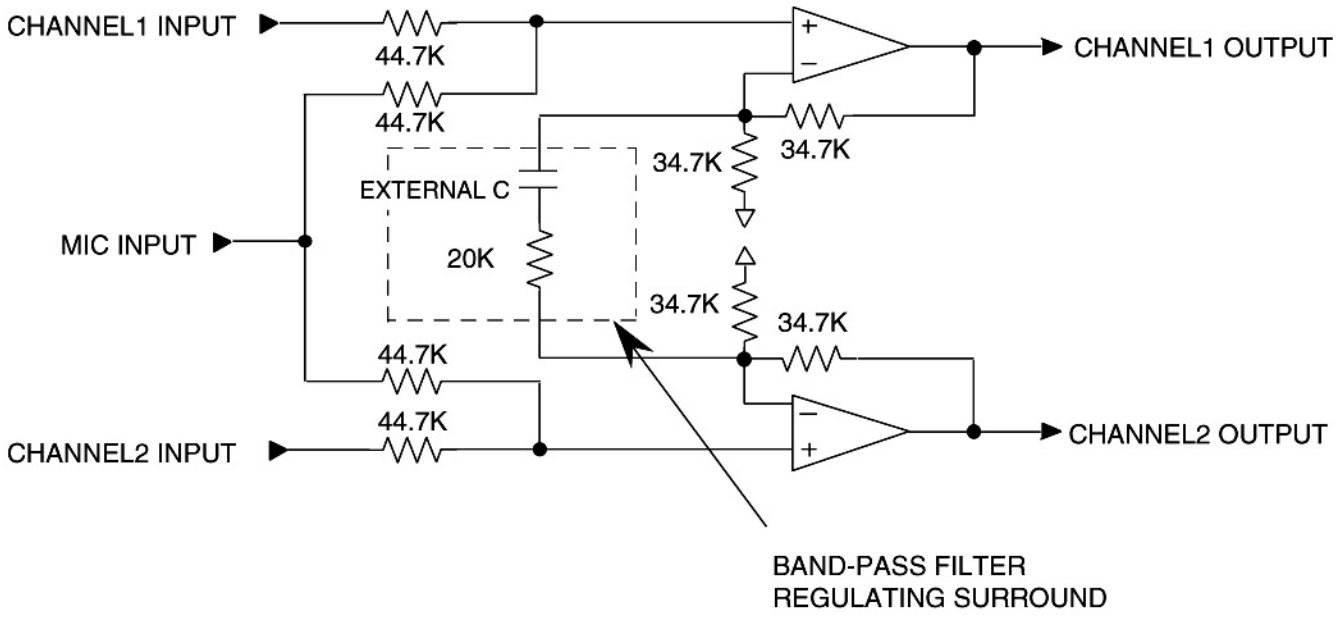


Fig.2 is equivalent to Fig.1. To convert component constants, the equation below is used.

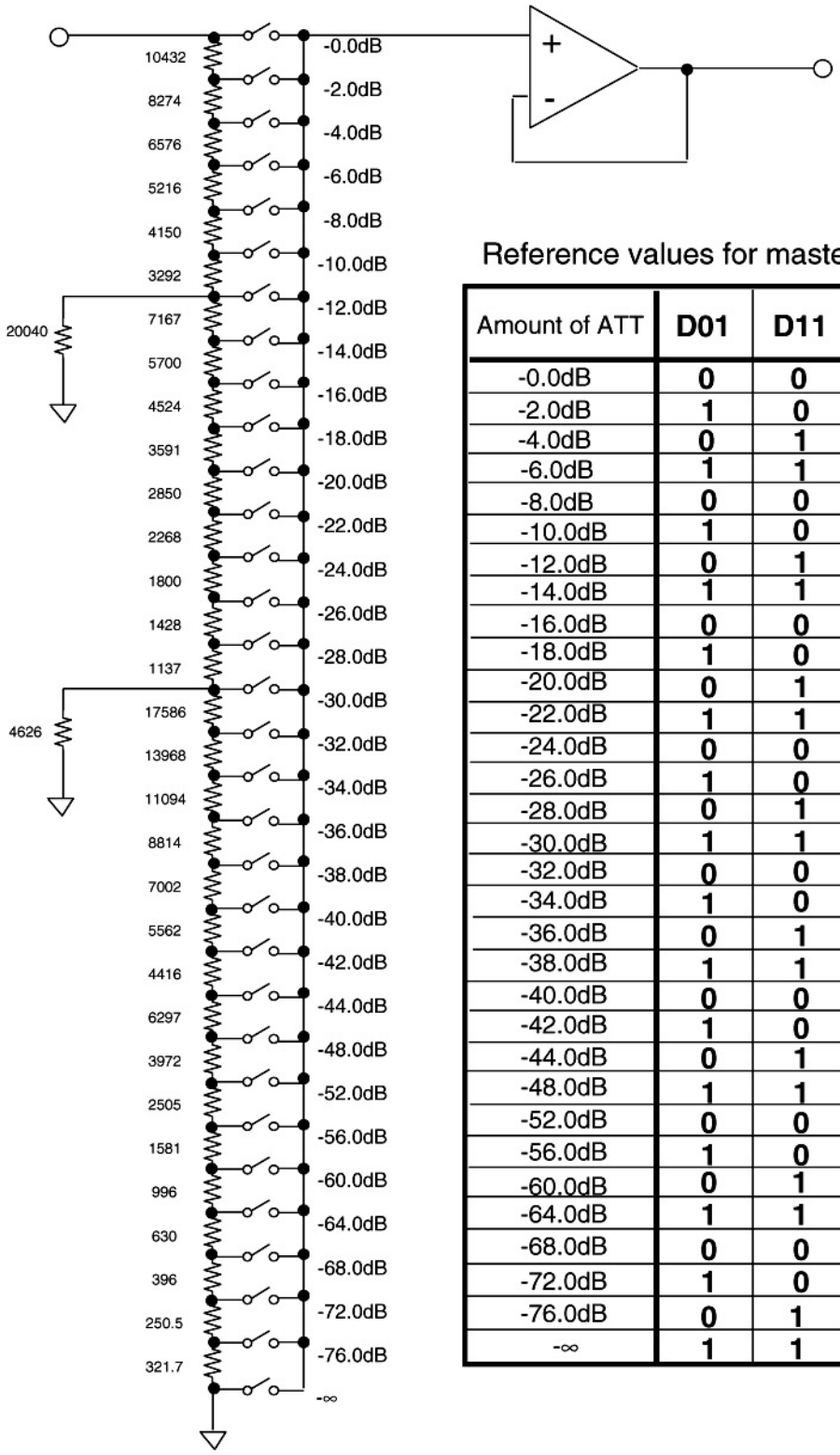
$L = C2 \cdot R1 \cdot R2$

Fig.2 An equivalent circuit using L

(2) Surround block equivalent circuit



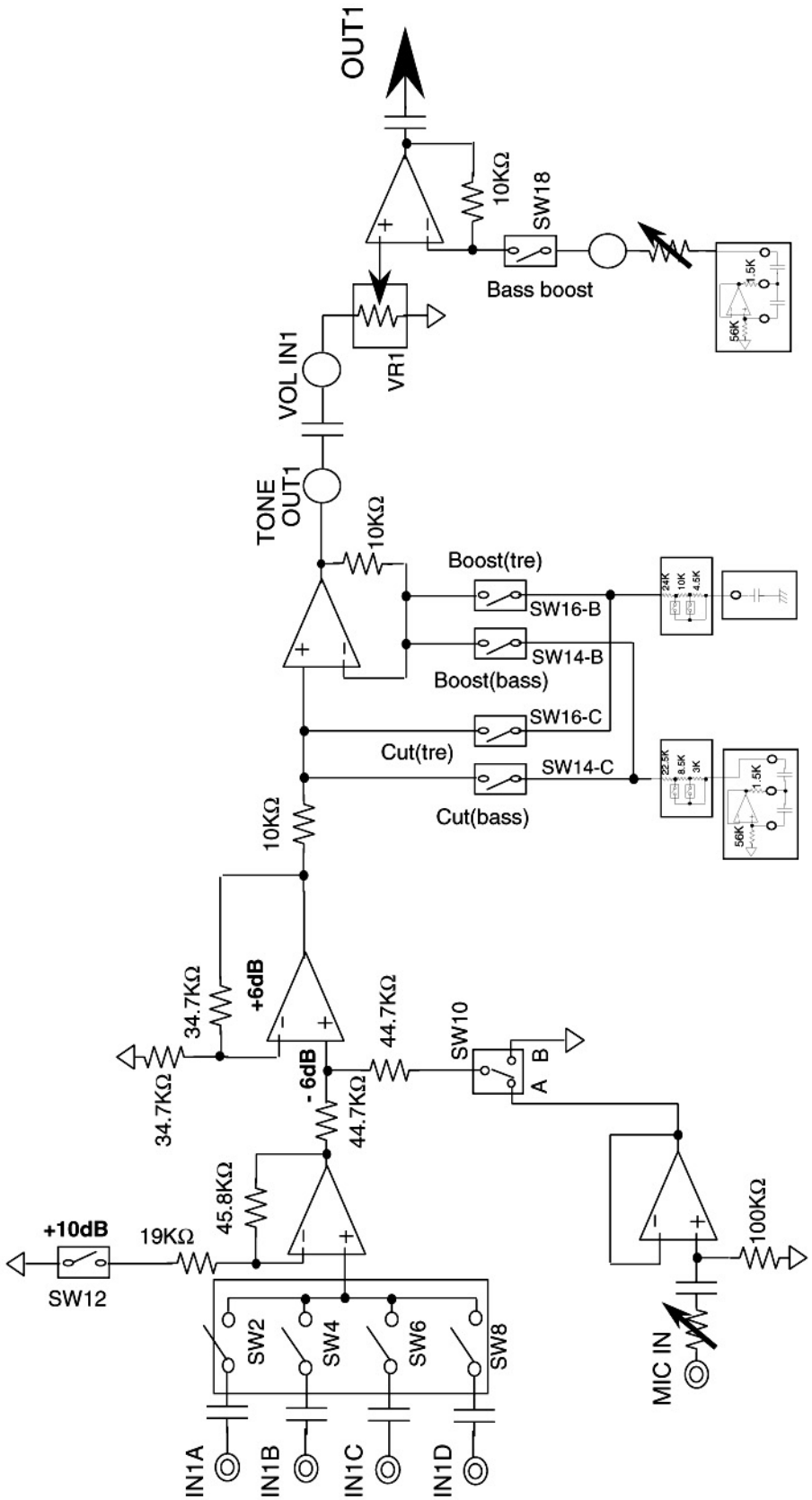
MASTER VOLUME EQUIVALENT CIRCUIT



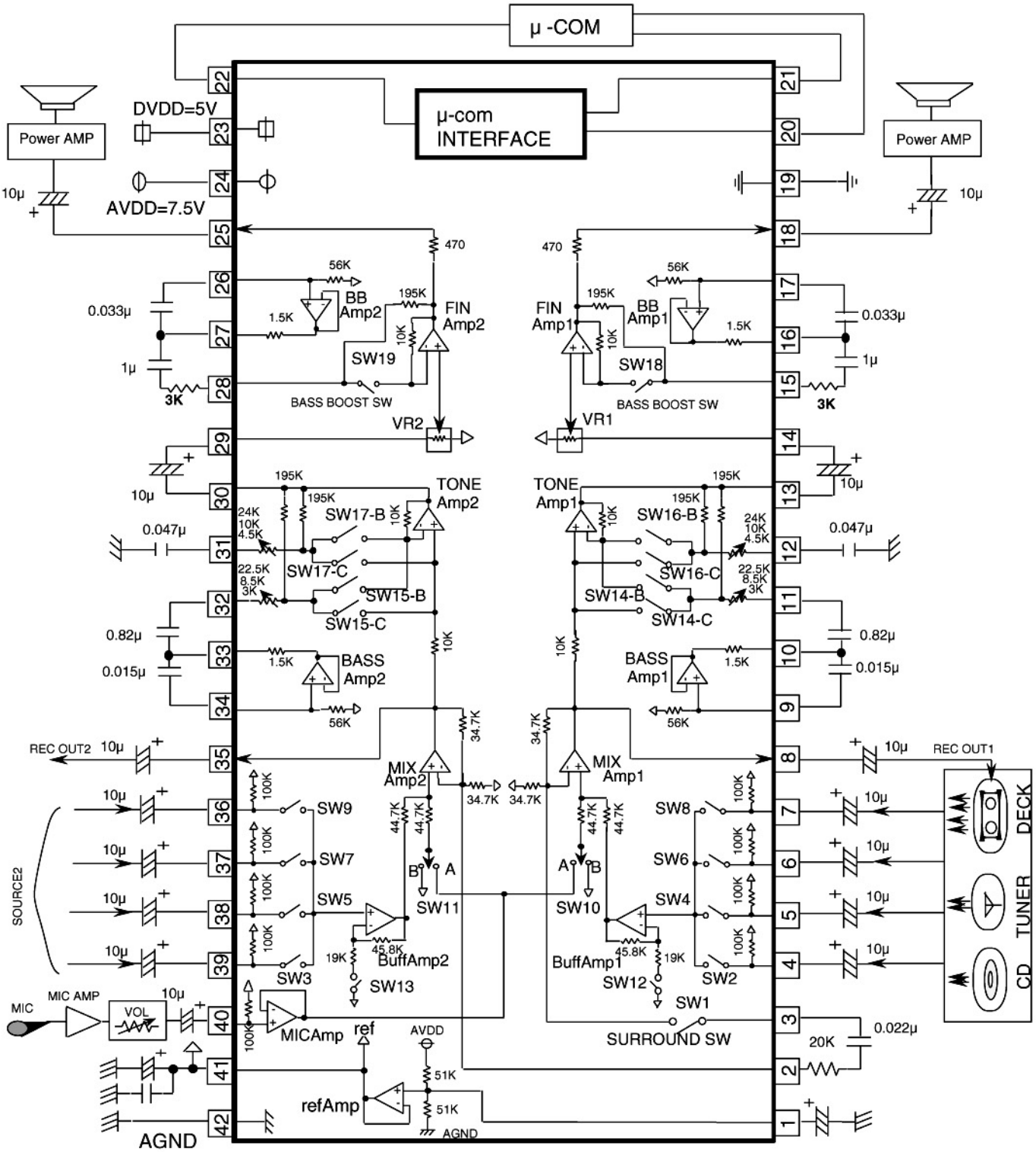
Reference values for mastervolume attenuation

Amount of ATT	D01	D11	D21	D31	D41
-0.0dB	0	0	0	0	0
-2.0dB	1	0	0	0	0
-4.0dB	0	1	0	0	0
-6.0dB	1	1	0	0	0
-8.0dB	0	0	1	0	0
-10.0dB	1	0	1	0	0
-12.0dB	0	1	1	0	0
-14.0dB	1	1	1	0	0
-16.0dB	0	0	0	1	0
-18.0dB	1	0	0	1	0
-20.0dB	0	1	0	1	0
-22.0dB	1	1	0	1	0
-24.0dB	0	0	1	1	0
-26.0dB	1	0	1	1	0
-28.0dB	0	1	1	1	0
-30.0dB	1	1	1	1	0
-32.0dB	0	0	0	0	1
-34.0dB	1	0	0	0	1
-36.0dB	0	1	0	0	1
-38.0dB	1	1	0	0	1
-40.0dB	0	0	1	0	1
-42.0dB	1	0	1	0	1
-44.0dB	0	1	1	0	1
-48.0dB	1	1	1	0	1
-52.0dB	0	0	0	1	1
-56.0dB	1	0	0	1	1
-60.0dB	0	1	0	1	1
-64.0dB	1	1	0	1	1
-68.0dB	0	0	1	1	1
-72.0dB	1	0	1	1	1
-76.0dB	0	1	1	1	1
-∞	1	1	1	1	1

SIGNAL TRANSMISSION BLOCK DIAGRAM



APPLICATION EXAMPLE



Units Resistance :Ω
Capacitance :F