12V MOSFET Drivers with Output Disable for Multiple Phase Synchronous-Rectified Buck Converter

General Description

The uP1951 is a quad, high voltage MOSFET driver optimized for driving four N-Channel MOSFETs in a dual synchronous-rectified buck converter. Each driver is capable of driving a 5000pF load with 30ns transition time. This device combined with uPI multi-phase buck PWM controller forms a complete core voltage regulator for advanced micro-processors.

The uP1951 features adaptive anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintaining minimum deadtime for optimized efficiency.

Both gate drives are turned off by pulling low OD# pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdowns.

Other feature is supply input under voltage lockout. The uP1951 is available in thermal enhanced WQFN3x3-16L package.

Features

- All-In-One Synchronous Buck Drivers
- Bootstrapped High-Side Driver
- Adaptive Anti-Shoot-Through Protection Circuitry
- Tri-State Input for Bridge Shutdown
- Output Disable Control Turns Off both MOSFETs
- Under Voltage Lockout for Supply Input
- WQFN3x3-16L Package
- RoHS Compliant and Halogen Free

Applications

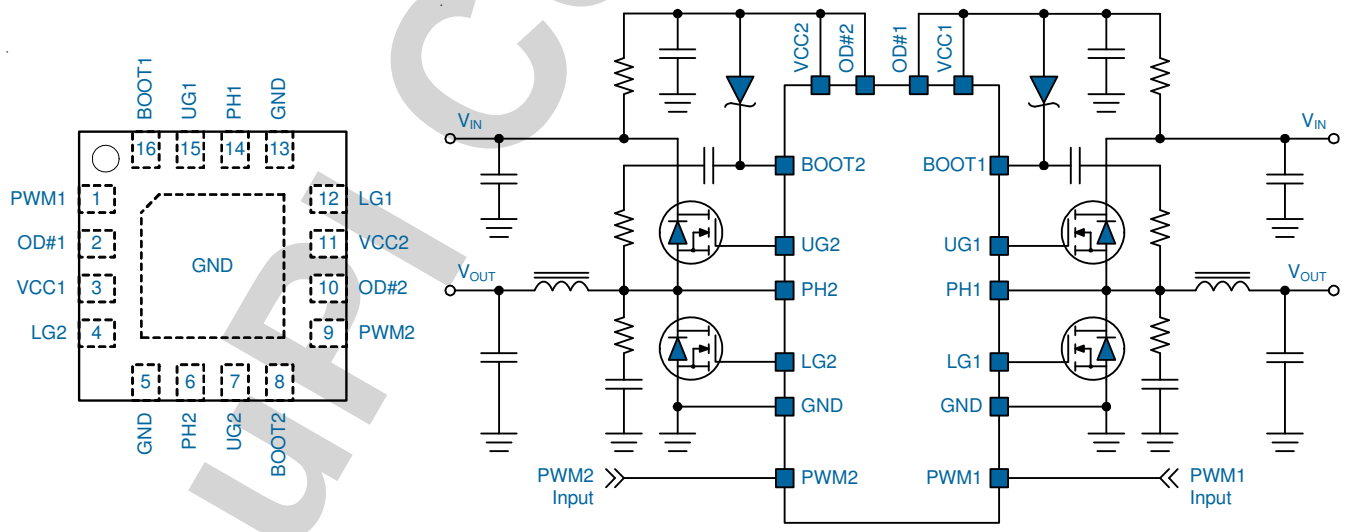
- Core Voltage Supplies for Desktop, Motherboard CPUs
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters

Ordering Information

Order Number	Package Type	Top Marking
uP1951PQDD	WQFN3x3-16L	uP1951P

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

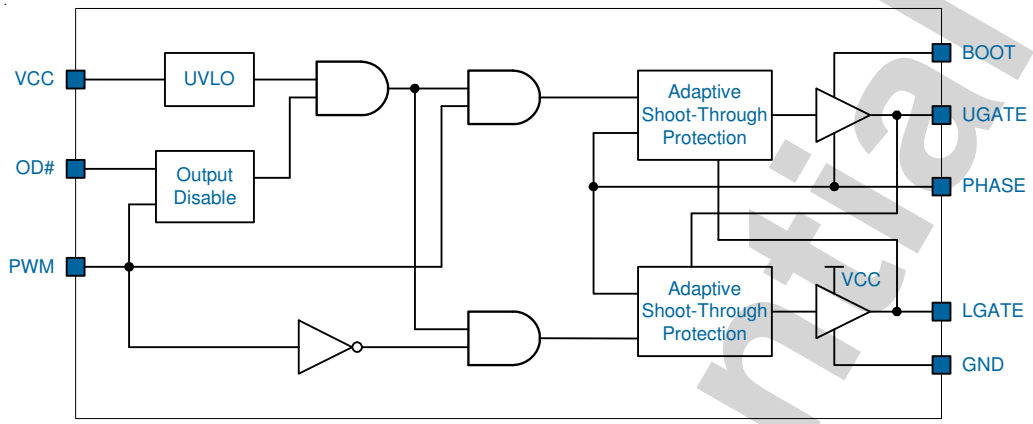
Pin Configuration & Typical Application Circuit



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Functional Block Diagram

1/2 of uP1951



Functional Pin Description

Pin Name	Pin Function
BOOTx	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOTx pin and the PHx pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC.
PWMx	**PWM Input.** This pin receives logic level input and controls the driver outputs.
OD#x	**Output Disable.** This pin disables normal operation and forces both UGx and LGx off when it is pulled low.
VCCx	**Supply Voltage for the IC.** This pin provides bias voltage for the IC. Connect these pins to 12V voltage source and bypass it with an R/C filter. Note that VCC1 and VCC2 are two independent pins, and they are NOT internally connected together. Therefore user must connect both VCC1 and VCC2 to 12V voltage source to supply power if both of the two output channels are used.
LGx	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
GND	**Ground for the IC.** All voltages levels are measured with respect to this pin.
PHx	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGx driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
UGx	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
Exposed Pad	**Ground for the IC.** The exposed pad should be well soldered to PCB for effective heat conduction.

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Functional Description

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The uP1951 features adaptive anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

Both gate drives are turned off by pulling low OD# pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdowns.

Other feature is supply input under voltage lockout. The uP1951 is available in thermal enhanced WQFN3x3-16L package.

Output Disable

Logic low of OD#x disables the gate drivers and keep both output low. Tie the OD#x pin to controller power directly if the output disable function is not used.

PWM Input

The PWMx pin is a tri-state input. Logic high turns on the high-side gate driver and turns off the low side gate driver once the POR of VCC is granted and OD#x is kept high. Logic low turns off the high side gate driver and turns on the low side gate driver.

High impedance input at PWMx pin will keep both high-side and low-side gate drivers low and turns off both MOSFETs. The PWMx pin voltage is kept around 2.0V by internal bias circuit when floating.

Low Side Driver

The low-side driver is designed to drive a ground-referenced N-Channel MOSFET. The bias to the low-side driver is internally connected to VCCx supply and GND. The low-side driver output is out of phase with the PWM input when it is enabled. The low side driver is held low if the OD#x pin is pulled low or high-impedance at PWM pin.

High-Side Driver

The high-side driver is designed to drive a floating N-Channel MOSFET. The bias voltage to the high-side driver internally connected to BOOTx and PHx pins. An external bootstrap supply circuit that is connected between BOOTx and PHx pins provides the bias current for the high-side gate driver.

The bootstrap capacitor C_{BOOT} is charged to V_{CC} when PHx pin is grounded by turning on the low-side MOSFET. The PHx rises to V_{IN} when the high-side MOSFET is turned on, forcing the BOOT pin voltage to $V_{IN} + V_{CC}$ that provides voltage to hold the high-side MOSFET on.

The high-side gate driver output is in phase with the PWMx input when it is enabled. The high-side driver is held low if the OD#x pin is pulled low or high-impedance at PWM pin.

Adaptive Shoot Through Protection

The adaptive shoot-through circuit prevents the high-side and low-side MOSFETs from being ON simultaneously and conducting destructive large current. It is done by turning on one MOSFET only after the other MOSFET is off already with adequately delay time.

At the high-side off edge, UGx and PHx voltages are monitored for anti-shoot-through protection. The uP1951 will not begin to output low-side driver high until both (V_{UGx} - V_{PHx}) and V_{PHx} are lower than 1.2V, making sure the high-side MOSFET is turned off completely.

At the low-side off edge, LGx voltage is monitored for anti-shoot-through protection. The uP1951 will not begin to output high-side driver high until V_{LGx} is lower than 1.2V, making sure the low-side MOSFET is turned off completely.

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Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC12 ---------- -0.3V to +15V
BOOTx to PHx ---------- -0.3V to +15V
PHx to GND
- DC ---------- -0.7V to 15V
- < 200ns ---------- -8V to 30V

BOOTx to GND
- DC ---------- -0.3V to VCC12 + 15V
- < 200ns ---------- -0.3V to 42V

UGx to PHx
- DC ---------- -0.3V to (BOOTx - PHx +0.3V)
- <200ns ---------- -5V to (BOOTx - PHx + 0.3V)

LGx to GND
- DC ---------- -0.3V to + (VCC12 + 0.3V)
- <200ns ---------- -5V to VCC12 + 0.3V

PWMx ---------- -0.3V to +6V
OD#x ---------- -0.3V to (VCCx + 0.3)V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WQFN3x3 - 16L q_{JA} ---------- 68°C/W
- WQFN3x3 - 16L q_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C
- WQFN3x3 - 16L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- 10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

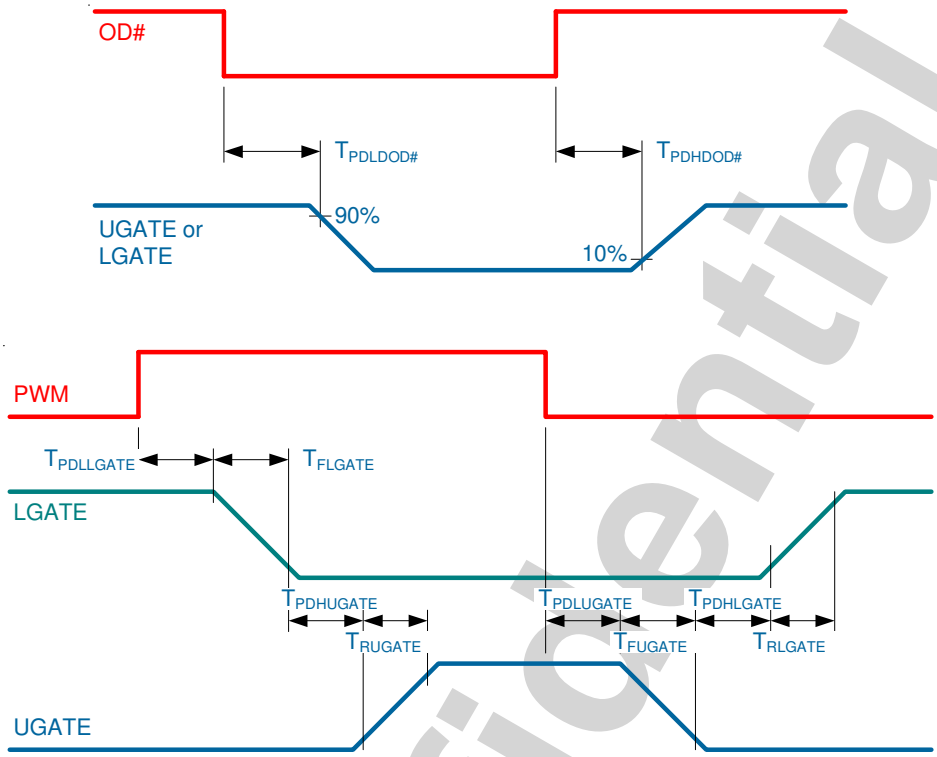
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Electrical Characteristics

(V_{CCX} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Voltage	V_{CC}		10.8	--	13.2	V
Supply Input Current	I_{CC}	PWMx = OD#x = 0V, each channel	--	2	5	mA
VCCx POR Rising Threshold	V_{CCXRTH}	V_{CCX} rising	4.0	4.2	4.4	V
VCCx POR Hysteresis	V_{CCXHYS}		--	0.25	--	V
PWM Input						
Input High Threshold	PWM_{RTH}		3.15	3.45	3.75	V
Input Low Threshold	PWM_{FTH}		0.6	0.9	1.2	V
PWM Floating Voltage	PWM_{FLT}		1.75	1.95	2.15	V
PWM Input Current	I_{PWM}	PWM = 0V	-420	-280	-140	uA
		PWM = 5V	1.0	1.6	1.9	mA
Output Disable Input OD#x						
Input High	$OD\#_H$		2.6	--	--	V
Input Low	$OD\#_L$		--	--	0.8	V
OD# Input Current	$I_{OD\#}$	OD# = 0V to 5V	-1	--	1	uA
Propagation Delay Time	$T_{PDHOD\#}$		--	20	45	ns
	$T_{PDLOD\#}$		--	20	45	ns
High Side Driver						
Output Resistance, Sourcing	R_{H_SRC}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = -80mA	--	1.6	3.2	Ω
Output Resistance, Sinking	R_{H_SNK}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = 80mA	--	1.5	3.0	Ω
Output Rising Time	T_{RUGATE}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T_{FUGATE}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	$T_{PDHUGATE}$	V_{BOOT} - V_{PHASE} = 12V	--	40	65	ns
	$T_{PDLUGATE}$	V_{BOOT} - V_{PHASE} = 12V	--	20	35	ns
Low Side Driver						
Output Resistance, Sourcing	R_{L_SRC}	V_{CC} = 12V, I_{LGATE} = -80mA	--	1.2	2.4	Ω
Output Resistance, Sinking	R_{L_SNK}	V_{CC} = 12V, I_{LGATE} = 80mA	--	0.8	1.6	Ω
Output Rising Time	T_{RLGATE}	V_{CC} = 12V, C_{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T_{FLGATE}	V_{CC} = 12V, C_{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	$T_{PDHLGATE}$	V_{CC} = 12V	--	40	65	ns
	$T_{PDLLGATE}$	V_{CC} = 12V	--	20	35	ns

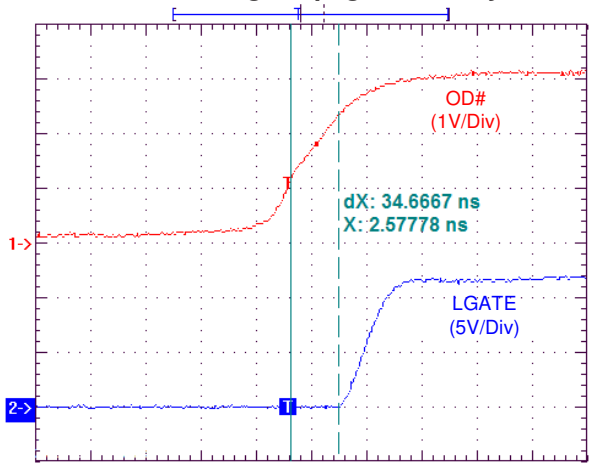
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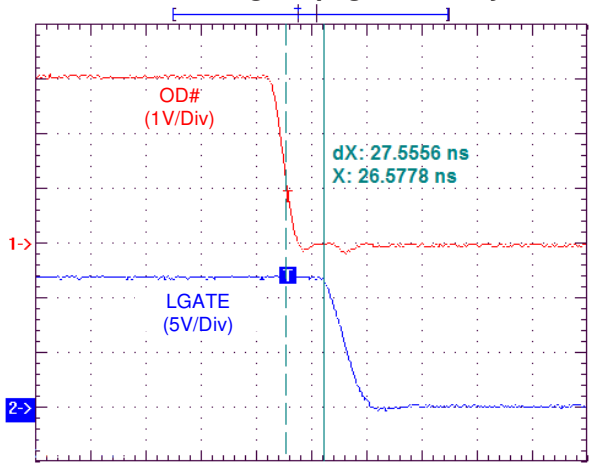
Typical Operation Characteristics

OD# Rising Propagation Delay



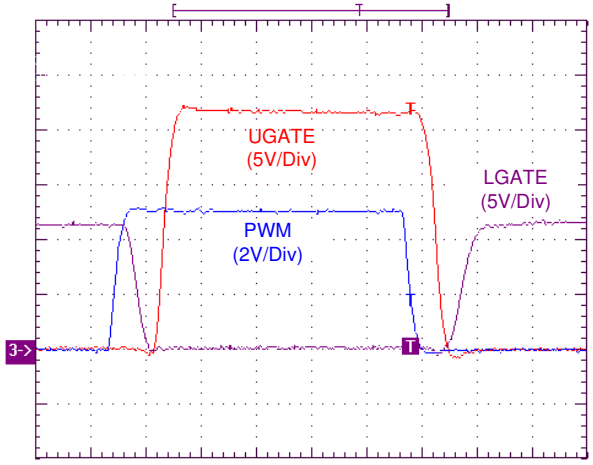
Time (40ns/Div)
PWM = 0V, 20MHz bandwidth limited

OD# Falling Propagation Delay



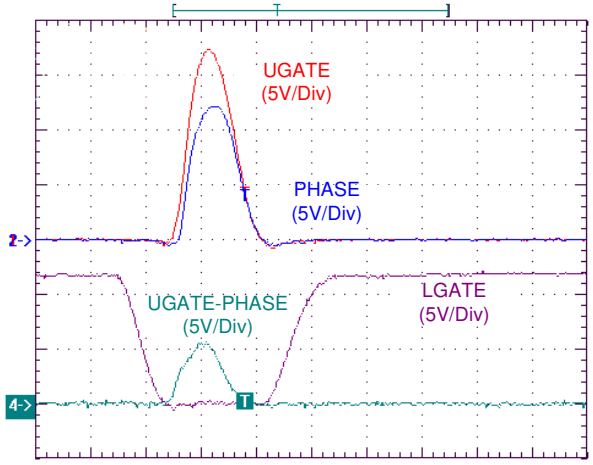
Time (40ns/Div)
PWM = 0V, 20MHz bandwidth limited

PWM Propagation Delay



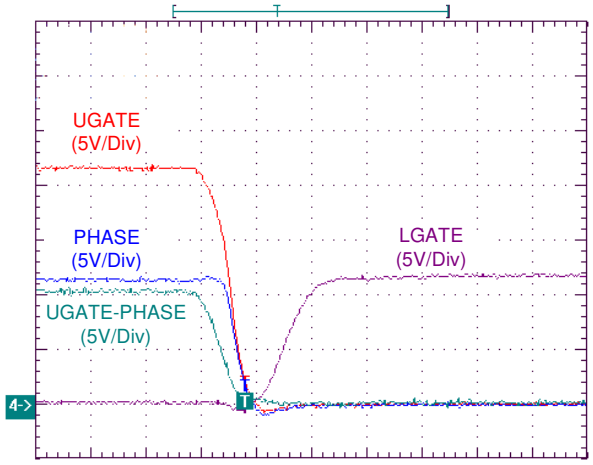
Time (80ns/Div)
20MHz bandwidth limited

Short Pulse Waveforms



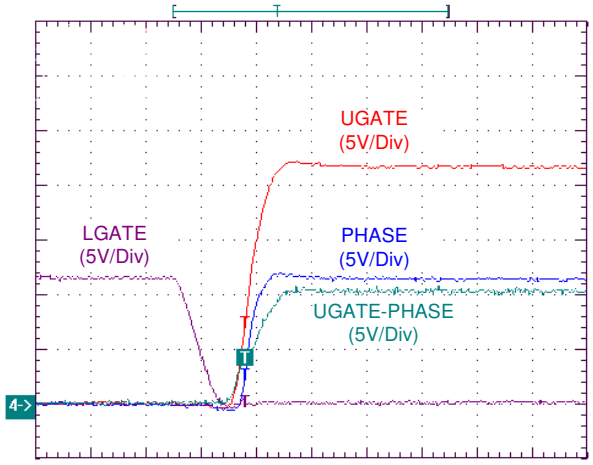
Time (40ns/Div)
20MHz bandwidth limited

Switching Waveforms



Time (40ns/Div)
20MHz bandwidth limited

Switching Waveforms



Time (40ns/Div)
20MHz bandwidth limited

Application Information

Thermal Consideration

The power dissipation in uP1951 is dependent of the supply voltage, the PWM frequency and the input capacitance of the MOSFET:

$$P_{LOSS} = V_{CC}\{I_{CC} + [V_{CC}(C_{ISS_U} + C_{ISS_L}) + V_{IN} \times C_{OSS_U}]f_{PWM}\}$$

where V_{CC} is the supply voltage, I_{CC} is the operation current of the control circuit, C_{ISS_U} and C_{ISS_L} are the total input capacitance of the upper and lower MOSFET respectively, V_{IN} is the supply voltage of the buck converter, C_{OSS_U} is the reverse transfer capacitance regarding the Miller effect and f_{PWM} is the PWM input frequency. Take a typical case for example, V_{CC} = 12V, I_{CC} = 1mA, C_{ISS_U} = 2x1.5nF, C_{OSS_U} = 2x0.1nF, V_{IN} = 12V, CISS_L = 2x3nF, f_{OSC} = 300kHz for each phase, the total power dissipation is calculated as:

$$P_{LOSS} = 2 \times 12V\{1mA + [12V(3nF + 6nF) + 12V \times 0.2nF]300kHz\}$$
$$= 0.82W$$

The junction temperature raise is calculated as:

$$\Delta T = T_J - T_A = \theta_{JA} \times P_{LOSS}$$
$$= 68^{O}C/W \times 0.82W$$
$$= 55.8^{O}C$$

Layout Consideration

Follow the layout guidelines for optimum performance of uP1951.

1.) Place the uP1951 physically near the power stages of buck converter.

2.) The exposed pad should be well soldered to the PCB with multiple vias to inner ground plane for optimum thermal performance.

3.) Place the bootstrap diode and capacitor physically near the IC.

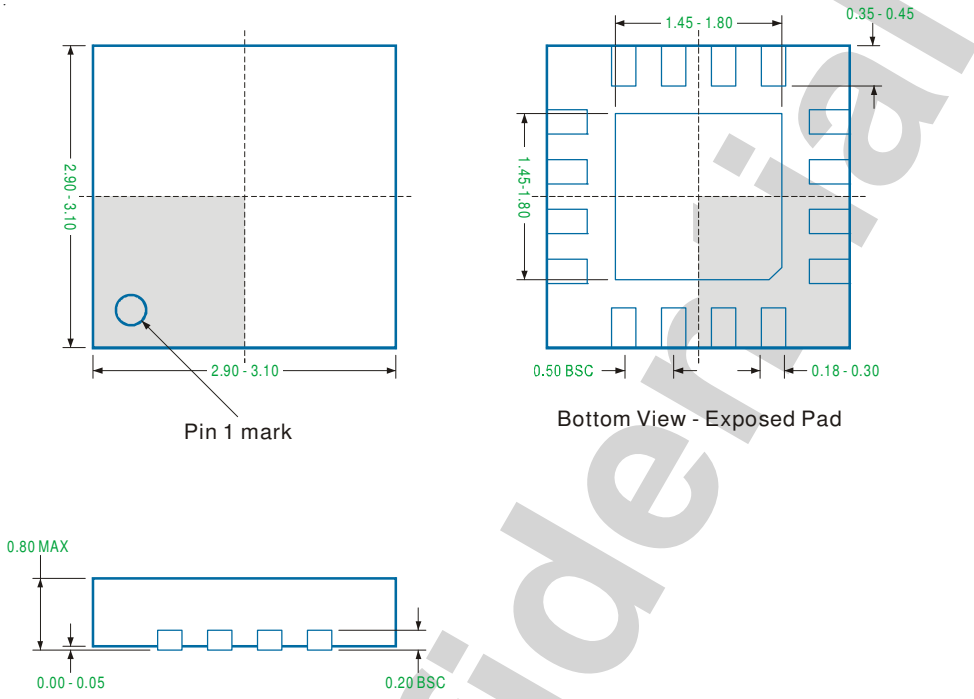
4.) Connect the PHx, UGx, LGx to the power MOSFET with short and wide traces. Minimize the number of vias along the traces.

5.) The PWMx and OD#x are high impedence node and sensitive to noise. They should be kept away from noise source, especilly when the connecting traces between controller and driver are long.

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Package Information

WQFN3x3 - 16L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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