PKS603-607

PeakSwitch™ Family

Enhanced, Energy-Efficient, Off-Line Switcher IC With Super Peak Power Performance

Product Highlights

EcoSmart® – Extremely Energy-Efficient

- Standby output power ≥0.6 W for 1 W input (high line)
- Sleep mode power ≥2.4 W at 3 W input (high line)
- No-load consumption <200 mW at 265 VAC input
- Surpasses California Energy Commission (CEC), ENERGY STAR, and EU requirements

PeakSwitch Features Reduce System Cost

- Delivers peak power of up to three times maximum continuous output power
- 277 kHz operation during peak power significantly reduces transformer size
- Programmable smart AC line sensing provides latching shutdown during short circuit, overload and open loop faults, and prevents glitches during power down or brownout
- Two external components reset latch on AC removal
- Adaptive switching cycle on-time extension increases low line peak output power, minimizing bulk capacitor size
- Adaptive current limit reduces output overload power
- Frequency jittering reduces EMI filter cost
- Tight I^2f tolerances and negligible temperature variation of key parameters ease design and lower cost
- Accurate hysteretic thermal shutdown with automatic recovery provides complete system level overload protection and eliminates need for manual reset

Better System Cost/Performance over RCC & Discrete

- Simple ON/OFF control – no loop compensation needed
- Very low component count – higher reliability and single side printed circuit board
- High bandwidth provides fast turn on with no overshoot and excellent transient load response
- Peak current limit operation rejects line frequency ripple
- Built-in current limit and hysteretic thermal protection

Applications

- Inkjet printer
- Data storage, audio amplifier, DC motor drives

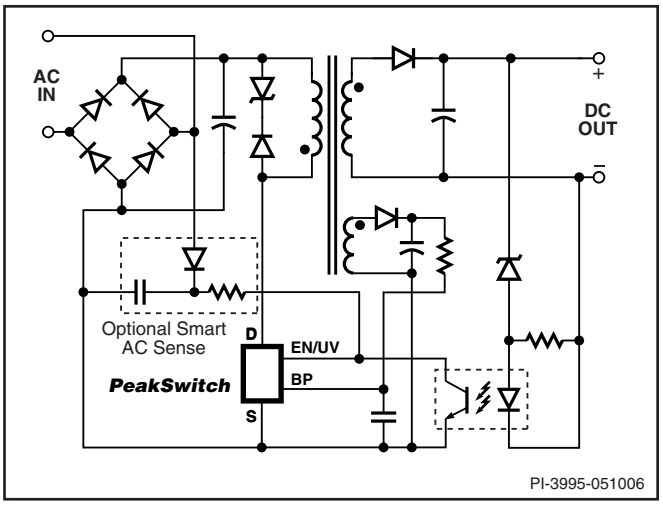


Figure 1. Typical Peak Power Application.

OUTPUT POWER TABLE				
PRODUCT[3]	230 VAC ±15%		85-265 VAC	
	Adapter Cont.[1]	Adapter Peak[2]	Adapter Cont.[1]	Adapter Peak[2]
PKS603 P	13 W	32 W	9 W	25 W
PKS604 P	23 W	56 W	16 W	44 W
PKS604 Y/F	35 W	56 W	23 W	44 W
PKS605 P	31 W	60 W	21 W	44 W
PKS605 Y/F	46 W	79 W	30 W	58 W
PKS606 P	35 W	66 W	25 W	46 W
PKS606 Y/F	68 W	117 W	45 W	86 W
PKS607 Y/F	75 W	126 W	50 W	93 W

Table 1.

Notes:
1. Typical continuous power in a non-ventilated enclosed adapter measured at +50 °C ambient.
2. Typical peak power for a period of 100 ms and a duty cycle of 10% in a non-ventilated enclosed adapter measured at +50 °C (see Key Applications section for details).
3. See Part Ordering Information.

Description

PeakSwitch is designed to address applications with high peak-to-continuous power ratio demands. The very high switching frequency during peak power loads and excellent load transient response reduce system cost as well as component count and size. *PeakSwitch* incorporates a 700 V power MOSFET, oscillator, high voltage switched current source for startup, current limit, and thermal shutdown onto a monolithic device. In addition, these devices incorporate auto-restart, line under-voltage sense and frequency jittering. An innovative design minimizes audio frequency components in the simple ON/OFF control scheme to practically eliminate audible noise with standard varnished transformer construction.

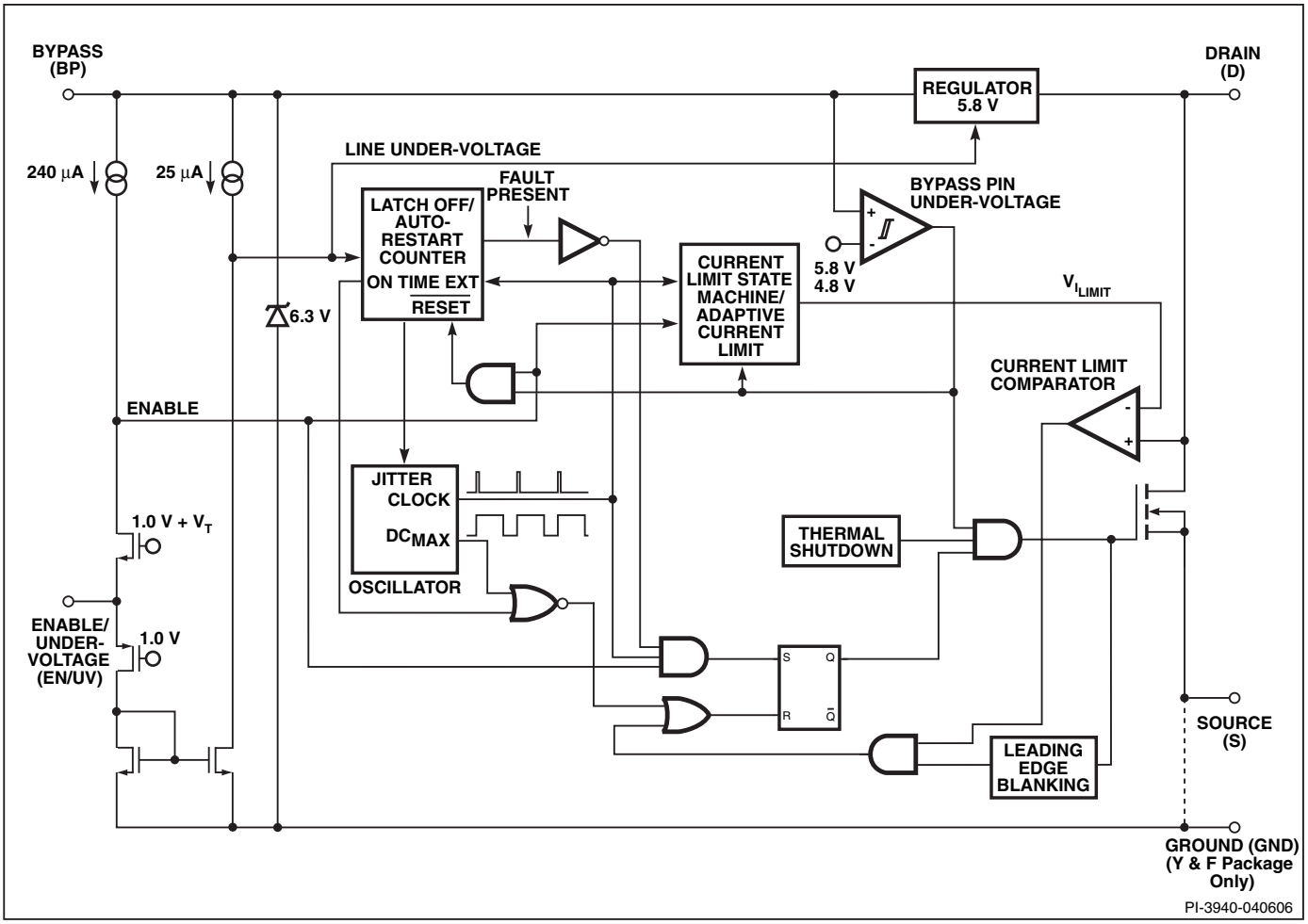


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
The power MOSFET drain connection provides internal operating current for both startup and steady-state operation.

BYPASS (BP) Pin:
A 0.33 µF external bypass capacitor for the internally generated 5.8 V supply is connected to this pin. In typical applications, this pin must be externally supplied via a bias winding.

ENABLE/UNDER-VOLTAGE (EN/UV) Pin:
This pin has dual functions: enable input and line under-voltage sense. During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is disabled when a current greater than 240 µA is drawn from this pin. This pin may also sense line under-voltage conditions through either an external resistor connected to the DC line voltage or an AC sense circuit.

SOURCE (S) Pin:
This is the MOSFET source connection for high voltage return and control circuit common.

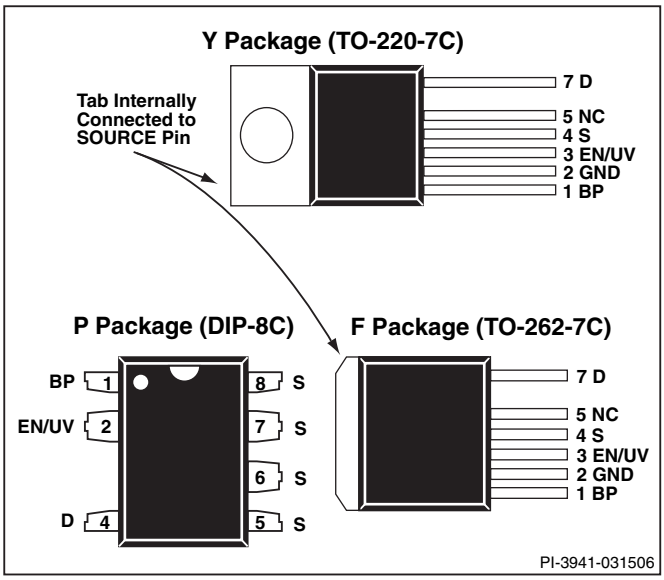


Figure 3. Pin Configuration.

GROUND (GND) Pin (Y or F Package Only):
This is the signal ground for the bypass capacitor and optocoupler.

PeakSwitch Functional Description

PeakSwitch integrates a 700 V power MOSFET switch with a power supply controller on the same die. Unlike conventional pulse width modulation (PWM) controllers, *PeakSwitch* uses a simple ON/OFF control to regulate the output voltage.

The controller consists of an oscillator, enable circuit (sense and logic), current-limit state machine, 5.8 V regulator, BYPASS pin under-voltage circuit, over-temperature protection, current limit circuit, and leading edge blanking. *PeakSwitch* incorporates additional circuitry for adaptive current limit, line under-voltage sense, programmable smart line sense, auto-restart, adaptive switching cycle on-time extension, and frequency jitter. Figure 2 is a functional block diagram of the device's most important features.

Oscillator

The typical oscillator frequency is internally set to an average of 277 kHz. Two signals are generated from the oscillator: the maximum duty cycle (DC_{MAX}) signal and the clock signal that indicates the beginning of each cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 16 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1.1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter.

Enable Input and Current-Limit State Machine

The enable input circuit at the EN/UV pin consists of a low impedance source follower output set at 1.0 V. The current through the source follower is limited to 240 µA. When the current out of this pin exceeds 240 µA, a low logic level (disable) is generated at the output of the enable circuit. This enable circuit output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled). If low, the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the EN/UV pin voltage or current during the remainder of the cycle are ignored.

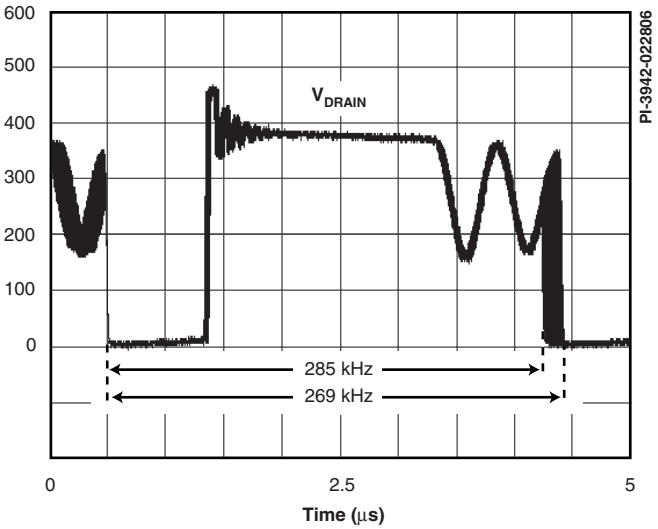


Figure 4. Frequency Jitter.

The current-limit state machine reduces the current limit by discrete amounts at light loads when *PeakSwitch* is likely to switch in the audible frequency range. The lower current limit raises the effective switching frequency above the audio range and reduces the transformer flux density, including the associated audible noise. The state machine monitors the sequence of EN/UV pin voltage levels to determine the load condition and adjusts the current limit level accordingly in discrete amounts.

Under most operating conditions (except when close to no-load), the low impedance of the source follower keeps the voltage on the EN/UV pin from going much below 1.0 V in the disabled state. This improves the response time of the optocoupler that is usually connected to this pin.

5.8 V Regulator and 6.3 V Shunt Voltage Clamp

The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN pin whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the *PeakSwitch* operates from the energy stored in the bypass capacitor. The voltage on the DRAIN pin powers the bypass during start-up.

There is a 6.3 V shunt regulator clamping the BYPASS pin at 6.3 V when current is provided through an external resistor from the bias winding in normal operation. Powering the *PeakSwitch* device in this way minimizes no-load consumption to about 150 mW at 265 VAC. Note that a bias winding must be used to power the device. See Key Application Considerations section for details.

BYPASS Pin Under-Voltage

The BYPASS pin under-voltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.8 V. Once the BYPASS pin voltage drops below 4.8 V, it must rise back to 5.8 V to enable (turn on) the power MOSFET.

Over Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is typically set at 142 °C with 75 °C hysteresis. When the die temperature rises above this threshold, the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled. A large

hysteresis of 75 °C (typical) is provided to prevent overheating of the PC board during a continuous fault condition.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The current limit state machine reduces the current limit threshold by discrete amounts under medium and light loads.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the MOSFET conduction portion of the switching cycle.

During startup and fault conditions, the controller prevents excessive drain currents by reducing the switching frequency.

Adaptive Current Limit

When switching in the full current limit state, a skipped cycle followed by a cycle that terminates at the full current limit implies that the line voltage is at high line. Under this condition, adaptive current limit reduces the full current limit level by approximately 10% in order to reduce output overload power. The next skipped cycle disables the adaptive current limit condition and restores the full current limit level.

Line Under-Voltage Sense Circuit

The line under-voltage circuit prevents startup below the programmed input voltage by connecting an external resistor from either the DC line or from an AC sense circuit (see Figure 1) to the EN/UV pin. The complete function is described in the flow chart shown in Figure 5. During power up or when the switching of the power MOSFET is disabled in auto-restart, the current flowing into the EN/UV pin must exceed 25 µA to initiate switching of the power MOSFET. During power up, once the threshold is exceeded, the Bypass pin must charge from 4.8 V to 5.8 V before MOSFET switching is initiated.

The line under-voltage circuit also detects when there is no external resistor connected to the EN/UV pin (less than ~1 µA into pin). In this case, the line under-voltage function is disabled and the device operates with a normal auto-restart function.

Programmable Smart AC Line Sense

When an external AC sense circuit is used (see Figure 1), the line under-voltage sense circuit can be used to determine the reason for a loss of feedback signal at the EN/UV pin. In the event of a fault condition such as output overload, output short circuit, or an open loop condition, the power MOSFET switching is disabled after the EN/UV pin is not pulled low for 30 ms. If the AC line is present (I_{EN} > 25 µA) at the time switching is disabled,

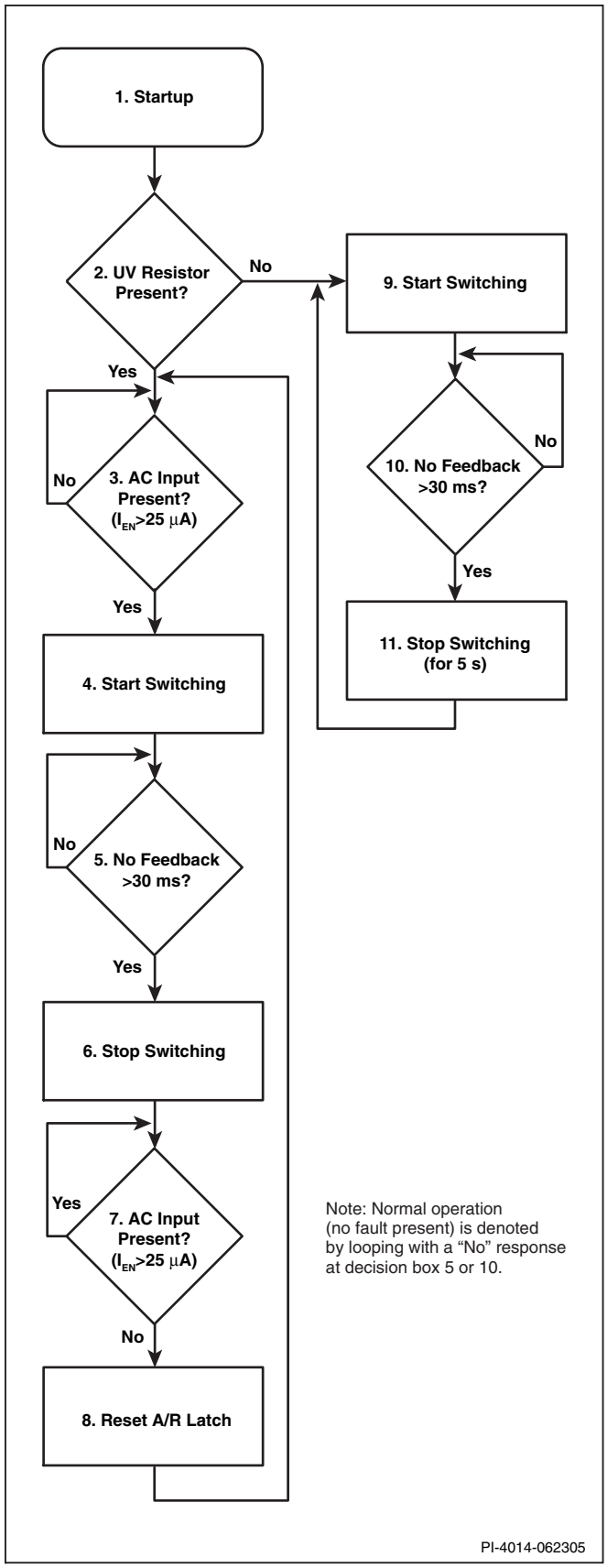


Figure 5. PeakSwitch Line Sense Function Flow Chart.

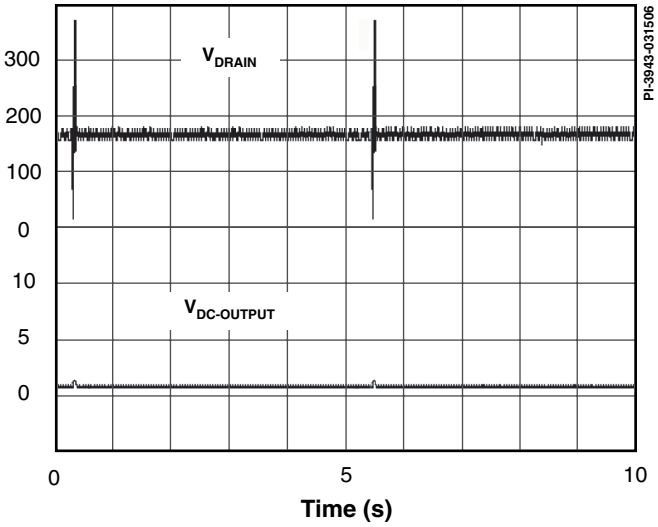


Figure 6. PeakSwitch Auto-Restart Operation.

the line under-voltage sense circuit prevents a restart attempt until the AC input voltage is removed (I_{EN} <25 µA). Then the internal auto-restart latch is reset and the power MOSFET switching will resume once the AC input voltage is applied again (I_{EN}>25 µA). This effectively provides a latching shutdown function with AC reset during such a fault condition.

When a brownout or line sag occurs, output regulation may be lost and the EN/UV pin will receive no feedback (it is pulled low). After 30 ms of no feedback, MOSFET switching is disabled. Since the AC line is abnormally low (I_{EN} <25 µA) MOSFET switching remains disabled until normal line voltage is restored. The power MOSFET switching will resume once the AC input returns to normal (I_{EN} >25 µA). This effectively disables the latching shutdown function during such a condition.

Auto-Restart (UV resistor not present)

In the event of a fault condition such as output overload, output short circuit or an open loop condition, *PeakSwitch* enters into auto-restart operation. An internal counter clocked by the oscillator is reset every time the EN/UV pin is pulled low. When the EN/UV pin receives no feedback for 30 ms, the power MOSFET switching is disabled for 5 seconds (150 ms for the first auto-restart event). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Figure 6 illustrates auto-restart circuit operation in the presence of an output short circuit.

Adaptive Switching Cycle On-time Extension

Adaptive switching cycle on-time extension keeps the MOSFET on until current limit is reached, instead of terminating after the DC_{MAX} signal goes low. This on-time extension is adaptive because it only occurs after the ENABLE pin has been high for approximately 750 µs, a condition that would arise if the peak output power was required in low line conditions. On-time extension is disabled during the startup of the power supply.

PeakSwitch Operation

PeakSwitch devices operate in the current-limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached. Since the highest current limit level and frequency

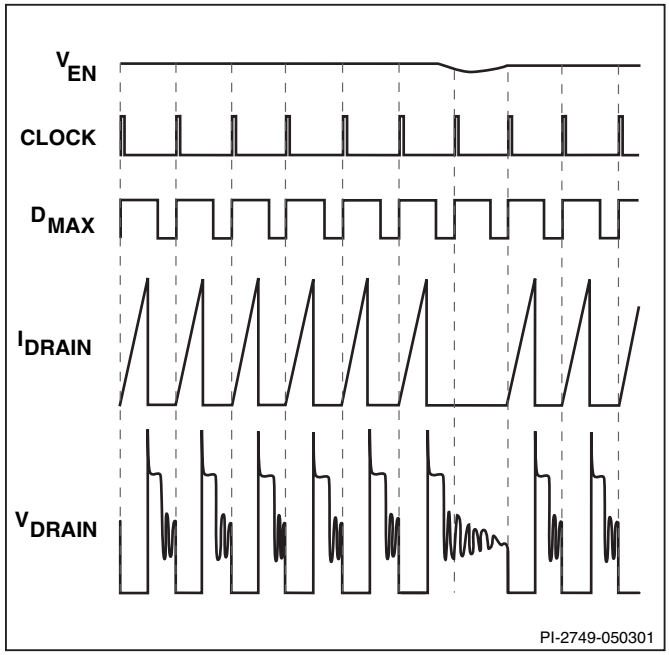


Figure 7. PeakSwitch Operation at Near Maximum Loading.

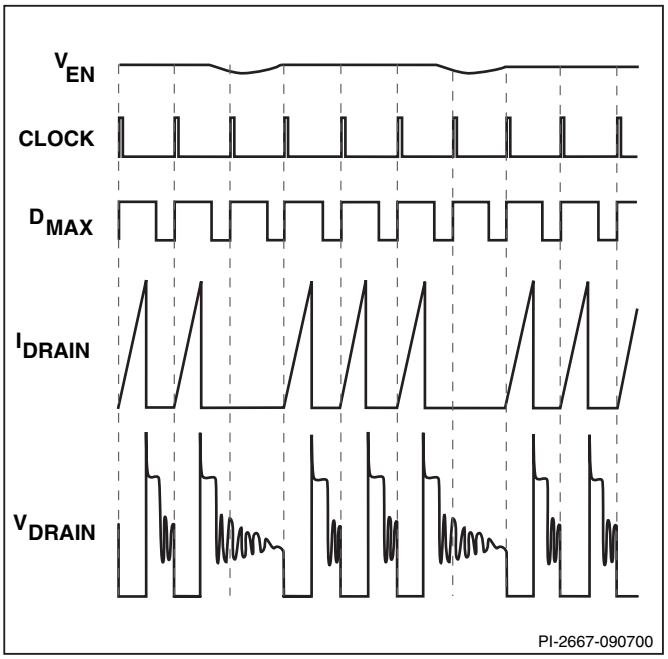


Figure 8. PeakSwitch Operation at Moderately Heavy Loading.

of a *PeakSwitch* design are constant, the power delivered to the load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the chosen *PeakSwitch* family member is appropriate for the power level, the current in the calculated inductance will ramp up to current limit before the DC_{MAX} limit is reached.

Enable Function

PeakSwitch senses the EN/UV pin to determine whether or not to proceed with the next switching cycle as described earlier. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle (even when the EN/UV pin changes state half way through the cycle). This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, amount of energy per switch cycle and the delay of the feedback.

The EN/UV pin signal is produced on the secondary by comparing the power supply output voltage with a reference voltage. The EN/UV pin signal is high when the power supply output voltage is less than the reference voltage.

In a typical implementation, the EN/UV pin is driven by an optocoupler. The collector of the optocoupler transistor is connected to the EN/UV pin and the emitter is connected to the SOURCE pin. The optocoupler LED is connected in series with a Zener diode across the DC output voltage to be regulated. When the output voltage exceeds the target regulation voltage level (optocoupler LED voltage drop plus Zener voltage), the optocoupler LED will start to conduct, pulling the EN/UV pin low. The Zener diode can be replaced by a TL431 reference circuit for improved accuracy.

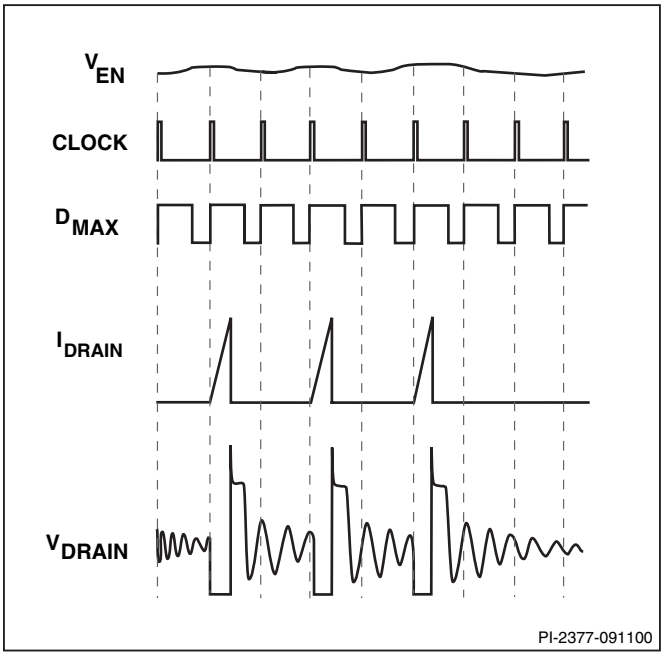


Figure 9. PeakSwitch Operation at Medium Loading.

ON/OFF Operation with Current-Limit State Machine

The internal clock of the *PeakSwitch* runs all the time. At the beginning of each clock cycle, it samples the EN/UV pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, when the EN/UV pin is high (less than 240 µA out of the pin), a switching cycle with the full current limit occurs. At lighter loads, when EN/UV is high, a switching cycle with a reduced current limit occurs.

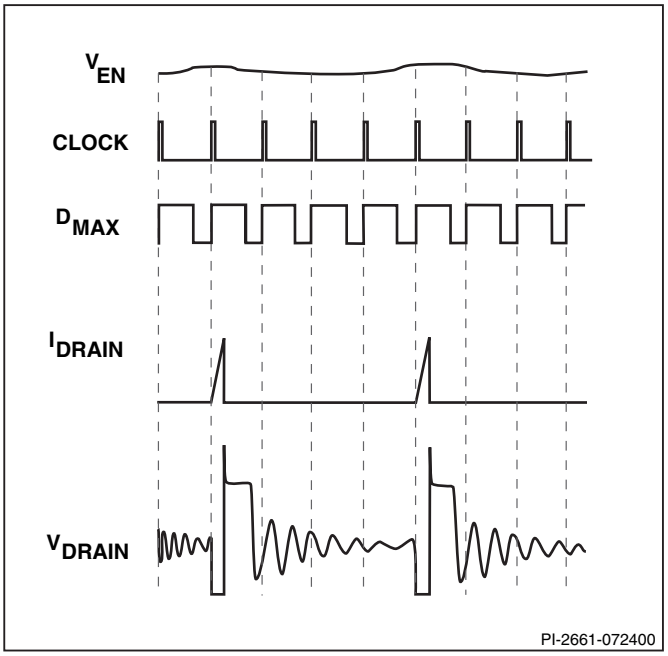


Figure 10. PeakSwitch Operation at Very Light Loading.

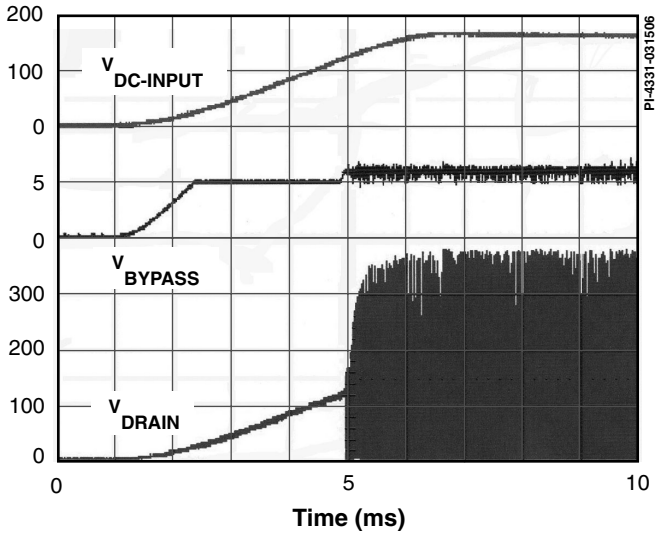


Figure 11. PeakSwitch Power Up with Optional External UV Resistor (4 MΩ) Connected to EN/UV Pin.

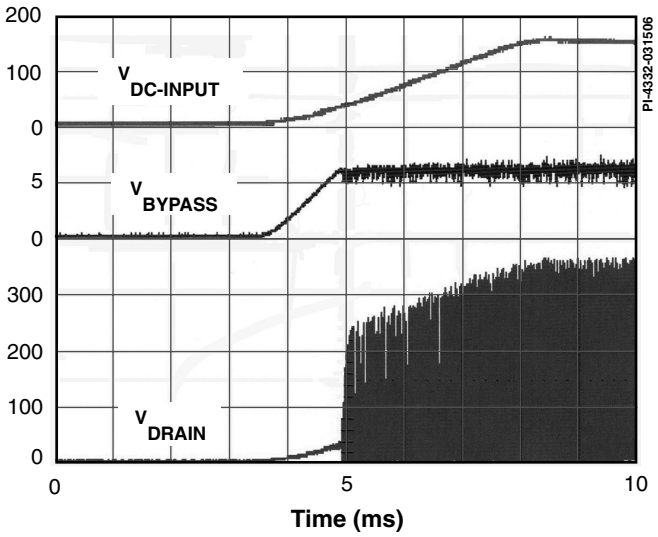


Figure 12. PeakSwitch Power Up Without Optional External UV Resistor Connected to EN/UV Pin.

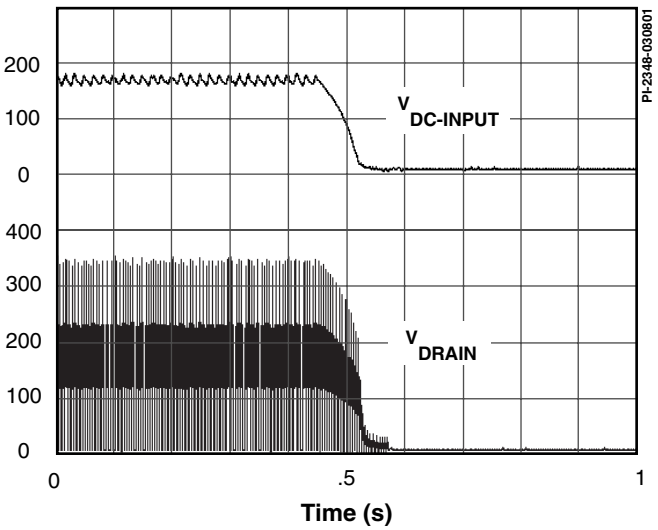


Figure 13. Normal Power Down Timing (Without UV).

At maximum peak load, *PeakSwitch* will conduct during nearly all of its clock cycles (Figure 7). At the rated continuous load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 8). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 9). At very light loads, the current limit will be reduced even further (Figure 10). Only a small percentage of cycles will occur to satisfy the internal power consumption of the power supply at no-load.

The response time of the ON/OFF control scheme is very fast compared to normal PWM control. This provides tight regulation and excellent transient response.

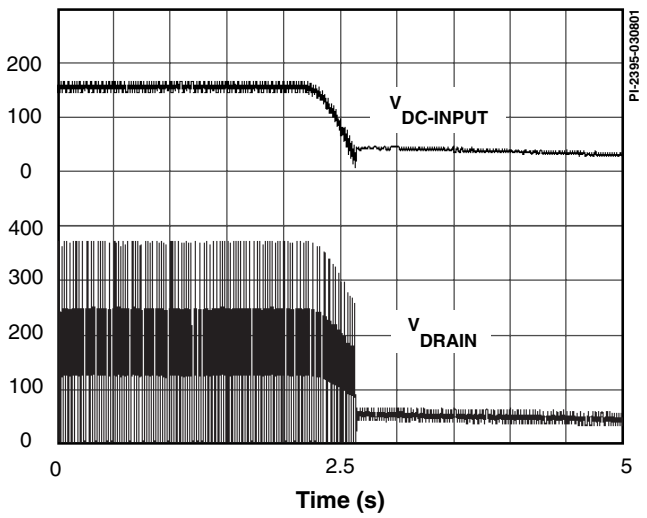


Figure 14. Slow Power Down Timing With Optional External (4 MΩ) UV Resistor Connected to EN/UV Pin.

Power Up/Down

The *PeakSwitch* requires only a 0.33 µF capacitor on the BYPASS pin. Because of its small size, the time to charge this capacitor is kept to an absolute minimum, typically less than 1.5 ms. Due to the fast nature of the ON/OFF feedback, there is no overshoot at the power supply output. When an external resistor is connected from the positive DC input to the EN/UV pin, the power MOSFET switching will be delayed during power up until the DC line voltage exceeds the threshold (100 V). Figures 11 and 12 show the power up timing waveform in applications with and without an external resistor (4 MΩ) connected to the EN/UV pin.

During power down, when an external resistor is used, the power MOSFET will switch for 30 ms after the output loses regulation. The power MOSFET will then remain off without any glitches since the under-voltage function prohibits restart when the line voltage is low.

Figure 13 illustrates a typical power-down timing waveform. Figure 14 illustrates a very slow power-down timing waveform as in standby applications. An external resistor is connected to the EN/UV pin in this case to prevent unwanted restarts.

Current Limit Operation

Each switching cycle is terminated when the DRAIN current reaches the current limit of the *PeakSwitch*. Current limit operation provides good line ripple rejection.

BYPASS Pin Capacitor

The BYPASS pin uses a small 0.33 uF ceramic capacitor for decoupling the internal power supply.

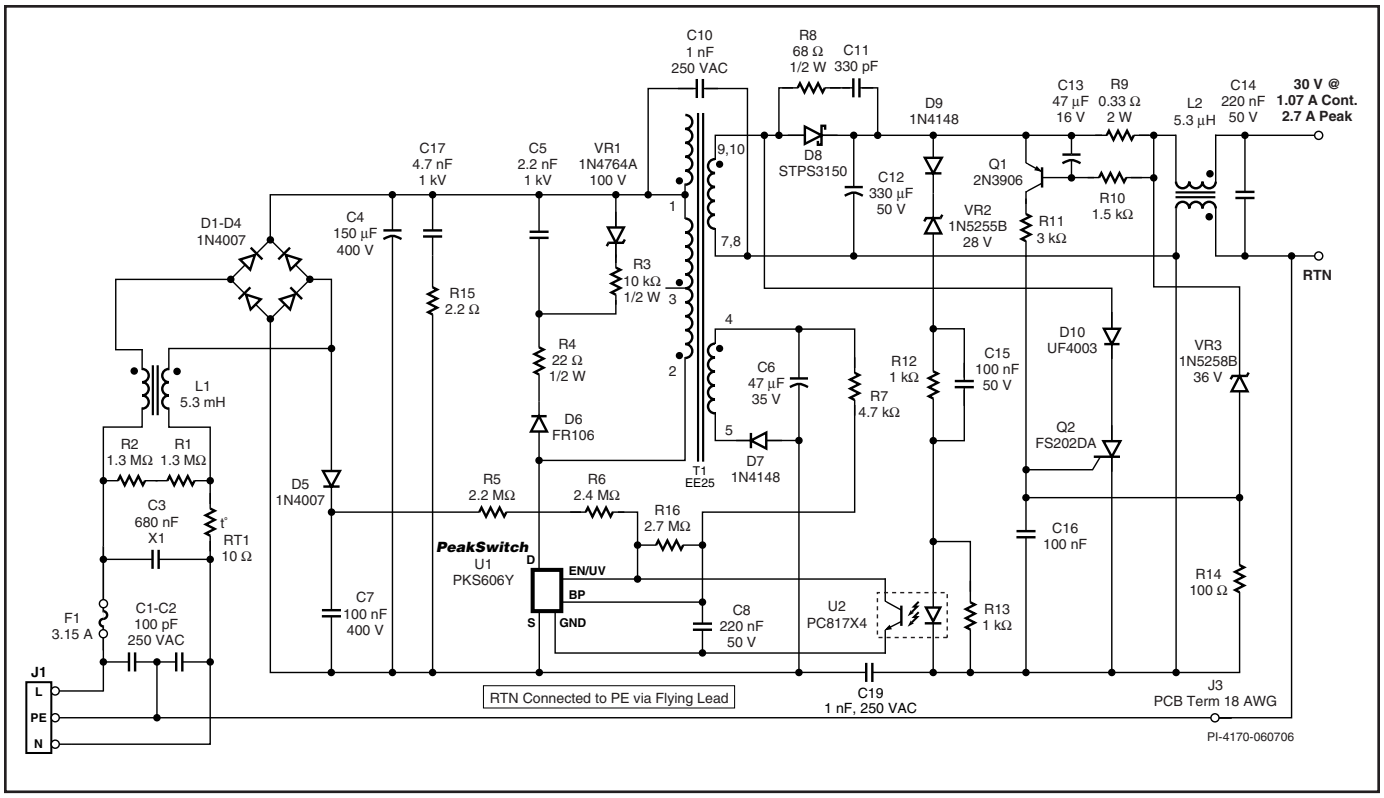


Figure 15. PeakSwitch PKS606Y, 32 W Continuous, 81 W Peak, Universal Input Power Supply.

Application Example

The circuit shown in Figure15 is a low cost, high efficiency, flyback power supply designed to provide a 30 V, 1.06 A continuous, 2.7 A peak output from universal input using the PKS606Y.

The supply features under-voltage lockout and smart AC sense with fast reset. Latching overload, open loop, and hysteretic thermal shutdown protect both the supply and load under fault conditions while high efficiency (>80%) and very low no-load consumption (<200 mW at 230 VAC) meets both active and standby efficiency requirements. Output regulation is accomplished using a simple Zener reference and opto coupler feedback.

Components C1, C2, C3, C10, C17, C19, R15, L1 and L2 provide common mode and differential mode EMI filtering. Resistors R1 and R2 discharge C3 when AC power is removed to prevent electric shock from touching the AC input. Thermistor RT1 limits the peak inrush current when AC is first applied.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. Diode D6, C5, R3, R4, and VR1 clamp the U1 drain voltage to safe levels. Use of a fast diode (500 ns) vs ultrafast for D6 increases power supply efficiency by recovering some of the clamp energy. A slow or standard recovery diode must not be used due to the high switching frequency (a slow diode will not recover fast enough under startup or output faults and therefore fail due to excess dissipation). The use of a Zener in series with R3 compared to a standard RCD clamp optimizes both EMI and energy efficiency.

Components D5, C7, and R5-6 provide AC line and under-voltage sensing for PeakSwitch U1. By providing a separate rectified voltage across C7 which is independent from the load condition, rather than using the main input capacitor, allows *PeakSwitch* to distinguish the cause of loss of regulation. It also provides fast reset when the AC input is removed, should latching shutdown be triggered. Connecting R5 and R6 to C4 would still provide under-voltage lockout but after a fault the user would have to wait for C4 to discharge before the supply would reset. Resistor R16 provides a small amount of bias to the U1 ENABLE/UNDER-VOLTAGE pin to retain the under-voltage lockout function during brown-out conditions.

With R5 and R6 present, switching is inhibited until the current into the EN/UV pin exceeds 25 µA. This allows the startup voltage to be programmed within the normal operating input voltage range, preventing glitching of the output under abnormal, low voltage conditions and also on removal of the AC input.

Under a fault condition, for example an output short circuit or broken feedback loop, if the line voltage is within the normal range (>25 µA into the EN/UV pin) the *PeakSwitch* will latch

off the power supply. This protects the load and supply from a continuous fault condition. Removing the AC input resets this condition.

The output voltage is determined by the Zener diode VR2, the voltage drop across R12 and the forward drop of D9 and the LED of optocoupler U2. Resistor R13 provides bias current through D9 and VR2, to ensure that VR2 is operating close to its knee voltage, while R12 sets the overall gain of the feedback loop. Capacitor C15 boosts high frequency loop gain to help distribute the enabled switching cycles and reduce pulse grouping.

When the output voltage exceeds the feedback threshold voltage, current will flow in the optocoupler LED, causing current flow in the transistor of the optocoupler. When this exceeds the ENABLE pin threshold current the next switching cycle is inhibited, as the output voltage falls (below the feedback threshold) a conduction cycle is allowed to occur and by adjusting the number of enabled cycles output regulation is maintained. As the load reduces the number of enabled cycles decreases, lowering the effective switching frequency and scaling switching losses with load. This provides almost constant efficiency down to very light loads, ideal for meeting energy efficiency requirements.

PeakSwitch device U1 is supplied from an auxillary winding on the transformer which is rectified and filtered by D7 and C6. Resistor R7 provides approximately 2 mA of supply current into the BYPASS pin capacitor C8. During startup or fault conditions when the bias voltage is low, the BYPASS pin is supplied from a high voltage current source within U1, eliminating the need for separate startup components.

Components Q1-2, R9-11, R14, C13, C16, and VR3 form an overvoltage and overcurrent protection circuit. An output overvoltage or overcurrent condition fires SCR Q2, clamping the output voltage and forcing *PeakSwitch* U1 into latching shutdown after 30 ms. The low pass filter formed by R10 and C13 adds a delay to the over-current sense. The shutdown condition can be reset by briefly removing AC power for ~3 seconds (maximum). The latching function within *PeakSwitch* significantly reduces the size of the SCR and output rectifier, D8, as the short circuit current only flows for 50 ms before the supply latches off.

This design meets EN55022 Class B conducted EMI with >10 dB margin even with the output RTN directly connected to earth ground.

Key Application Considerations

PeakSwitch Design Considerations

Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 100 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or single 100/115 VAC with a voltage doubler.
2. Efficiency of 70% for Y/F packaged devices, 75% for P packaged devices at 85-265 VAC, 75% for 230 VAC input all packages
3. Minimum datasheet value of I^2f
4. Transformer primary inductance tolerance of ±10%
5. Reflected output voltage (V_{OR}) of 135 V
6. Voltage only output of 15 V with an ultra fast PN rectifier diode
7. Continuous conduction mode operation with transient K_P* value of 0.25
8. Sufficient heatsinking is provided, either externally (Y/F packages) or through an area of PC board copper (P package) to keep the SOURCE pin or tab temperature at or below 110 °C.
9. Device ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters

*Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power capability due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This avoids the initial current limit (I_{INIT}) being exceeded at MOSFET turn on.

Peak vs. Continuous Power

PeakSwitch devices have current limit values that allow the specified peak power values in the power table. With sufficient heatsinking, these power levels could be provided continuously, however this may not be practical in many applications. *PeakSwitch* is optimized for use in applications that have short duration, high peak power demand, but a significantly lower continuous or average power. Typical ratios would be $P_{PEAK} \geq 2 \times P_{AVE}$. The high switching frequency of *PeakSwitch* allows a small core size to be selected to deliver the peak power, but the short duration prevents the transformer winding from overheating. As average power increases, it may be necessary to select a larger transformer to allow increased copper area for the windings based on the measured transformer temperature.

The power table provides some guidance between peak power and continuous power in sealed adapters, however specific applications may differ. For example, if the peak power condition is very low duty cycle, say a 2 second peak occurring only at power up to accelerate a hard disk drive, then the transformer's thermal rise is only a function of the continuous power. However, if the peak power occurs every 200 ms for 50 ms then it would need to be considered.

In all cases, the acceptable temperature rise of the *PeakSwitch* and transformer should be verified under worst case ambient and load conditions.

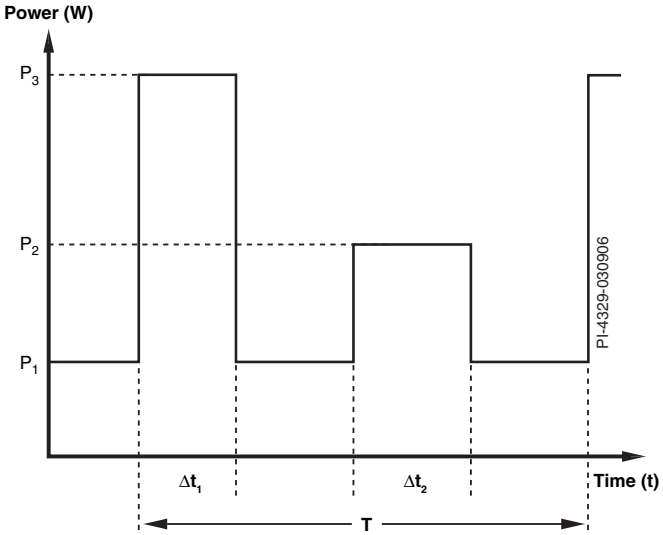


Figure 16. Continuous (Average) Output Power Calculation Example.

Figure 16 shows how to calculate the average power requirements for a design with two different peak load conditions.

$$P_{AVE} = P_1 + (P_3 - P_1) \cdot \delta_1 + (P_2 - P_1) \cdot \delta_2$$

$$\delta_1 = \frac{\Delta t_1}{T}, \delta_2 = \frac{\Delta t_2}{T}$$

Where P_X are the different output power conditions, Δt_X are the durations of each peak power condition, and T is the period of one cycle of the pulse load condtion.

Audible Noise

The cycle skipping mode of operation used in *PeakSwitch* can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result.

Ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits, may also generate audio noise. If this is the case try replacing them with a capacitor having a different type of dielectric or construction, for example a film type capacitor.

Maximum Flux Density

A maximum value of 3000 Gauss during normal operation is recommended to limit the maximum flux density under start up and output short circuit. Under these conditions the output voltage is low and little reset of the transformer occurs during the MOSFET off time. This allows the transformer flux density to staircase above the normal operating level. A value of 3000 Gauss at the peak current limit of the selected device, together with the built in protection features of *PeakSwitch* provides sufficient margin to prevent core saturation under startup or output short circuit conditions.

Optocoupler CTR

To minimize the delay introduced by the optocoupler, it is recommended that a high (300-600%) CTR optocoupler is used in *PeakSwitch* designs.

Bias Winding

All *PeakSwitch* designs must use a bias winding to feed operating current into the BYPASS pin once the supply is operational. It is recommended that the value of the resistor from the bias winding to the BYPASS pin be selected such that it supplies the same current as the maximum datasheet drain supply current (I_{S2}) for the specific device being used.

PeakSwitch Layout Considerations

See Figure 17 for a recommended circuit board layout for *PeakSwitch*.

Single Point Grounding

Devices in Y and F packages have separate return pins for the MOSFET source (S) and the controller (GND) connections which are internally connected. Therefore connecting these pins on the PC board is not recommended.

Devices in the P package do not have separate return pins, but in both cases the low current feedback signals and IC decoupling, high MOSFET current and bias winding primary return connection should route through separate traces to the Kelvin connection.

The bias winding return connection is treated separately, even though it carries low current. To route high currents away from the device when the supply is subjected to line surge transients, the bias winding should be returned directly to the input bulk capacitor.

Bypass Capacitor (C_{BP})

The BYPASS pin capacitor should be located as close as possible to the BYPASS and SOURCE pins.

Primary Loop Area

The area of the primary loop that connects the input filter capacitor, transformer primary and *PeakSwitch* together should be kept as small as possible.

Primary Clamp Circuit

A clamp is used to limit the peak voltage on the DRAIN pin at turn off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases to minimize EMI care should be taken to minimize the circuit path from the clamp components to the transformer and *PeakSwitch*.

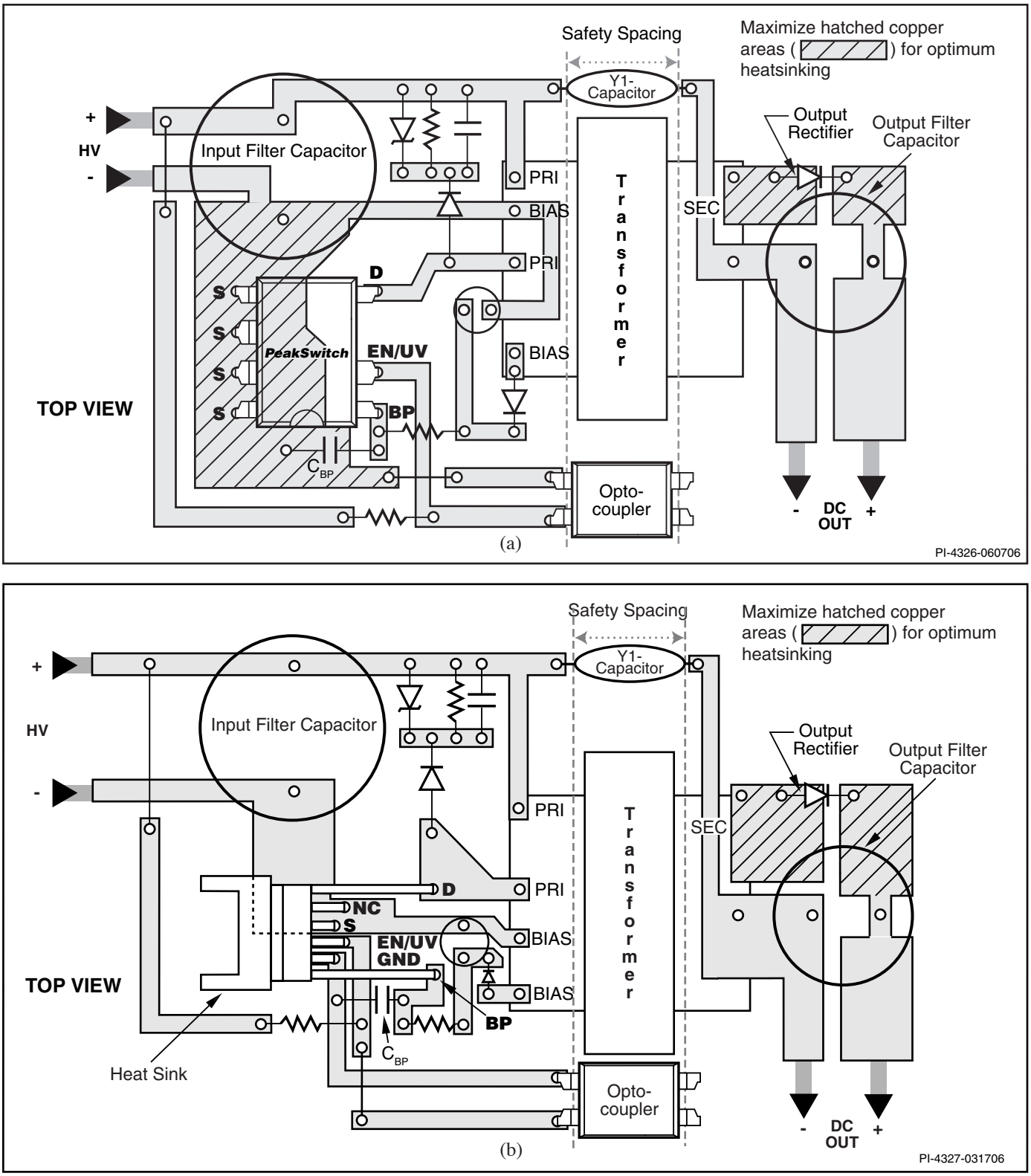


Figure 17. Recommended Layout for PeakSwitch in (a) P and (b) Y/F Packages.

Thermal Considerations

For the P package, the four SOURCE pins are internally connected to the IC lead frame and provide the main path to remove heat from the device. Therefore, all the SOURCE pins should be connected to a copper area underneath the *PeakSwitch* to act not only as a single point ground, but also as a heatsink. As this area is connected to the quiet source node, it should be maximized for good heatsinking. Similarly, for axial output diodes, maximize the PCB area connected to the cathode.

Y-Capacitor

The placement of the Y-type cap should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. If a second Y- type cap is required from primary to secondary return, connect the primary side directly to the negative terminal of the input capacitor. Such a placement will route high magnitude common mode surge currents away from the *PeakSwitch* device. Note – if an input π (C, L, C) EMI filter is used, then the inductor in the filter should be placed between the negative terminals on the input filter capacitors.

Optocoupler

Place the optocoupler physically close to the *PeakSwitch* to minimize the primary side trace lengths. Keep the high current high voltage drain and clamp traces away from the optocoupler to prevent noise pick up.

Output Diode

For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminal of the diode for heatsinking. A larger area is preferred at the quite cathode terminal. A large anode area can increase high frequency radiated EMI.

Quick Design Checklist

As with any power supply design, all *PeakSwitch* designs should be verified on the bench to make sure that component specifications are not exceeded under worst case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that the V_{DS} does not exceed 650 V at highest input voltage and peak (overload) output power. The 50 V margin to the 700 V BV_{DSS} specification allows margin for design variation.
2. Maximum drain currents – Verify the simultaneous drain voltage and current levels are within the curve provided in Figure 29 under worst case conditions. Typically this occurs at start up (and during an output short circuit), highest input line voltage and maximum ambient temperature. When making this measurement using a current probe, to monitor the drain current, ensure the results are corrected for the 10-20 ns current probe delay.
3. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms show no signs of transformer saturation. If the transformer shows signs of saturation, it should be redesigned with a lower flux density, or a higher quality core material should be used. To prevent false triggering of the current limit, verify the leading edge current spike event is below $I_{INIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the absolute maximum limit specified in the Absolute Maximum Ratings section.
4. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for *PeakSwitch*, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of *PeakSwitch* as specified in the data sheet. Under low line, maximum power, a maximum *PeakSwitch* SOURCE pin or tab temperature of 110 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations web site: www.powerint.com.

ABSOLUTE MAXIMUM RATINGS[1,4]

DRAIN Voltage .....-0.3 V to 700 V
DRAIN Peak Current: ..... $2 \times I_{LIMIT}$ (Typical)[5]
EN/UV Voltage .....-0.3 V to 9 V
EN/UV Current ....100 mA
BYPASS Voltage .....-0.3 V to 9 V
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature[2] .....-40 °C to 150 °C
Lead Temperature[3]..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. Maximum ratings specified may be applied one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.
5. Peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V. See also Figure 29.

THERMAL IMPEDANCE

Thermal Impedance: Y/F Package:
(θ_{JA})[1] .....80 °C/W
(θ_{JC})[2] .....2 °C/W
P Package:
(θ_{JA}) .....70 °C/W[3]; 60 °C/W[4]
(θ_{JC})[5] ..... 10 °C/W[5]

Notes:
1. Free standing with no heatsink.
2. Measured at the back surface of tab.
3. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
4. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.
5. Measured on the SOURCE pin close to plastic interface.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 18 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	T_J = 25 °C See Figure 4	Average	250	277	304	kHz
			Peak-Peak Jitter		16		
Maximum Duty Cycle	DC_{MAX}	S1 Open		62	65	68	%
EN/UV Pin Turn Off Threshold Current	I_{DIS}			-350	-240	-200	µA
EN/UV Pin Voltage	V_{EN}	$I_{EN/UV}$ = -125 µA		0.4	1.0	1.5	V
		$I_{EN/UV}$ = 25 µA		1.3	2.0	2.7	
DRAIN Supply Current	I_{S1}	$V_{EN/UV}$ = 0 V		350	475	600	µA
	I_{S2}	EN/UV Open (MOSFET Switching) See Note A, B	PKS603	460	570	690	
			PKS604	600	725	870	
			PKS605	700	875	1050	
			PKS606	950	1175	1400	
			PKS607	1160	1430	1700	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C See Note C	PKS603-604	-7.5	-5.0	-2.5	mA
			PKS605-607	-10.0	-6.6	-3.2	
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C See Note C	PKS603-604	-4.5	-3.0	-1.5	
			PKS605-607	-6.5	-4.5	-2.5	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 18 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS (cont.)							
BYPASS Pin Shunt Regulator Voltage	$V_{BP(SH)}$	See Note D		6.0	6.3	6.7	V
BYPASS Pin Voltage	V_{BP}			5.5	5.8	6.15	V
BYPASS Pin Voltage Hysteresis	V_{BPH}			0.8	1.0	1.3	V
EN/UV Pin Line Under-Voltage Threshold	I_{LUV}	T_J = 25 °C		22.5	25	27.5	µA
CIRCUIT PROTECTION							
Current Limit	I_{LIMIT}	PKS603 P T_J = 25 °C	di/dt = 200 mA/µs See Note E	0.75	0.81	0.87	A
		PKS604 P/Y/F T_J = 25 °C	di/dt = 290 mA/µs See Note E	1.35	1.45	1.55	
		PKS605 P T_J = 25 °C	di/dt = 290 mA/µs See Note E	1.35	1.45	1.55	
		PKS605 Y/F T_J = 25 °C	di/dt = 325 mA/µs See Note E	1.76	1.89	2.02	
		PKS606 P T_J = 25 °C	di/dt = 255 mA/µs See Note E	1.40	1.51	1.62	
		PKS606 Y/F T_J = 25 °C	di/dt = 660 mA/µs See Note E	2.60	2.80	3.00	
		PKS607 Y/F T_J = 25 °C	di/dt = 800 mA/µs	2.79	3.00	3.21	
Power Coefficient	I^2f	PKS603 P T_J = 25 °C	di/dt = 200 mA/µs	164	182	204	A^2kHz
		PKS604 P/Y/F T_J = 25 °C	di/dt = 290 mA/µs	524	582	652	
		PKS605 P T_J = 25 °C	di/dt = 290 mA/µs	524	582	652	
		PKS605 Y/F T_J = 25 °C	di/dt = 325 mA/µs	890	989	1108	
		PKS606 P T_J = 25 °C	di/dt = 255 mA/µs	569	632	708	
		PKS606 Y/F T_J = 25 °C	di/dt = 660 mA/µs	1955	2172	2433	
		PKS607 Y/F T_J = 25 °C	di/dt = 800 mA/µs	2242	2493	2793	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 18 (Unless Otherwise Specified)		Min	Typ	Max	Units
CIRCUIT PROTECTION (cont.)							
Initial Current Limit	I_{INIT}	See Figure 21 See Note F		0.75 × $I_{LIMIT(Min)}$			mA
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note F		170	215		ns
Current Limit Delay	t_{ILD}	T_J = 25 °C See Notes F, G			150		ns
Thermal Shutdown Temperature				135	142	150	°C
Thermal Shutdown Hysteresis					75		°C
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	PKS603 I_D = 81 mA	T_J = 25 °C		7.8	9.0	Ω
			T_J = 100 °C		11.7	13.5	
		PKS604 I_D = 150 mA	T_J = 25 °C		5.2	6.0	
			T_J = 100 °C		7.8	9.0	
		PKS605 I_D = 200 mA	T_J = 25 °C		3.9	4.5	
			T_J = 100 °C		5.8	6.7	
		PKS606 I_D = 300 mA	T_J = 25 °C		2.6	3.0	
			T_J = 100 °C		3.9	4.5	
		PKS607 I_D = 300 mA	T_J = 25 °C		2.0	2.3	
			T_J = 100 °C		3.0	3.5	
OFF-State Drain Leakage Current	I_{DSS1}	V_{BP} = 6.2 V $V_{EN/UV}$ = 0 V V_{DS} = 560 V T_J = 125 °C See Note H				200	µA
	I_{DSS2}	V_{BP} = 6.2 V $V_{EN/UV}$ = 0 V	V_{DS} = 375 V T_J = 50 °C See Note H		15		
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, $V_{EN/UV}$ = 0 V, See Note I, T_J = 25 °C		700			V
Drain Supply Voltage				50			V
Output EN/UV Delay	$t_{EN/UV}$	See Figure 20				5	µs
Output Disable Setup Time	t_{DST}				0.5		µs

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 18 (Unless Otherwise Specified)	Min	Typ	Max	Units
OUTPUT (cont.)						
Auto-Restart ON Time	t_{AR}	T_J = 25 °C See Note J		30		ms
Auto-Restart OFF Time	t_{AROFF}	See Note K		5		s

NOTES:

A. Total current consumption is the sum of I_{S1} and I_{DSS} when EN/UV pin is shorted to ground (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when EN/UV pin is open (MOSFET switching).

B. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 6.1 V.

C. See Typical Performance Characteristics section for BYPASS pin startup charging waveform.

D. BYPASS pin is externally supplied (bias winding).

E. For current limit at other di/dt values, refer to Figure 25.

F. This parameter is derived from characterization.

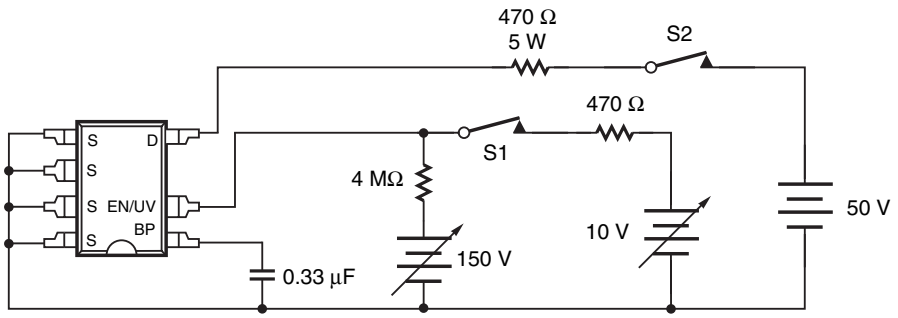
G. This parameter is derived from the change in current limit measured at 1X and 4X of the di/dt shown in the I_{LIMIT} specification.

H. I_{DSS1} is the worst case OFF state leakage specification at 80% of BV_{DSS} and maximum operating junction temperature. I_{DSS2} is a typical specification under worst case application conditions (rectified 265 VAC) for no-load consumption calculations.

I. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

J. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency). Auto-restart on time is extended during startup and certain fault conditions because the controller reduces its oscillator clock frequency to prevent excessive drain currents. If excessive drain currents are still occuring half way through the auto-restart on time, output MOSFET switching is disabled for the remainder of that auto-restart on time episode (if the line is not sensed) or the supply latches off (if the line is sensed and adequate line voltage is present).

K. Only applicable if no UV resistor is present at the EN/UV pin. 5 s applies only if the preceding switching auto-restart event did not result in EN/UV pin going low. In that event, the first auto-restart off-time is 150 ms.



NOTE: This test circuit is not applicable for current limit or output characteristic measurements.

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Figure 18. PeakSwitch General Test Circuit.

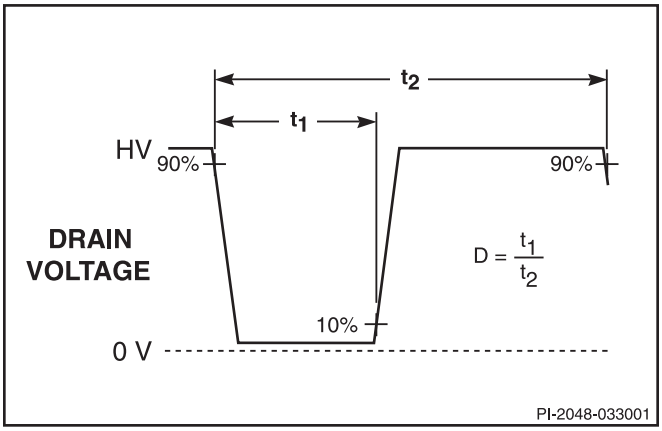


Figure 19. Duty Cycle Measurement.

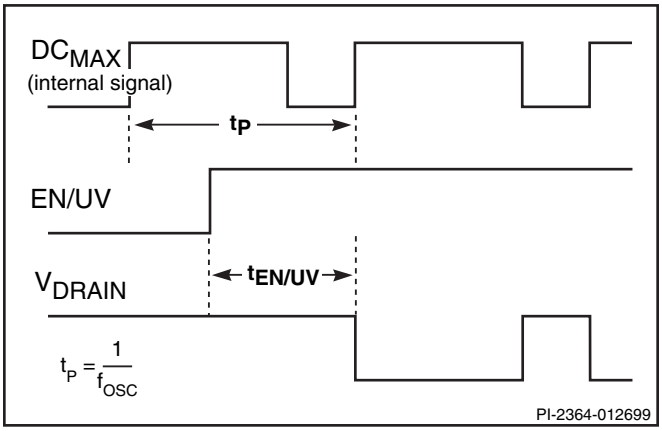


Figure 20. Output Enable Timing.

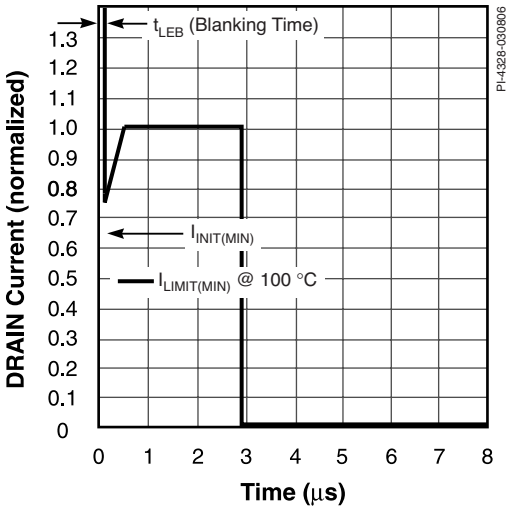


Figure 21. Current Limit Envelope.

Typical Performance Characteristics

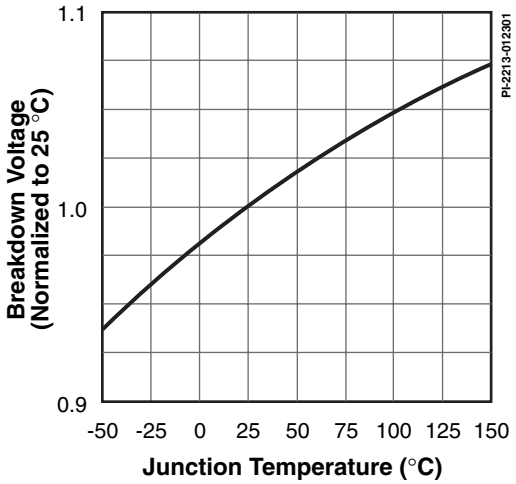


Figure 22. Breakdown vs. Temperature.

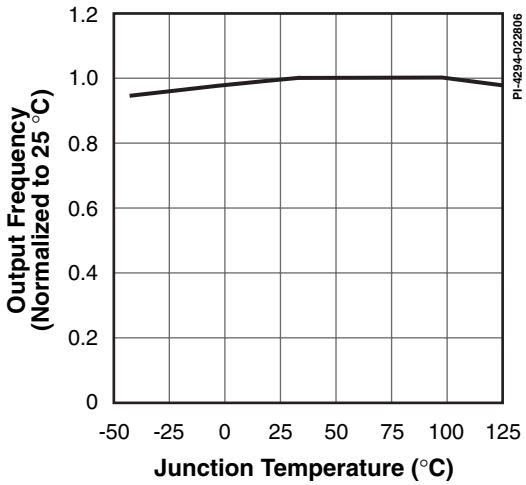


Figure 23. Frequency vs. Temperature.

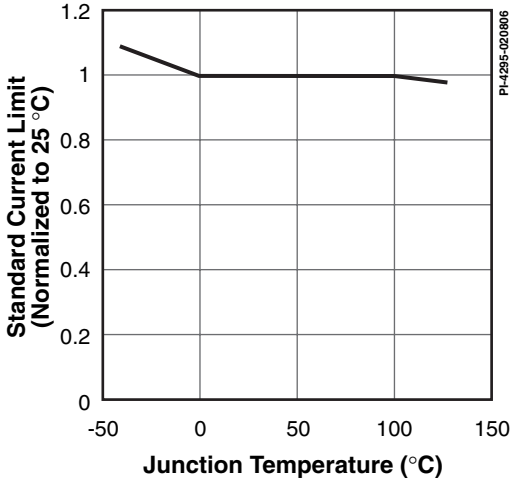


Figure 24. Standard Current Limit vs. Temperature.

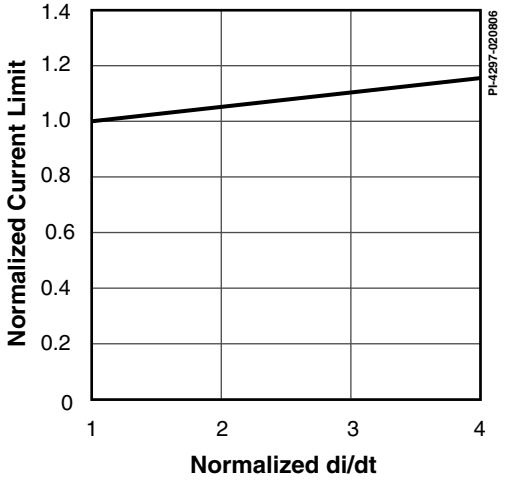


Figure 25. Current Limit vs. di/dt.

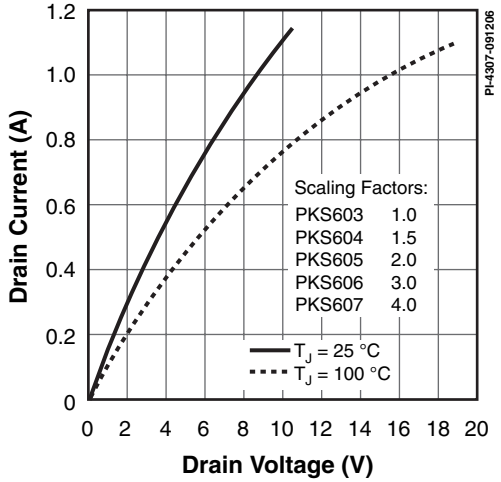


Figure 26. Output Characteristic.

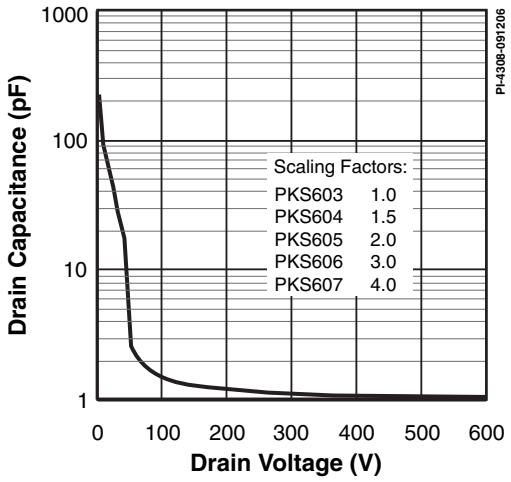


Figure 27. C_{OSS} vs. Drain Voltage.

Typical Performance Characteristics (cont.)

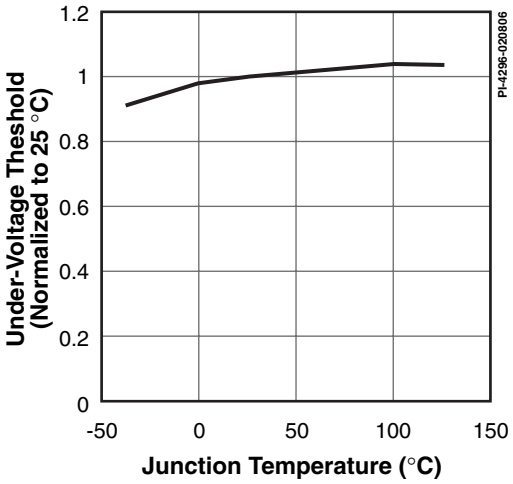


Figure 28. Under-Voltage Threshold vs. Temperature.

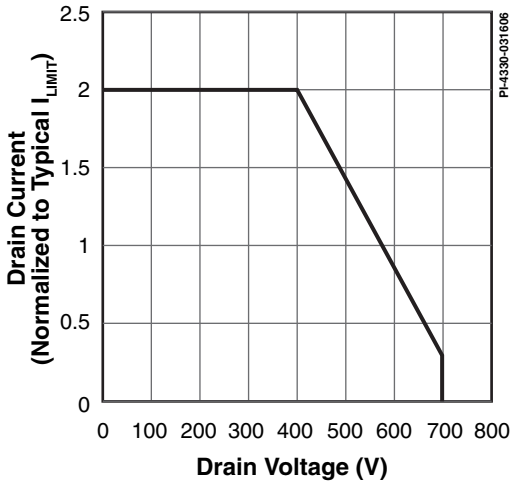
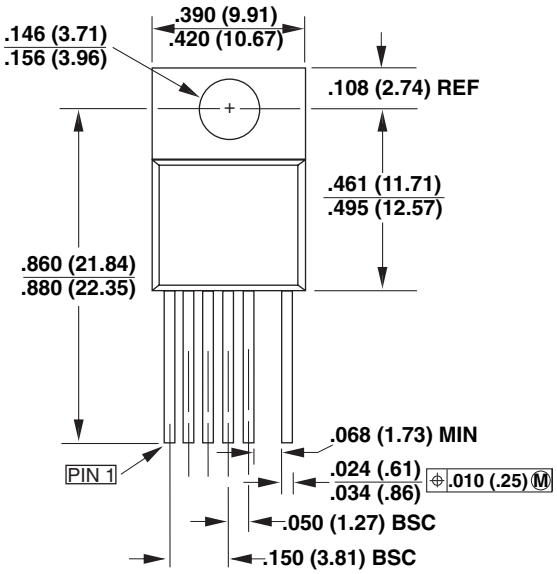


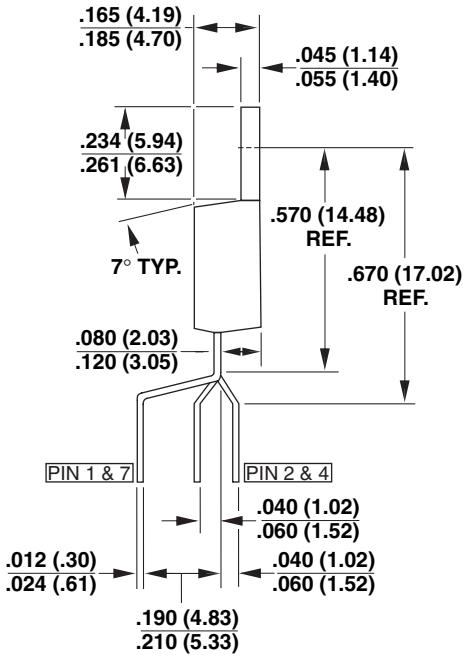
Figure 29. Maximum Allowable Drain Current vs. Drain Voltage.

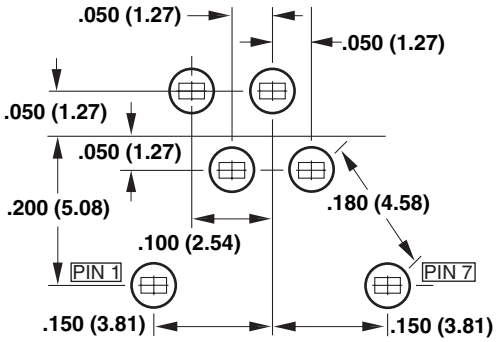
PART ORDERING INFORMATION

PKS 604 P N	***PeakSwitch* Product Family**	
	Series Number	
	Package Identifier	
	P	Plastic DIP-8C
	Y	Plastic TO-220-7C
	F	Plastic TO-262-7C
	Lead Finish	
	N	Pure Matte Tin (Pb-Free)

TO-220-7C







Y07C MOUNTING HOLE PATTERN

Notes:

1. Controlling dimensions are inches. Millimeter dimensions are shown in parentheses.
2. Pin numbers start with Pin 1, and continue from left to right when viewed from the front.
3. Dimensions do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15mm) on any side.
4. Minimum metal to metal spacing at the package body for omitted pin locations is .068 in. (1.73 mm).
5. Position of terminals to be measured at a location .25 (6.35) below the package body.
6. All terminals are solder plated.

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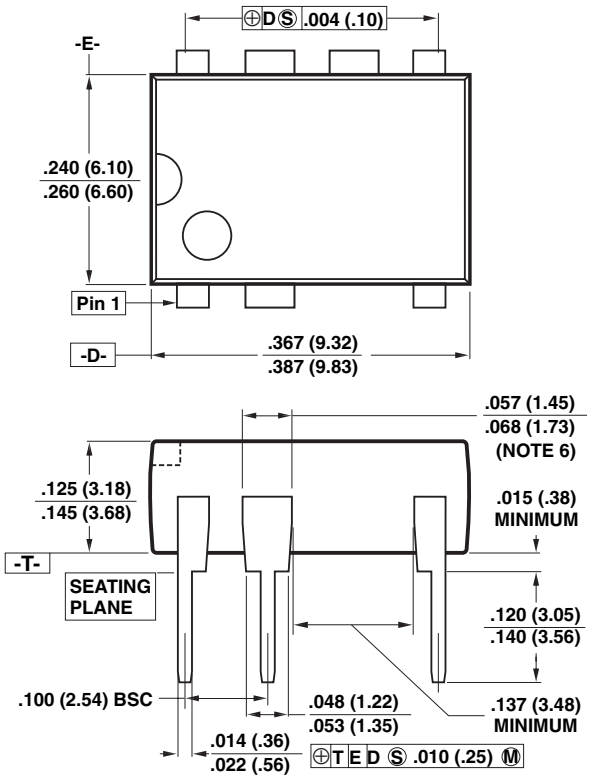
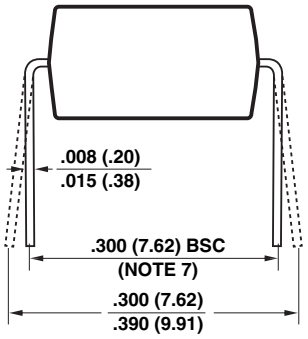
DIP-8C



Notes:

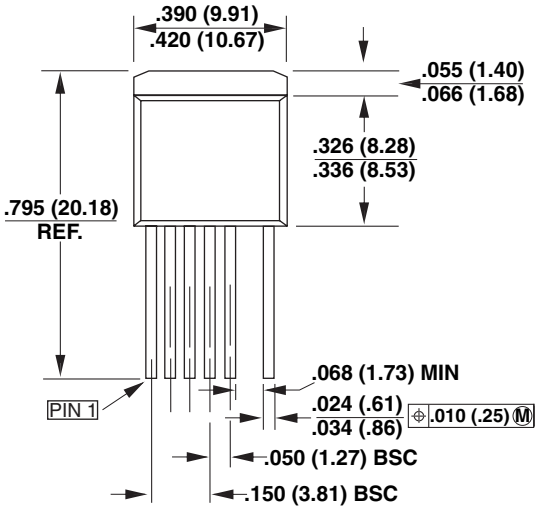
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.

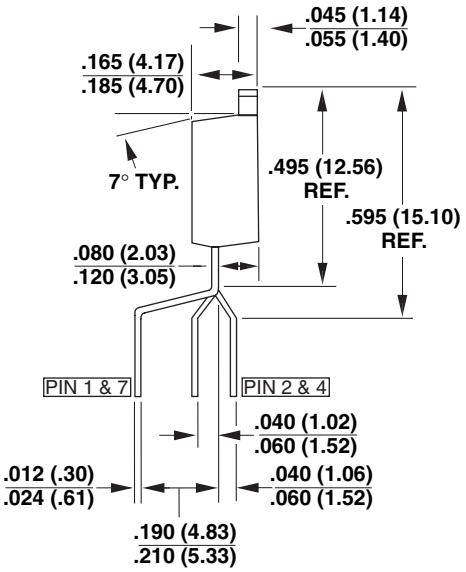


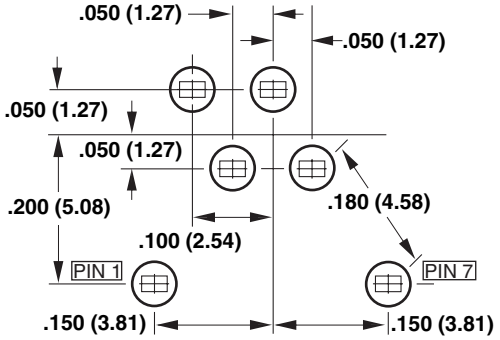
P08C

PI-3933-100504

TO-262-7C







F07C MOUNTING HOLE PATTERN

Notes:

1. Controlling dimensions are inches. Millimeter dimensions are shown in parentheses.
2. Pin numbers start with Pin 1, and continue from left to right when viewed from the front.
3. Dimensions do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15mm) on any side.
4. Minimum metal to metal spacing at the package body for omitted pin locations is .068 inch (1.73 mm).
5. Position of terminals to be measured at a location .25 (6.35) below the package body.
6. All terminals are solder plated.

PI-2757-122004

Revision	Notes	Date
F	1) Final Release Data Sheet.	3/06
G	Revised device symbol in Figures 1 and 15 to be consistent with other PI documentation (added second ground connection). Revised layout of Figure 17 (PI-4326).	4/06
H	Revised grounding in Figure 1 to match actual implementation.	6/06
I	Added PKS607.	8/06

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