TPS55010 具有集成 FET 的 2.95V 至 6V 输入、2W 隔离式 DC/DC 转换器

1 特性

- 隔离式 Fly-Buck™拓扑
- 一次侧反馈
- 开关频率：100kHz 至 2000kHz
- 与外部时钟同步
- 可调节缓启动
- 可调输入电压欠压闭锁 (UVLO)
- 漏极开路故障输出
- 逐周期电流限制
- 热关断保护
- 3 mm x 3 mm 16 引脚 QFN 封装

2 应用

- PLC 抗噪、数据采集和测量设备
- 隔离式 RS-232 和 RS-485 通信通道
- 为线路驱动器、ISO 放大器、传感器、CAN 收发器供电
- 为 IGBT 栅极驱动器提供浮动式电源
- 提升医疗设备安全性

3 说明

TPS55010 是一款用于为隔离式接口（例如，RS-485 和 RS-232）提供 3.3V 或 5V 隔离输入电源的变压器驱动器。

该器件使用固定频率电流模式控制和具有一次侧反馈的半桥功率级，可稳定高达 2W 功耗级别的输出电压。开关频率可在 100kHz 至 2000kHz 范围内调节，因此可以优化解决方案的尺寸、效率和抗噪性能。开关频率由电阻器设置，或通过 RT/CLK 引脚与外部时钟同步。为了最大限度减少浪涌电流，可以向 SS 引脚上连接一个小电容器。可以使用 EN 引脚作为启用引脚或用于在 2.6V 的基础上提高默认的输入 UVLO 电压。

通过使用同款变压器，TPS55010 可调整一次侧电压，为不同的输入和输出电压组合提供解决方案。现有的变压器可提供单路正输出电压、双路正输出电压和双路负输出电压。

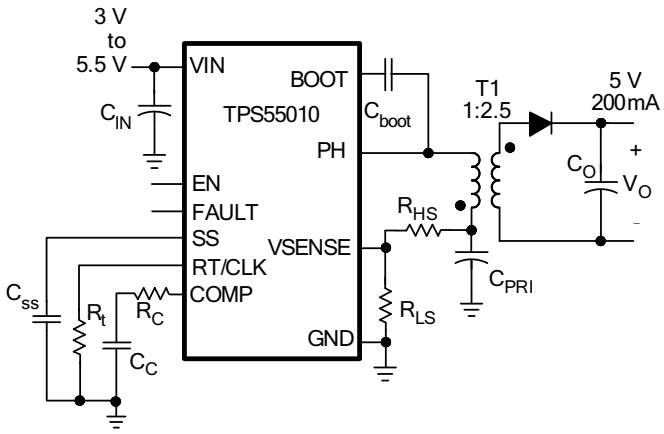
TPS55010 采用 3mm x 3mm 16 引脚、带散热焊盘的 QFN 封装。

器件信息 (1)

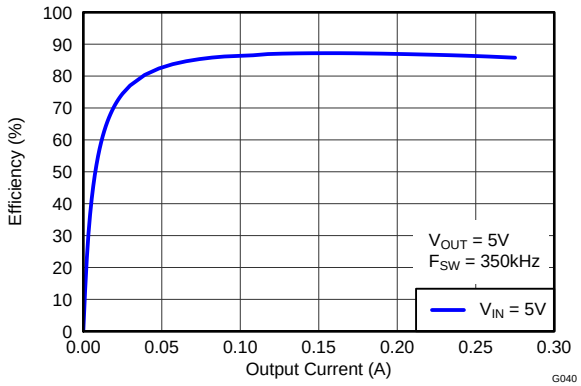
部件号	封装	封装尺寸（标称值）
TPS55010	WQFN (16)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

4 简化电路原理图



效率与负载电流间的关系



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (June 2011) to Revision B **Page**

- 已更改 已添加“器件信息”表，“处理额定值”表， “应用 和实施”部分，“布局”部分以及“器件和文档支持”部分 ... 1
- Added the Handling Rating table ... 4
- Added the Recommended Operating Conditions table ... 4
- Added Figure 23 ... 23
- Added Figure 24 ... 24
- Changed Figure 26 through Figure 28 ... 26
- Changed Figure 40 ... 27
- Changed Figure 42 through Figure 44 ... 34
- Changed Figure 54 ... 35

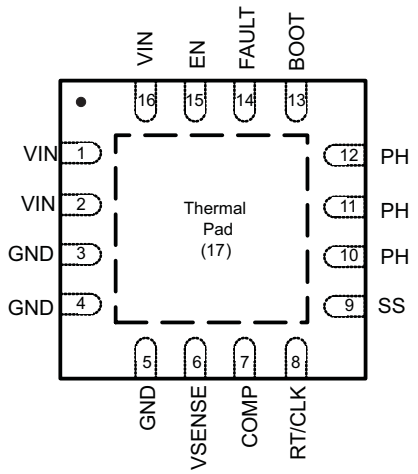
Changes from Original (April 2010) to Revision A **Page**

- 已将器件状态从“产品预览”改为“量产数据” ... 1

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6 Pin Configuration and Functions

RTE PACKAGE
(TOP VIEW)



Pin Functions

Name	Number	Description
VIN	1, 2, 16	Supplies the control circuitry and switches of the power converter.
GND	3, 4, 5	Power Ground. This pin should be electrically connected directly to the thermal pad under the IC.
VSENSE	6	Inverting node of the transconductance error amplifier.
COMP	7	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
RT/CLK	8	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
SS	9	Slow-start. An external capacitor connected to this pin sets the output rise time.
PH	10, 11, 12	The source of the internal high side power MOSFET, and drain of the internal low side MOSFET.
BOOT	13	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
FAULT	14	An open drain output. Active low if the output voltage is low due to thermal shutdown, dropout, overvoltage or EN shut down.
EN	15	Enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
THERMAL PAD	17	GND pin should be connected to the exposed thermal pad for proper operation. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

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7 Specifications

7.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VIN	–0.3	7	V
	EN	–0.3	3.6	V
	BOOT		PH + 7	V
	VSENSE	–0.3	3	V
	COMP	–0.3	3	V
	FAULT	–0.3	7	V
	SS	–0.3	3	V
	RT/CLK	–0.3	6	V
	BOOT-PH	–0.3	7	V
	PH	–0.6	7	V
	PH, 10ns Transient	–2	10	V
Current	EN		100	µA
	RT/CLK		100	µA
	COMP		100	uA
	FAULT		10	mA
	SS		100	µA
Operating Junction Temperature		–40	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ELECTRICAL SPECIFICATIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Rating

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
T_{stg}	Storage Temperature		–65	150	°C
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.98		6	V
P_O	Output power			2	W

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7.4 Thermal Information

THERMAL METRIC(1)		TPS55010 RTE (16 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	60	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	55.5	
θ_{JB}	Junction-to-board thermal resistance	24.9	
ψ_{JT}	Junction-to-top characterization parameter	1.0	
ψ_{JB}	Junction-to-board characterization parameter	24.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	9.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C TO 150°C, VIN = 2.95V TO 6V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE					
Operating input voltage	VIN	2.95		6	V
Shutdown current	EN = 0V, 25°C		2	5	µA
Operating current	VSENSE = 0.9V, 25°C		360	575	µA
Internal undervoltage lockout			2.6	2.9	V
ENABLE					
Enable threshold	rising		1.25	1.37	V
	falling	1.15	1.18		
Input current	Threshold - 50mV		–1.2		µA
	Threshold + 50mV		–4.6		µA
Hysteresis			3.4		
VOLTAGE REFERENCE					
Reference	3V < VIN < 6V	0.804	0.829	0.854	V
MOSFET					
High side switch resistance	BOOT- PH = 5 V		45	81	mΩ
Low side switch resistance	VIN = 5 V		45	81	mΩ
ERROR AMPLIFIER					
Input current			50		nA
Error amp transconductance	-2 µA < $I_{(COMP)}$ < 2 µA		245		uS
Error amp dc gain	VSENSE = 0.8 V		500		V/V
Minimum unity gain Bandwidth			3		MHz
Error amp source/sink	$V_{(COMP)}$ = 1V, 100 mV overdrive		±16		µA
COMP to Iph gm	$I_{(PH)}$ = 0.5 A		7.5		A/V
CURRENT LIMIT					
High side sourcing current limit	VIN = 3 V	2	2.75		A
Low Side Sinking Current Limit	VIN = 3 V	–3	–4.5		A
THERMAL SHUTDOWN					
Thermal Shutdown			171		°C
OT Hysteresis			12		°C

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Electrical Characteristics (continued)

T_J = –40°C TO 150°C, VIN = 2.95V TO 6V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
RT/CLK					
RT/CLK voltage	$R_{(RT/CLK)}$ = 195 kΩ		0.5		V
RT/CLK high threshold			1.6	2.2	V
RT/CLK low threshold		0.4	0.6		V
BOOT					
Boot UVLO			2.5		V
SS Slow Start					
Charge current	$V_{(SS)}$ = 0.4 V	0.5	2.2	4	µA
SS to VSENSE matching	$V_{(SS)}$ = 0.4 V		35		mV
SS to reference Crossover	98% reference		1.1		V
SS discharge current (overload)	VSENSE = 0 V		325		µA
SS discharge voltage	VSENSE = 0V		46		mV
SS discharge current (UVLO, EN, thermal fault)	$V_{(SS)}$ = 0.5 V		1.2		mA
VIN UVLO to SS start time			100		µs
FAULT Pin					
VSENSE threshold	VSENSE falling		91		% VREF
	VSENSE rising		108		% VREF
Output high leakage	VSENSE = V_{REF}, $V_{(FAULT)}$ = 5.5 V		2		nA
Output low	$I_{(FAULT)}$ = 3 mA		0.3		V
Minimum VIN for valid output	$V_{(FAULT)}$ < 0.5 V at 100 µA			1.6	V

7.6 Timing Requirements

		MIN	TYP	MAX	UNIT
RT/CLK					
Minimum CLK pulse width			75		ns

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PH						
t_{on}	Minimum on time	Measured at 10% to 10% of VIN		130		ns
t_{off}	Minimum off time	$V_{(BOOT-PH)}$ ≥ 3 V		0%		
RT/CLK						
	Switching frequency using CLK mode		300		2000	kHz
	Switching frequency using RT mode		100		2000	kHz
	Switching Frequency	$R_{(RT/CLK)}$ = 195 kΩ	400	500	600	kHz
	PLL lock in time			50		µs
	RT/CLK falling edge to PH rising edge delay			90		ns
SS Slow Start						
	VIN UVLO to SS start time			100		µs

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7.8 Typical Characteristics

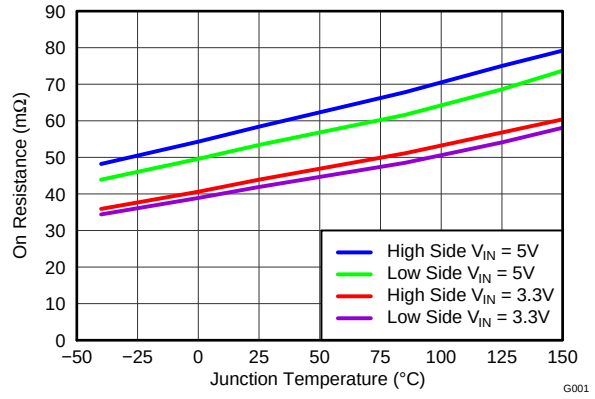


Figure 1. High Side and Low Side $R_{DS(on)}$ vs Temperature

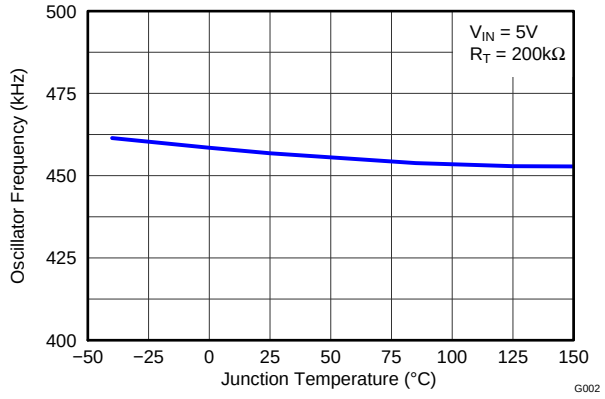


Figure 2. Frequency vs Temperature

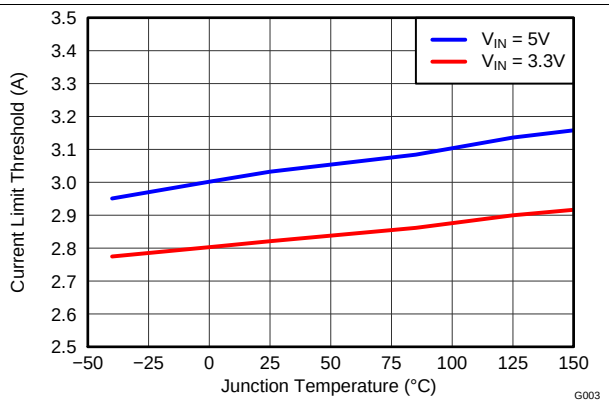


Figure 3. High Side Current Limit (Sourcing) vs Junction Temperature

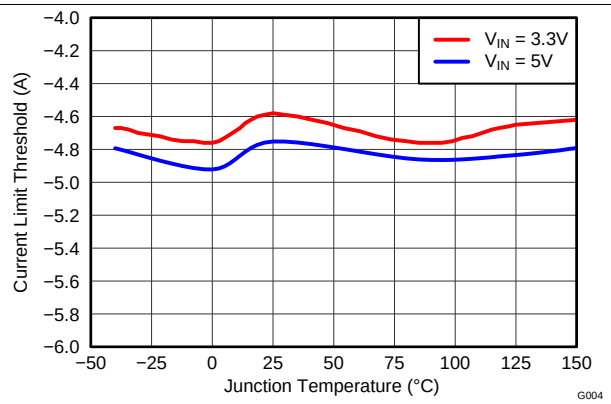


Figure 4. Low Side Current Limit (Sinking) vs Junction Temperature

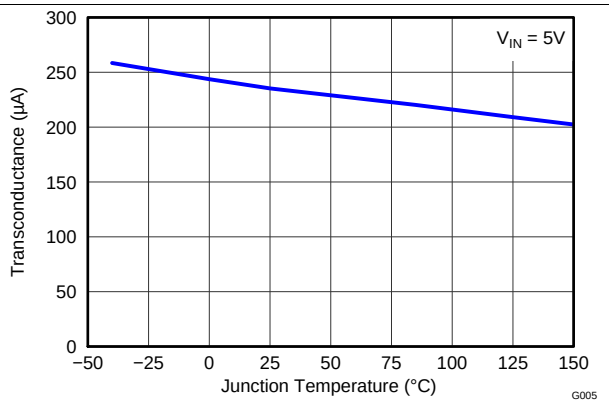


Figure 5. Error Amplifier Transconductance vs Temperature

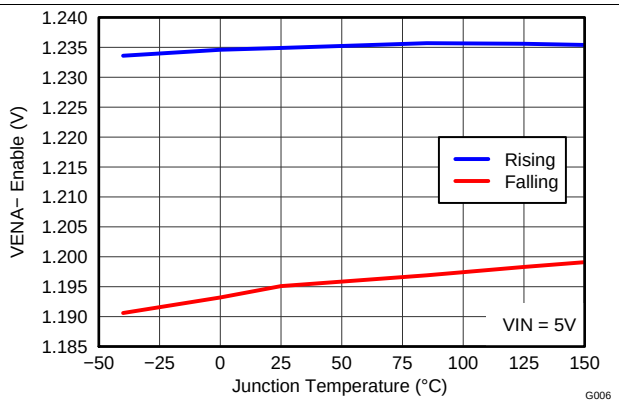


Figure 6. EN Pin Voltage vs Temperature

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Typical Characteristics (continued)

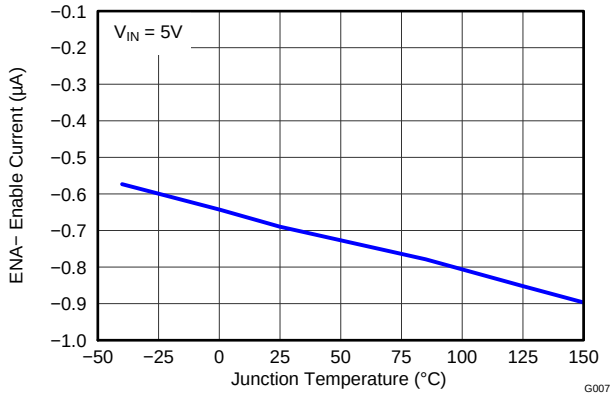


Figure 7. EN Pin Pullup vs Temperature (V_{EN} = Threshold -50 mV)

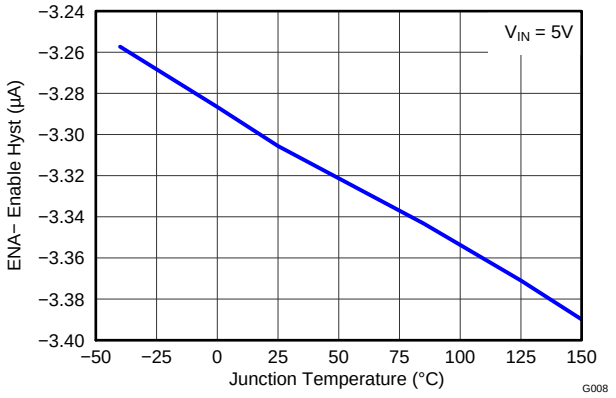


Figure 8. EN Pin Hysteresis Current vs Temperature

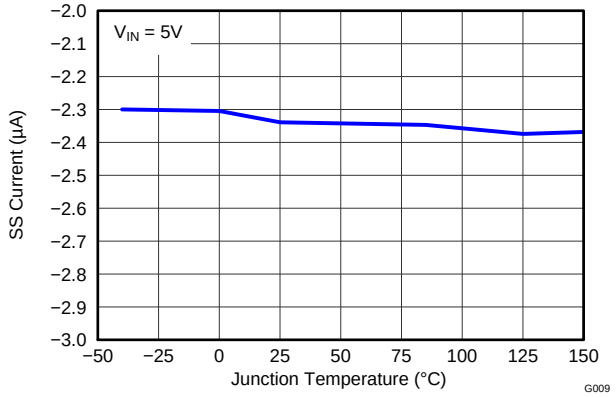


Figure 9. SS Charge Current vs Temperature

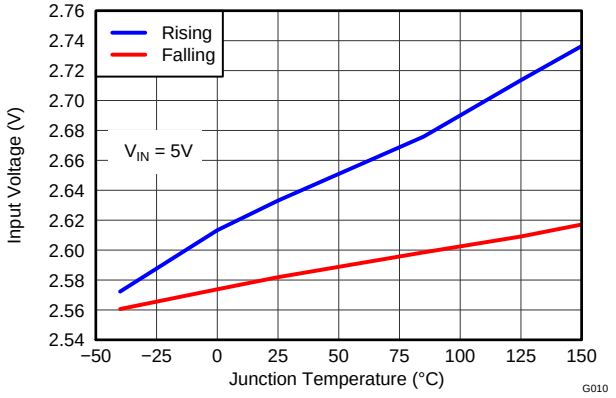


Figure 10. Input Start and Stop Voltage vs Temperature

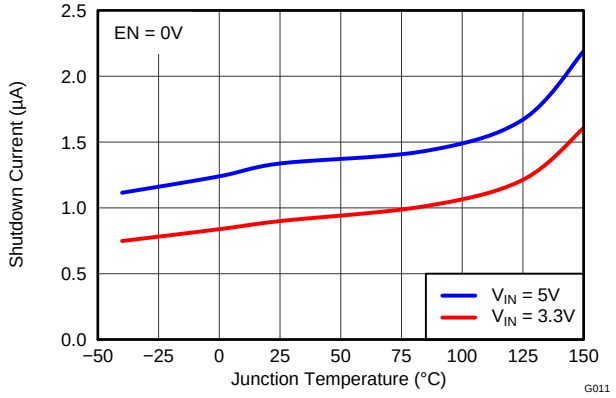


Figure 11. Shutdown Supply Current vs Temperature

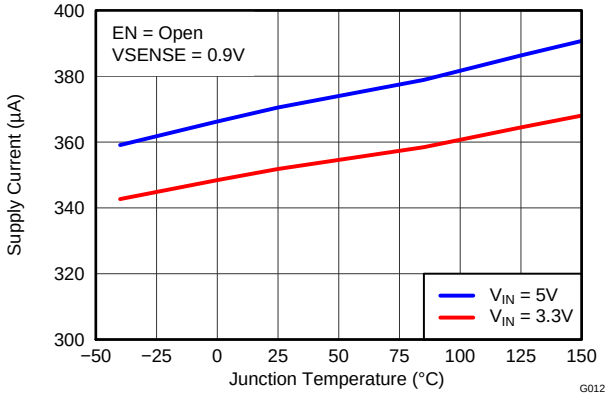


Figure 12. VIN Supply Current vs Temperature

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Typical Characteristics (continued)

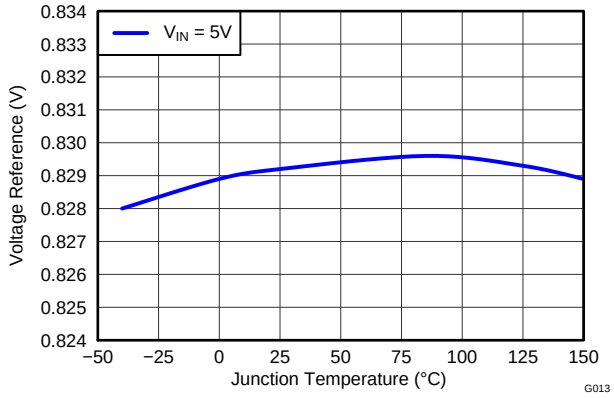


Figure 13. Voltage Reference vs Temperature

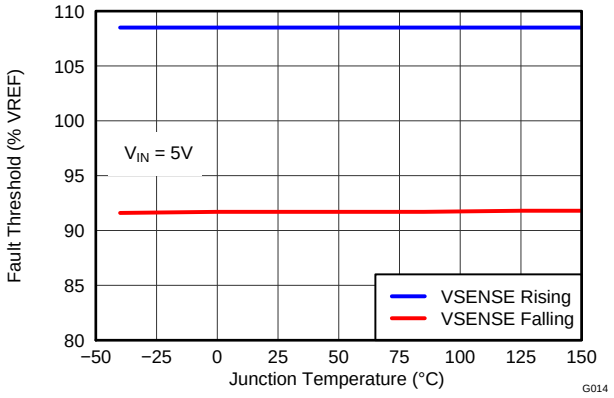


Figure 14. Fault Threshold vs Temperature

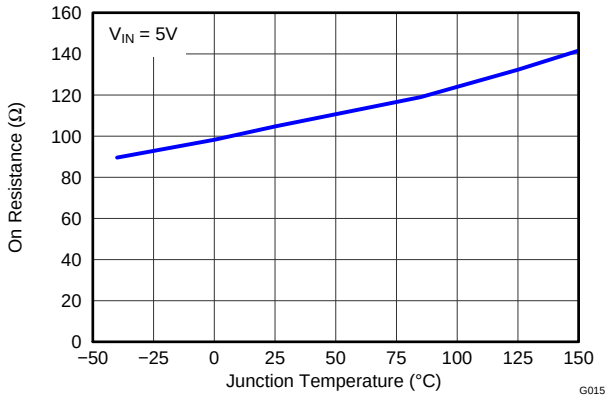


Figure 15. Fault On-Resistance vs Temperature

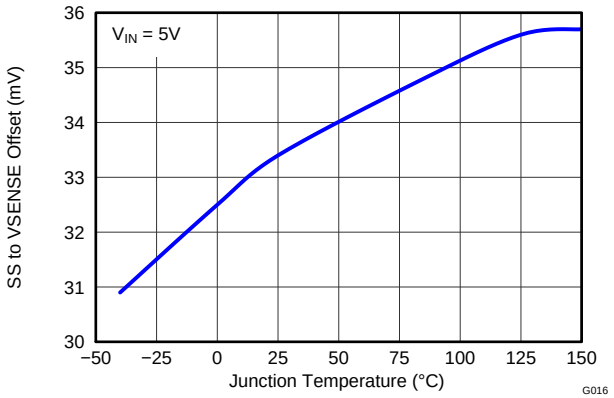


Figure 16. SS to VSENSE Offset vs Temperature

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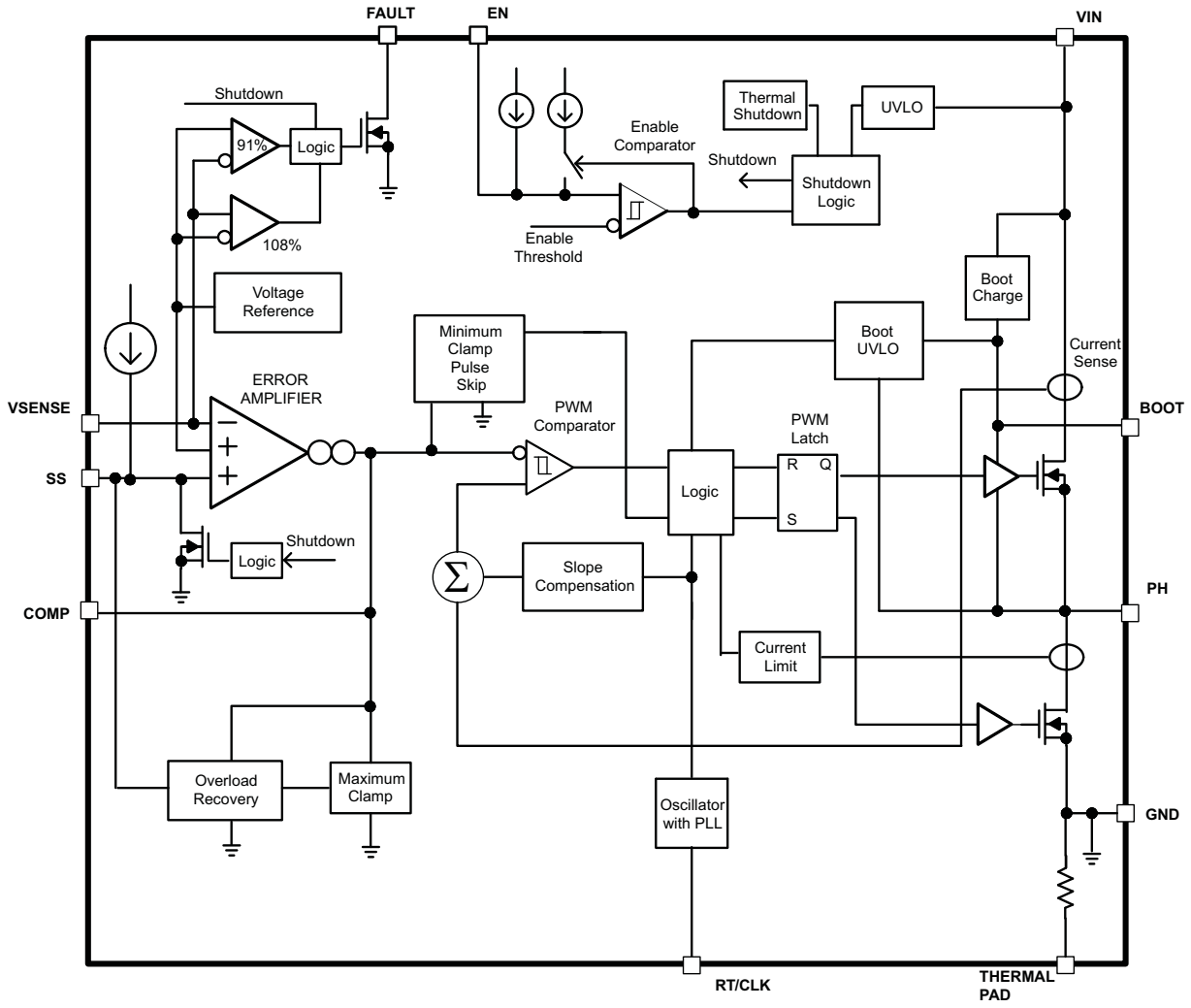
8 Detailed Description

8.1 Overview

The TPS55010 is a half bridge transformer driver designed to implement a high efficiency, low power isolated supply. The primary side feedback implemented using two resistors and a primary side capacitor provides excellent regulation over line and load compared to an open loop push pull converter.

The half bridge power stage consists of two integrated n-channel MOSFETs with 45 mΩ on resistance. The drive voltage for the integrated high side MOSFET is supplied by a capacitor between the BOOT and PH pins. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the high side power switch turn on to a falling edge of an external system clock. The wide switching frequency of 100 kHz to 2000 kHz (300kHz to 2000kHz in CLK mode) allows for efficiency, size optimization or noise avoidance when selecting the switching frequency. The TPS55010 has a typical default start up voltage of 2.6 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS55010 is typically 360 µA when not switching and under no load. When the device is disabled, the supply current is less than 5 µA. The slow start (SS) pin is used to minimize inrush currents during start up.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The TPS55010 uses an adjustable fixed frequency, peak current mode control. The primary voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The TPS55010 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases.

8.3.2 Half Bridge and Bootstrap Voltage

The TPS55010 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

8.3.3 Error Amplifier

The TPS55010 uses a transconductance error amplifier. The amplifier compares the VSENSE voltage to the lower of the SS pin voltage or the internal 0.829 V voltage reference. The transconductance of the error amplifier is 245 µA/V. The frequency compensation components are placed between the COMP pin and ground.

8.3.4 Voltage Reference

The voltage reference system produces a precise ±3.0% voltage reference over temperature by scaling the output of a temperature-stable band gap circuit. The band gap and scaling circuits produce 0.829 V at the non-inverting input of the error amplifier.

8.3.5 Adjusting the Output Voltage

The primary side voltage is set with a resistor divider from the primary side capacitor to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10 kΩ for the R_{LS} resistor and use Equation 1 to calculate R_{HS}. The output voltage is a function of the primary voltage, transformer turns ratio and forward voltage of the diode.

$$R_{HS} = R_{LS} \times \left(\frac{V_{PRI} - 0.829V}{0.829V} \right) \quad (1)$$

$$V_{OUT} = V_{PRI} \times \frac{N_{SEC}}{N_{PRI}} - V_{fd} \quad (2)$$

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Feature Description (continued)

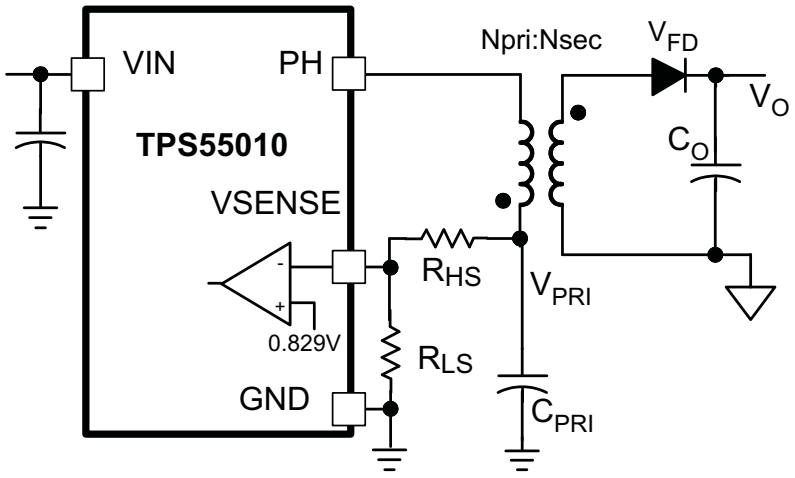


Figure 17. Setting the Output Voltage

8.3.6 Enable and Adjusting Undervoltage Lockout

The TPS55010 is disabled when the VIN pin voltage falls below 2.6 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 18 to adjust the input voltage UVLO by using two external resistors. The EN pin has an internal pull-up current source of 1.2 µA that provides the default condition of the TPS55010 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 3.4 µA of hysteresis is added. When the EN pin is pulled below 1.18 V, the hysteresis current is removed.

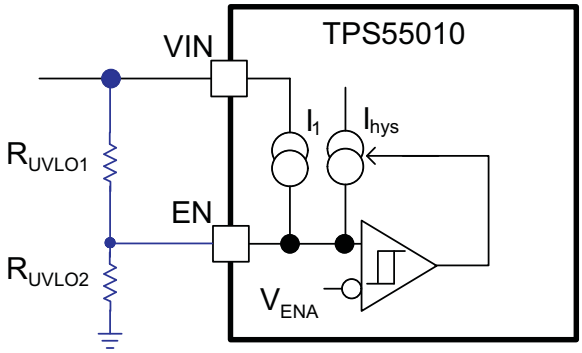


Figure 18. Adjustable Under Voltage Lock Out

$$R_{UVLO1} = \frac{V_{START}\left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I1 \times \left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_{HYS}} \quad (3)$$

$$R_{UVLO2} = \frac{R_{UVLO1} \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_{UVLO1} \times \left(I1 + I_{HYS}\right)} \quad (4)$$

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Feature Description (continued)

8.3.7 Adjusting Slow Start Time

A capacitor on the SS pin to ground implements a slow start time to minimize inrush current during startup. The TPS55010 regulates to the lower of the SS pin and the internal reference voltage. The TPS55010 has an internal pull-up current source of 2.2 µA which charges the external slow start capacitor. Equation 5 calculates the required slow start capacitor value where T_{SS} is the desired slow start time in ms, Iss is the internal slow start charging current of 2.2 µA, and V_{REF} is the internal voltage reference of 0.829 V.

If during normal operation, the VIN goes below the UVLO, EN pin pulled below 1.18 V, or a thermal shutdown event occurs, the TPS55010 stops switching. When the VIN goes above UVLO, EN is released or pulled high, or a thermal shutdown is exited, then SS is discharged to below 40 mV before reinitiating a powering up sequence. The VSENSE voltage will follow the SS pin voltage with a 35 mV offset up to 85% of the internal voltage reference. When the SS voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS voltage to the internal voltage reference. If no slow start time is needed, the SS pin can be left open. The slow start capacitor should be less than 0.47 µF.

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(uA)}{V_{REF}(V)} \quad (5)$$

8.3.8 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS55010 is adjustable over a wide range from 100 kHz to 2000 kHz by placing a maximum of 1070 kΩ and minimum of 42.2 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use Equation 6.

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 130 ns.

$$R_T(k\Omega) = \frac{156000}{f_{sw}(kHz)^{1.0793}} \quad (6)$$

8.3.9 How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through one of the circuit networks shown in Figure 19. The square wave amplitude must transition lower than 0.4V and higher than 2.2V on the RT/CLK pin and have a high time greater than 75 ns. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin signal.

The external synchronization circuit should be designed in such a way that the device has the default frequency set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 19 through another resistor (e.g 50 Ω) to ground for clock signal that are not Hi-Z or tri-state during the off state. The RT resistor value should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10 pF ceramic capacitor to RT/CLK pin. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5 V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Since there is a PLL on the regulator the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then will increase or decrease the switching frequency until the PLL locks onto the external CLK frequency within 50 microseconds. When the device transitions from the PLL to resistor mode the switching frequency will slow down from the CLK frequency to 150 kHz, then reapply the 0.5V voltage and the resistor will then set the switching frequency.

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Feature Description (continued)

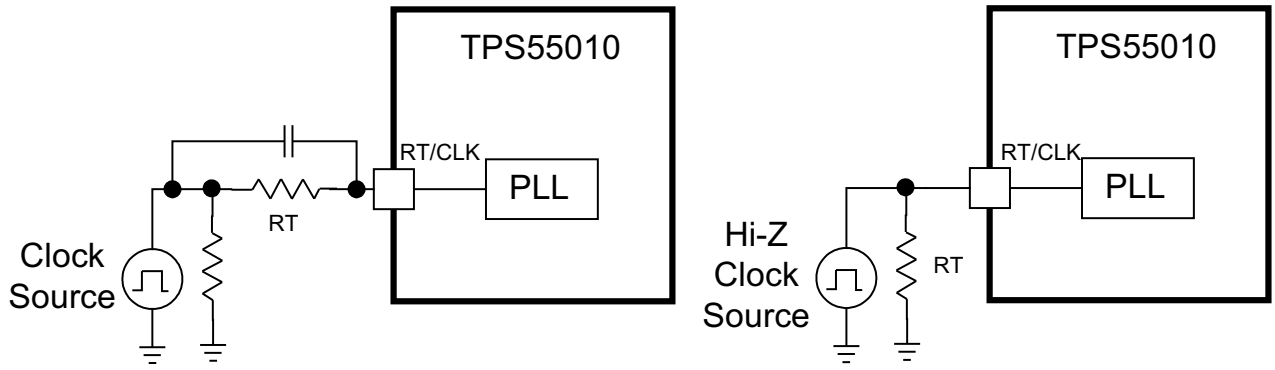


Figure 19. Synchronizing to a System Clock

8.3.10 Overcurrent Protection

The TPS55010 implements a cycle by cycle current limit. During each switching cycle the high side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

8.3.11 Reverse Overcurrent Protection

The TPS55010 implements low side current protection by detecting the voltage across the low side MOSFET. When the converter sinks current through its low side FET, the control circuit turns off the low side MOSFET if the reverse current is more than 4.5 A

8.3.12 FAULT Pin

The FAULT pin output is an open drain MOSFET. The output is pulled low when the VSENSE voltage is below 91% or rising above 108% of the nominal internal reference voltage. It is recommended to use a pull-up resistor between the values of 1kΩ and 100kΩ to a voltage source that is 6 V or less. The FAULT pin is in a valid state once the VIN input voltage is greater than 1.6 V. The FAULT pin is pulled low, if the input UVLO or thermal shutdown is asserted, or the EN pin is pulled low.

8.3.13 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 171°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 159°C, the device reinitiates the power up sequence by discharging the SS pin to below 40 mV. The thermal shutdown hysteresis is 12°C.

8.4 Device Functional Modes

8.4.1 Operation of the Fly-Buck™ Converter

Figure 20 shows a simplified schematic and the two primary operational states of the Fly-Buck converter. The power supply is a variation of a Flyback converter and consists of a half bridge power stage S_{HS} and S_{LS}, transformer, primary side capacitor, diode and output capacitor. The output voltage is regulated indirectly by using the primary side capacitor voltage, V_{PRI}, as feedback. The Fly-Buck is a portmanteau of flyback and buck since the transformer is connected as a flyback converter and the input to output voltage relationship is similar to a buck derived converter, assuming the converter is operating in steady state and the transformer has negligible leakage inductance.

The C_{PRI} and L_{PRI} are charged by the input voltage source VIN during the time the high side switch S_{HS} is on. During this time, diode D1 is reversed biased and the load current is supplied by output capacitor C_O.

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Device Functional Modes (continued)

During the off time of S_{HS}, S_{LS} conducts and the voltage on C_{PRI} continues to increase during a portion of the S_{LS} conduction time. The voltage increase is due to the energy transfer from L_{PRI} to C_{PRI}. For the remaining portion of the S_{LS} conduction time, the C_{PRI} voltage decreases because of current in L_{PRI} reverses; see the IL_{PRI} and V_{PRI} waveforms in Figure 21. By neglecting the diode voltage drop, conduction dead time and leakage inductance, the input to output voltage conversion ratio can be derived as shown in Equation 7 from the flux balance in L_{PRI}. It can be seen in Equation 7 that the input to output relationship is the same as a buck-derived converter with transformer isolation. The dc voltage V_{PRI} on the primary side capacitor in Equation 8 has the same linear relationship to the input voltage as a buck converter.

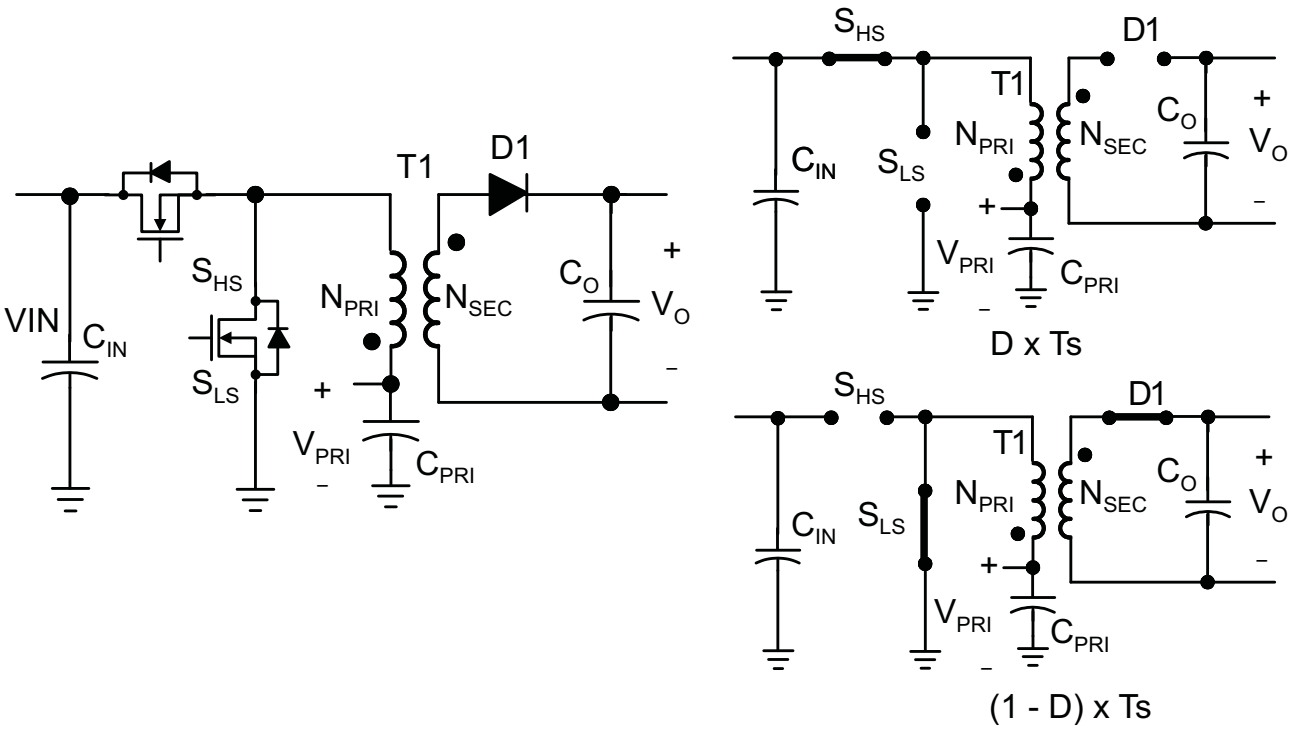


Figure 20. Output Voltage Conversion Ratio

$$\frac{V_O}{V_{IN}} = \frac{N_{SEC}}{N_{PRI}} \times D \tag{7}$$

$$\frac{V_{PRI}}{V_{IN}} = D \tag{8}$$

Device Functional Modes (continued)

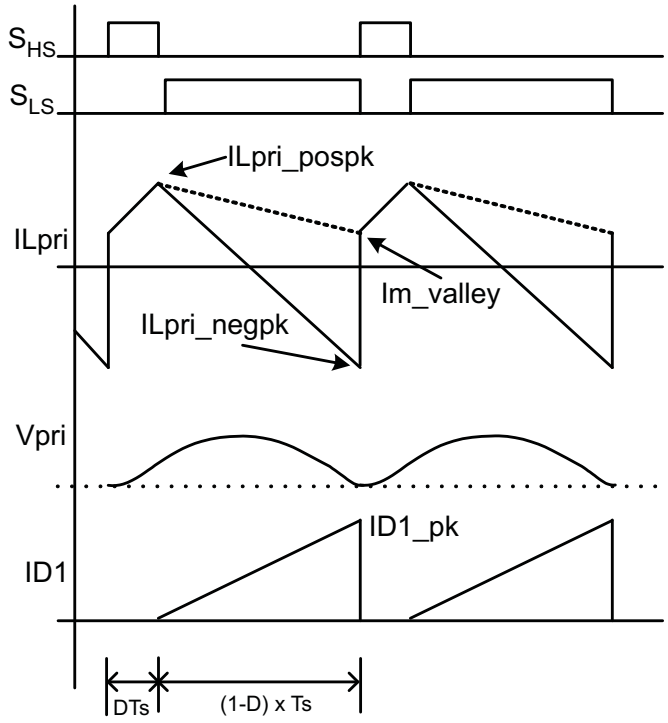


Figure 21. Simplified Voltage and Current Waveforms

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9 Application And Implementation

9.1 Application Information

The following design example illustrates how to determine the components for a single output isolated power supply. TI offers an EVM (TPS55010EVM-009) with user guide (SLVU459) and excel calculator tool (SLVC363) to expedite the design process. Additionally the PMP6813 and PMP6838 reference designs show the small solution size possible with the TPS55010. The support material is available on the TPS55010 product folder at www.ti.com.

9.2 Typical Applications

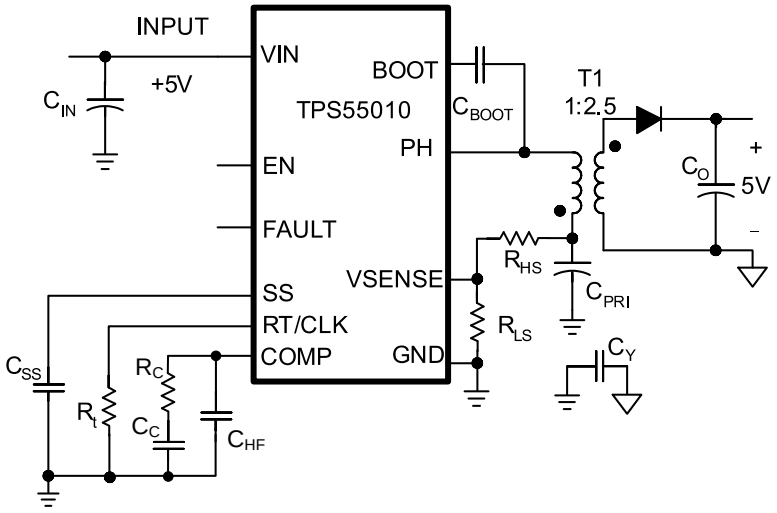


Figure 22. 5 V to 5 V Isolated Power Supply Schematic

Table 1. Reference Design for Common Applications

	5 V to 5 V at 0.2 A	3.3 V to 5 V at 0.2 A	5 V to 3.3 V at 0.3 A	3.3 V to 3.3 V at 0.3 A
C_{IN}	47 µF X5R 6.3V	100 µF X5R 6.3V	47 µF X5R 6.3V	100 µF X5R 6.3V
C_{OUT}	2 x 10 µF X5R 10V	47 µF X5R 6.3V	22 µF X5R 6.3V	47 µF X5R 6.3V
C_{PRI}	47 µF X5R 10V	100 µF X5R 6.3V	100 µF X5R 6.3V	100 µF X5R 6.3V
C_{BOOT}	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V
C_{SS}	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V	0.1 µF X5R 10V
C_{COMP}	5.6 nF	3.9 nF	3.3 nF	3.9 nF
C_{HF}	82 pF	68 pF	68 pF	100 pF
R_{COMP}	10.5 kΩ	16.9 kΩ	18.2 kΩ	17.4kΩ
R_{HS}	16.5 kΩ	16.5 kΩ	8.25 kΩ	8.25 kΩ
R_{LS}	10.0 kΩ	10.0 kΩ	10.0 kΩ	10.0 kΩ
R_T	280 kΩ (350kHz)	332 kΩ (300kHz)	402 kΩ (250kHz)	511 kΩ (200kHz)
T1 (See the SLVU459 BOM)	750311880	750311880	750311880	750311880
D1	B120	B120	B120	B120

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9.2.1 Design Guide – Step-by-Step Design Procedure

Table 2. Design Parameters

PARAMETER	VALUE
Input Voltage	5 V nominal (4.5 V to 5.5 V)
Output Voltage	5 V
Output Voltage Ripple	<0.5%
Output Current	200 mA
Start Voltage	4.5V
Stop Voltage	4V

9.2.2 Primary Side Voltage

The output voltage is a function of the primary voltage, transformer turns ratio and the diode voltage. The primary voltage is a function of the duty cycle and input voltage, and is similar to a step down (buck) regulator as shown in Equation 9. The primary side voltage must be lower than the minimum operating input voltage by 500 mV to avoid maximum duty cycle problems and allow sufficient time for energy transfer during the low side power switch on time. Typically, a primary side voltage that is 50% of the input voltage is ideal to maximize the output power, but 20% to 80% is acceptable. Using the design constraints, the primary side voltage could be from 3.6 V to 1.1 V. A 2.2 V primary side voltage is selected, and the duty cycle is approximately 45%.

$$D = \frac{V_{PRI}}{V_{IN}} \tag{9}$$

9.2.3 Voltage Feedback

9.2.3.1 Turns Ratio

The transformer turns ratio is calculated using the desired output voltage, diode voltage and the primary voltage. Assuming a diode voltage of 0.5 V, V_{OUT} of 5 V, V_{PRI} of 2.2 V yields a N_{PRI}:N_{SEC} turns ratio of 1:2.5.

$$\frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} + V_{FD}}{V_{PRI}} \tag{10}$$

Selecting 10 kΩ for the R_{LS}, R_{HS} is calculated to be 16.5 kΩ using Equation 11. Choose 100 kΩ as the nearest standard value.

It may be necessary to adjust the feedback resistors to optimize the output voltage over the full load range. Usually checking and setting the output voltage to the nominal voltage at 50% load, yields the best results.

$$R_{HS} = R_{LS} \times \left(\frac{V_{PRI} - 0.829V}{0.829V} \right) \tag{11}$$

9.2.4 Selecting the Switching Frequency and Primary Inductance

The selection of switching frequency is usually a trade-off between efficiency and component size. However, when isolation is a requirement, switching frequency is not the key variable in determining solution size. Low switching frequency operation improves efficiency by reducing gate drive losses and MOSFET and diode switching losses. However, a lower switching frequency operation requires a larger primary inductance which will have more windings and higher dc resistance.

The optimal primary inductance should be selected between two inductance values, $L_{PRI(MAX)}$ and $L_{PRI(MIN)}$. The primary inductance should be less than $L_{PRI(MAX)}$ for zero voltage switching to improve efficiency and greater than $L_{PRI(MIN)}$ to avoid the peak switch current from exceeding the high side power switch current limit. The recommended minimum and maximum inductance are calculated with Equation 12 and Equation 13. For low output power applications these design equations can suggest too large of an inductance resulting in a small magnetizing current ripple. The ripple current is part of the PWM control system, so the peak-to-peak magnetizing ripple current should be kept above 400 mA for stable and dependable operation. To keep the magnetizing ripple current above 400 mA, make sure the primary inductance value does not exceed the value

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calculated in Equation 14. Once the primary inductance is selected, check against the low side current limit using the Equation 16 and the high side current limit. For this design example, the switching frequency is selected to be 350 kHz. Using Equation 6, the resistor value is 280 kΩ. $L_{PRI(MAX)}$ and $L_{PRI(MIN)}$ are calculated to be 3.5 µH and 1.2 µH respectively assuming a current limit of 2 A. The maximum inductance using Equation 14 to ensure the magnetizing ripple current is high enough is 8.8 µH. Selecting a primary inductance of the 2.5 µH, the positive and negative peak current are calculated as 1.20 A and -1.99 A in the primary which do not exceed the current limits of the power switch. The rms currents can be calculated and used to determine the power dissipation in the device.

The magnetizing ripple current is calculated as 1.41 A using Equation 17. The highside FET and lowside FET rms currents are calculated as 0.43 A and 0.61 A, respectively using Equation 18 and Equation 19. The sum of these currents, i.e. 1.04 A is the primary side rms current for the magnetics.

$$L_{PRI(MAX)} = \frac{V_{IN} \times D \times (1 - D)}{2 \times \frac{N_{SEC}}{N_{PRI}} \times I_{OUT} \times f_{sw}} \tag{12}$$

$$L_{PRI(MIN)} = \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{sw} \times \left(I_{HSCL} - I_{OUT} \times \frac{N_{SEC}}{N_{PRI}} \right)} \tag{13}$$

$$L_{PRI(MAX)} = \frac{(V_{IN} - V_{PRI}) \times D}{0.4A \times f_{sw}} \tag{14}$$

$$ILpri_pospk \approx I_{OUT} \frac{N_{SEC}}{N_{PRI}} + \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{sw} \times L_{OPRI}} \tag{15}$$

$$ILpri_negpk \approx - I_{OUT} \frac{N_{SEC}}{N_{PRI}} \times \left(\frac{1 + D}{1 - D} \right) - \frac{V_{IN} \times D \times (1-D)}{2 \times f_{sw} \times L_{OPRI}} \tag{16}$$

$$Im_ripple = \frac{V_{IN} \times D \times (1 - D)}{f_{sw} \times L_{OPRI}} \tag{17}$$

$$Ihs_rms \approx \left(D \times \left(I_{OUT} \frac{N_{SEC}}{N_{PRI}} \right)^2 + \frac{D}{12} \times Im_ripple^2 \right)^{\frac{1}{2}} \tag{18}$$

$$Ils_rms \approx \left(\frac{3 \times D\text{-}1}{3 \times (1\text{-}D)} \times \left(I_{OUT} \times \frac{N_{SEC}}{N_{PRI}} \right)^2 + \frac{Im_ripple \times I_{OUT} \times N_{SEC}}{3 \times N_{PRI}} + \frac{1 - D}{12} \times Im_ripple^2 \right)^{\frac{1}{2}} \tag{19}$$

$$ILrms \approx IHS_rms + ILS_rms \tag{20}$$

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9.2.5 Primary Side Capacitor

The ΔV_{PRI} voltage should be less than 2% of V_{PRI}. The rated RMS current of C_{PRI} should be greater than Equation 21. For this design example, assuming the ΔV_{PRI} is 0.044 V, the primary side capacitance is 24 µF and the rms current is 1.04 A. A 47 µF/6.3 V X5R ceramic capacitor is used.

$$I_{CPRI_rms} = ILrms \tag{21}$$

$$I_{CPRI_ch} \approx IL_{CPRI_}pospk \times \sqrt{\frac{D + (1 - D) \times \frac{IL_{PRI_}pospk}{IL_{PRI_}pospk - IL_{PRI_}negpk}}{3}} \tag{22}$$

$$t_{CPRI} \approx \frac{D}{f_{SW}} + \frac{(1 - D)}{f_{SW}} \times \frac{IL_{PRI_}pospk}{IL_{PRI_}pospk - IL_{PRI_}negpk} \tag{23}$$

$$C_{PRI} = \frac{I_{CPRI_ch} \times t_{CPRI}}{\Delta V_{PRI}} \tag{24}$$

9.2.6 Secondary Side Diode

The diode should be selected to handle the voltage stress and rms current calculated in Equation 25 and Equation 26. Typically, a low duty cycle or high turns ratio design will have a larger voltage stress on the diode. At the maximum input voltage of 5.5V, the Vdiode_max voltage is calculated at 13.3 V. The rms current is calculated as 0.31 A. The diode peak current is 0.71 A using Equation 27 and the power dissipated in the diode is 0.1 W. The B120 diode is used which is rated for 20 V and 1 A.

$$Vdiode_max = \left(V_{IN} - V_{PRI}\right) \times \frac{N_{SEC}}{N_{PRI}} + V_{OUT} \tag{25}$$

$$Idiode_rms = 2 \times I_{OUT} \times \left(\frac{1}{3 \times (1 - D)}\right)^{\frac{1}{2}} \tag{26}$$

$$Idiode_peak = 2 \times \frac{I_{OUT}}{1 - D} \tag{27}$$

$$Pdiode = V_{fd} \times I_{OUT} \tag{28}$$

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9.2.7 Secondary Side Capacitor

The ΔV_{CO} voltage should be 0.25% to 1% of V_{CO} voltage. The converter transfers energy each switching period to the secondary, since the converter has primary side feedback, at light or no load conditions the output voltage may rise above the desired output. If the application will experience a no load condition, attention to the capacitor voltage ratings should be considered. Adding a ballast load, zener diode or linear regulator can help prevent the overvoltage at light or no load.

The output capacitance is calculated to be 10.1 µF using Equation 29 and the rms current is 0.24 A.

Two 10 µF/10V X5R ceramic capactors are used. The effective capacitance is lower than the 20 µF, because of dc voltage bias.

$$C_O = \frac{I_{OUT} \times D}{f_{SW} \times \Delta V_{CO}} \tag{29}$$

$$IC_{O_}rms = \sqrt{Idiode_rms^2 - I_{OUT}^2} \tag{30}$$

9.2.8 Input Capacitor

The ΔV_{CIN} voltage should be 0.25% to 1% of V_{IN}. The TPS55010 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 2.2 µF of effective capacitance or larger coupled to VIN and GND pins and in some applications additional bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. In applications with significant unload transients, the bulk input capacitance must be sized to include energy transfer from the primary side capacitor to the input capacitor. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS55010.

The input ripple current can be calculated using Equation 33. The value of a ceramic capacitor varies significantly overtemperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable overtemperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

The input capacitor should be larger than the values calculated in Equation 31 and Equation 32. For this design, the calculated minium input capacitance is 12.6 µF using Equation 31 and the rms current is 0.46 A. A 47 µF/10V X5R ceramic capacitor is used on the input. A 0.1 µF ceramic capacitor is placed as close to the VIN and GND pins as possible for a good bias supply.

$$C_{IN(MIN)} = \frac{I_{OUT} \frac{N_{SEC}}{N_{PRI}} \times D}{f_{SW} \times \Delta V_{CIN}} \tag{31}$$

$$C_{IN(MIN)} = \frac{Im_ripple \times L_{O(PRI)}}{8 \times \left(V_{IN} \times V_{PRI}\right) \times \Delta V_{CINI}} \tag{32}$$

$$ICin_rms = ILpri_pospk \times \sqrt{\frac{D}{3}} \tag{33}$$

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9.2.9 Y – Capacitor

The Y-capacitor should be used between the primary and secondary to attenuate common mode (CM) noise in noise sensitive applications. When connecting the primary and secondary grounds with a large loop area, the primary side switching noise can be injected via the interwinding capacitance of the isolation transformer, creating common mode noise in the secondary. A Y-capacitor can be used to provide a local return path for these currents with a small capacitor connected between the secondary ground and the primary ground. The voltage rating of the Y-capacitor should be equivalent to the transformer insulation voltage. If the converter is used for safety isolation there is an upper limit on the amount of capacitance. The inter-winding capacitances of the transformer and maximum leakage current (e.g. UL60950 Class I equipment leakage current <3.5 mA) allowed by the safety standard will set the maximum value. It is not recommended to use the Y-capacitor in applications which experience large voltage transients such as a floating gate drive supply in a power inverter.

9.2.10 Slow Start Capacitor

To minimize overshoot during power up or recovery from an overload condition a slow start capacitor is used. A 35-ms slow start is desired and using Equation 5 a 0.1 µF capacitor is calculated.

9.2.11 Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the BOOT pin and PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

9.2.12 UVLO Resistors

Using the start and stop voltages of 4.5 V and 4 V, respectively, the UVLO resistors 71.5 kΩ and 26.7 kΩ are calculated using Equation 3 and Equation 4.

9.2.13 Compensation

There are several methods used to compensate DC/DC regulators. The method presented here uses the model of the PWM modulator in the SLVC363 excel tool to choose the compensation components. For most optimized loop compensation, the gain and phase of the PWM modulator can be measured with a network measurement tool.

Compensation of a Fly-Buck converter should be done at no load when the loop response is similar to that of a buck converter. With a 47 µF primary capacitor Type 2 compensation is recommended providing a phase boost typically of 165 degrees. For 60 degrees of phase margin, the modulator phase must then be above –105 degrees. The target loop bandwidth is then the frequency when the modulator phase is –105 degrees. Figure 23 shows the modeled modulator frequency response. When modeling the frequency response of the modulator, make sure to include the derating of the ceramic capacitor due to DC bias. In this example the 47 µF capacitor was derated to 36 µF. From this, the target frequency is 29 kHz where the gain is 0.75 dB. With the modulator gain, the value of R_C is chosen to set the gain of the compensated error amplifier at the reciprocal of the modulator gain with Equation 34. C_C is then chosen to place a zero at 1/10 the target bandwidth with Equation 35. C_{HF} from the COMP pin to ground attenuates high frequency noise. This is selected to add a pole at half the switching frequency with Equation 36. In this example, the final standard values for the compensation are R_C = 10.5 kΩ, C_C = 5600 pF and C_{HF} = 82 pF.

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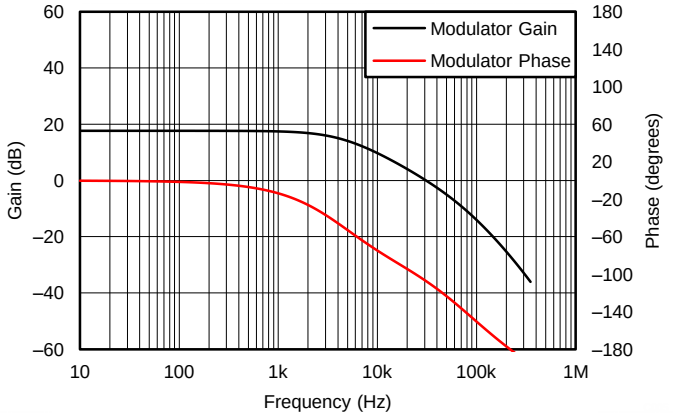


Figure 23. Modeled Modulator Small Signal Response

$$R_C = \frac{1}{gmea \times \frac{R_{LS}}{\left(R_{HS} + R_{LS}\right)} \times 10^{\frac{Gmod_{fbw}}{20}}} \quad (34)$$

$$C_C = \frac{1}{2\pi \times R_C \times \frac{fsw}{10}} \quad (35)$$

$$C_{HF} = \frac{1}{2\pi \times R_C \times \frac{fsw}{2}} \quad (36)$$

9.2.14 Design Tips

In applications operating near the maximum input voltage (for example 5 V and higher) and at high risk for overload conditions on the output, a bulk ceramic input capacitor with low ESR may be necessary to keep the input voltage stable. If the low-side MOSFET turns off while sinking current nnergy is transferred back to the input and the additional capacitance is used to absorb this energy. During over load conditions the peak current transferred to the input can be as high as the low-side MOSFET sinking current limit.

If there is a large ripple on VIN, there is not only risk of exceeding the absolute maximum voltage on the VIN pin, but also on the PH pin. When the low-side MOSFET turns off while sinking current the body diode of the internal high-side MOSFET will conduct for a short dead time period before the high-side MOSFET turns on. While the body diode conducts, the PH pin voltage is equal to V_{IN} + Vbody. Vbody is 0.8 V typical but can be as high as 1.2 V maximum. The 0.1 µF bypass input capacitor should placed as close as is practically possible to the VIN and GND pins to help minimize high frequency voltage overshoot at the PH pin. Additionally a snubber capacitor located as close as possible to the PH pins and the GND pins with a value of 1000 pF limits the slew rate of the PH node to reduce the voltage stress at the PH pin. To further reduce the voltage stress on the internal low-side MOSFET, an external schottky diode with a low voltage drop can be added from the PH pin to the VIN pin. This bypasses the body diode of the internal high-side MOSFET. Figure 24 shows the added components.

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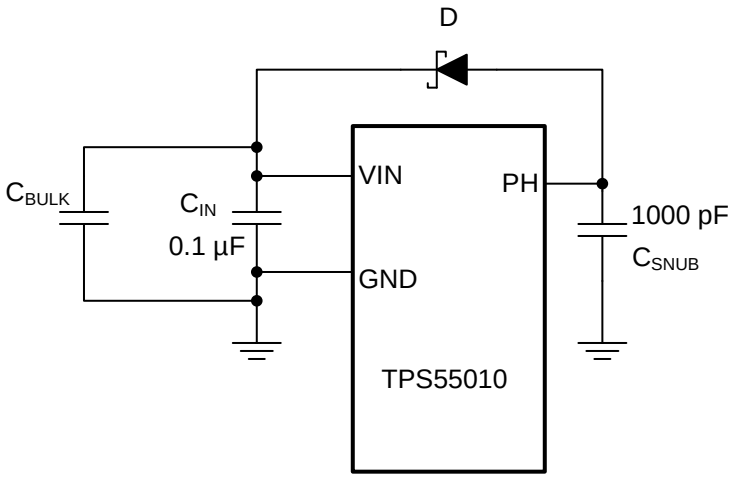


Figure 24. Other External Components

9.2.15 How to Specify a Fly-Buck Transformer

There are two catalog transformers available for the TPS55010. See Table 3

Table 3. Transformers

Part Number	Specifications	Vendor
750311880	2.5 µH, 1:2.5 Turns Ratio, Basic Insulation, 2500 Vrms	See the SLVU459 BOM
750311780	2.0 µH, 1:8:8 Turns Ratio, Basic Insulation, 2000 Vrms	See the SLVU494 BOM

If a catalog or standard off the shelf transformer is not available, use this section to determine the transformer specifications to supply a vendor. Selecting the magnetizing inductance is similar to the conventional flyback converter operating in continuous conduction mode. One distinction is the voltage across the transformer during the on time is different. The voltage is the difference in the input voltage and voltage across the primary capacitor. For a conventional flyback, only the input voltage is across the primary. Another distinction is the peak current in the primary is the negative current peak.

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Table 4. Transformer Design Form

PARAMETER	DESCRIPTION		
Input Voltage Range (V)			
Output Voltage (V)			
Output Current (A)			
Operating Mode	Continuous Conduction Mode		
Primary Voltage (V)	Use Equation 9 and Equation 10		
Duty Cycle Range (%)	Use Equation 9		
Turns Ratio (N_{PRI}:N_{SEC})	Use Equation 10		
Switching Frequency (Hz)	Use Equation 12 to Equation 16		
Primary Inductance (H)	Use Equation 12 to Equation 16		
Peak Current Positive (A)	Use Equation 12 to Equation 16		
Peak Current Negative (A)	Use Equation 12 to Equation 16		
Insulation Requirements	Functional, Basic, Reinforced		
Regulatory Agencies/Specification	UL, IEC		
Dielectric Withstand Voltage		AC	DC
Working Voltage		AC	DC

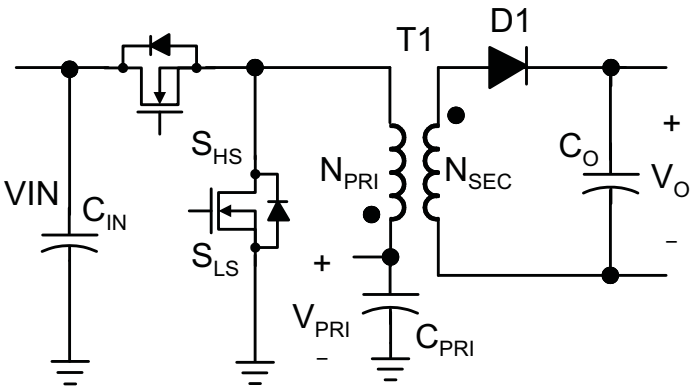


Figure 25. Topology

9.2.16 Application Curves

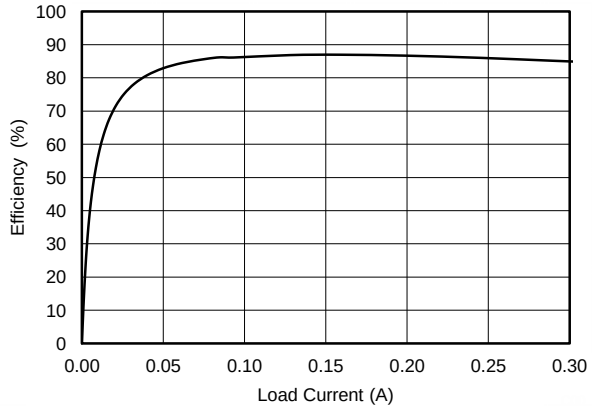


Figure 26. Efficiency vs Output Current

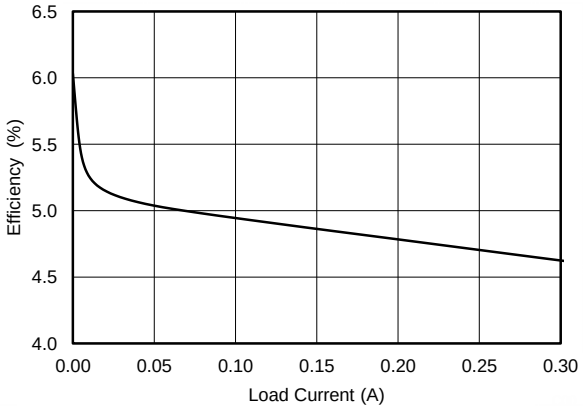


Figure 27. Output Voltage vs Output Current

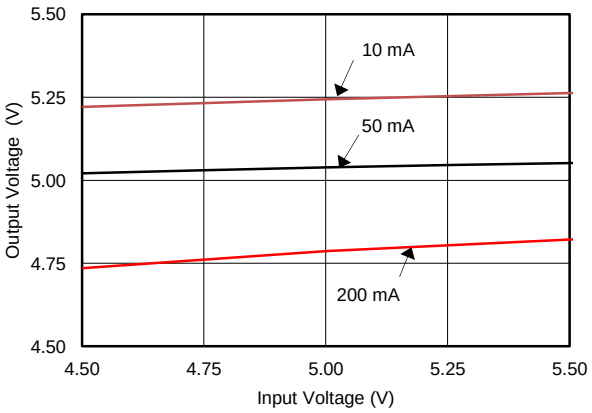


Figure 28. Output Voltage vs Input Voltage

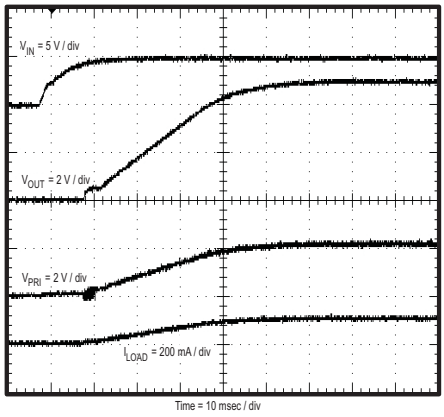


Figure 29. Power Up with Input Voltage

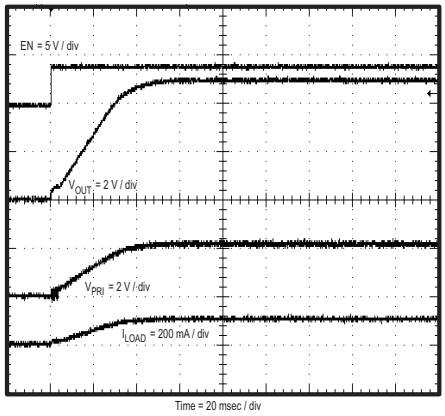


Figure 30. Power Up with Enable Pin

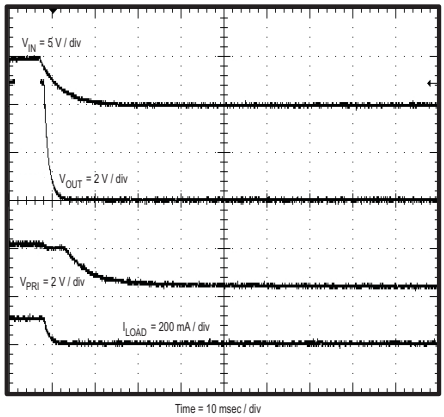


Figure 31. Power Down with Input Voltage

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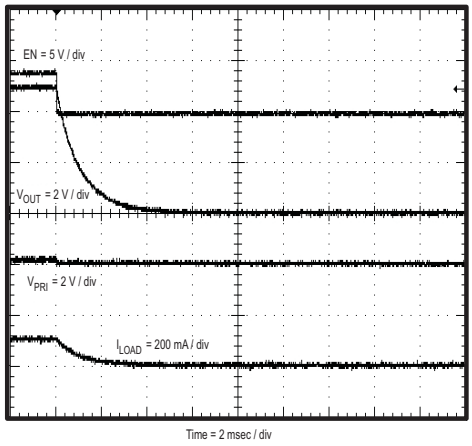


Figure 32. Power Down with Enable Pin

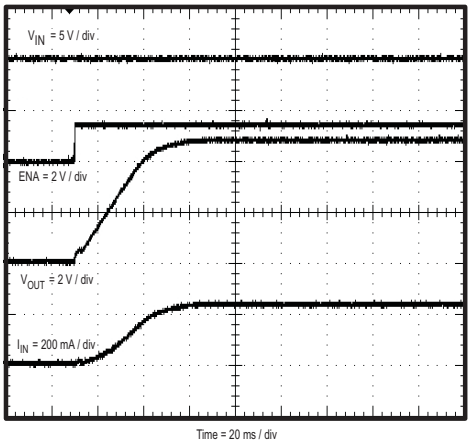


Figure 33. Inrush Current During Power Up

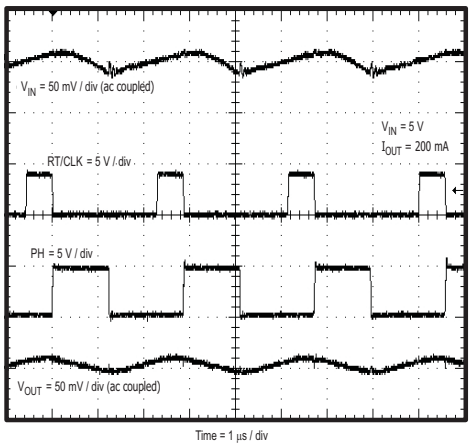


Figure 34. Synchronize to External Clock

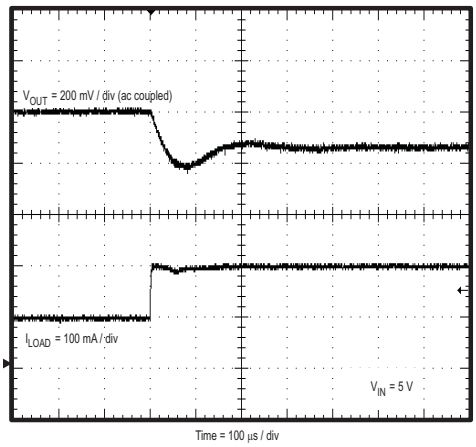


Figure 35. Load Step Response

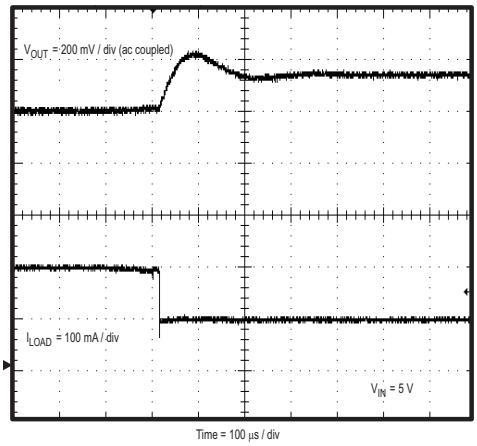


Figure 36. Load Step Response

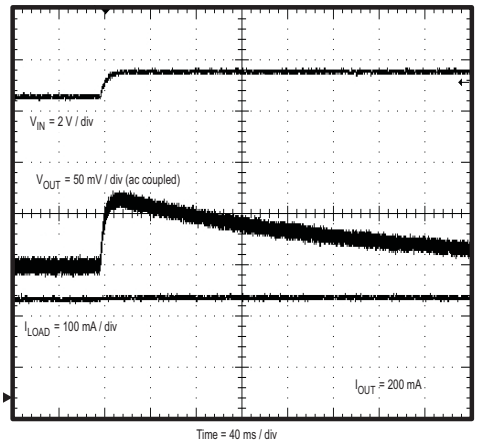


Figure 37. Line Step Response

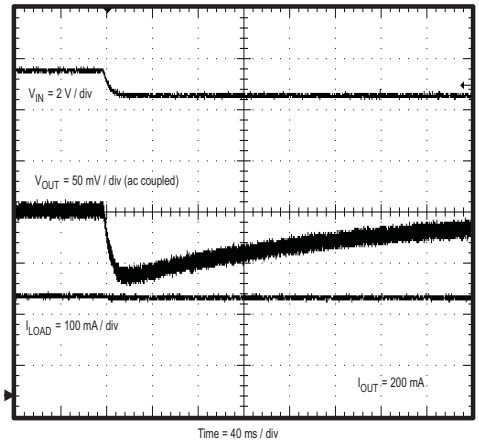


Figure 38. Line Step Response

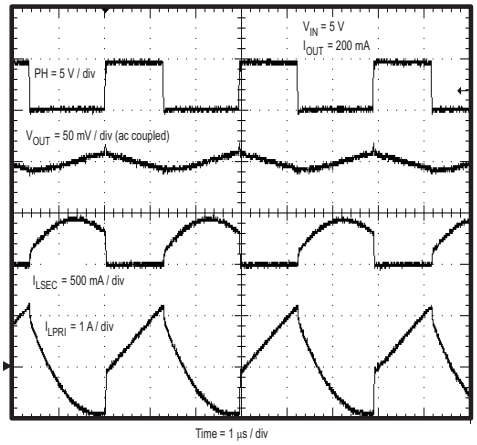


Figure 39. Steady State Waveforms

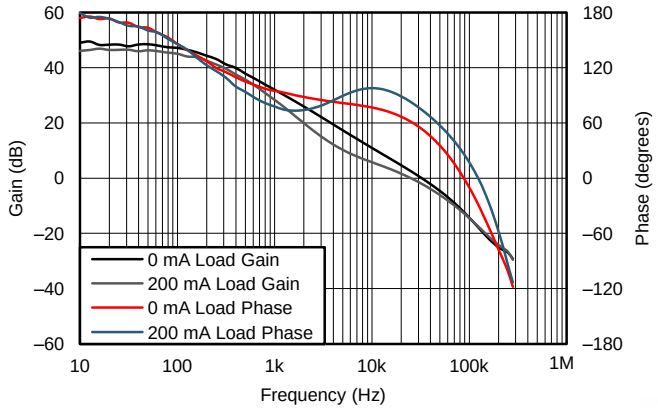


Figure 40. Frequency Response

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9.3 Typical Application, Dual Output

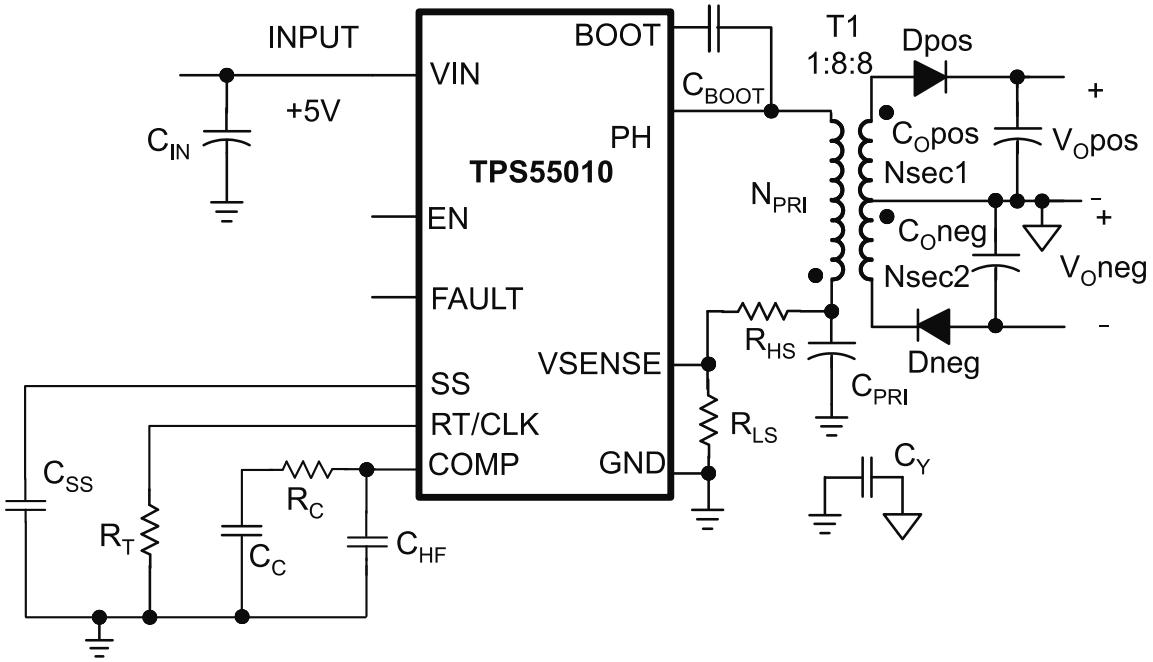


Figure 41. 5 V to 15 V and -15 V Isolated Power Supply

Table 5. Reference Design for Dual Output Application

	5 V to +15 V and -15 V at 0.04 A each
C_{IN}	47 µF X5R 6.3V
C_{OPOS},C_{ONEG}	10 µF X5R 25V
C_{PRI}	47 µF X5R 10V
C_{BOOT}	0.1 µF X5R 10V
C_{SS}	0.1 µF X5R 10V
C_C	3.9 nF
C_{HF}	68 pF
R_C	11.0 kΩ
R_{HS}	13.7 kΩ
R_{LS}	10.0 kΩ
R_T	243 kΩ
T1	750311780 (See the SLVU494 BOM)
D_{POS}, D_{NEG}	B1100

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9.3.1 Design Guide Requirements

Table 6. Design Parameters

PARAMETER	VALUE
Input Voltage	5 V nominal (4.5 V to 5.5 V)
Positive Output Voltage, $V_{O(POS)}$	+15 V
Negative Output Voltage, $V_{O(NEG)}$)	-15 V
Output Voltage Ripple	<0.5%
Output Current $I_{O(POS)}$, $I_{O(NEG)}$	40 mA
Start Voltage	4.5 V
Stop Voltage	4 V

9.3.2 Detailed Design Procedures

9.3.2.1 Primary Side Voltage for Dual Output

Similar to the single output design, the dual output voltages are a function of the primary voltage, transformer turns ratio and the diode voltages. Using the same design constraints as the single, the primary side voltage could be from 3.6 V to 1.1 V. A 1.93 V primary side voltage is selected, and the duty cycle is approximately 38.5%.

$$D = \frac{V_{PRI}}{V_{IN}} \tag{37}$$

9.3.2.2 Turns Ratio

The transformer turns ratio is calculated using the desired output voltages, diode voltages and the primary voltage. Assuming diode voltages of 0.5 V, $V_O$pos of 15 V, $V_O$neg of -15V and a V_{PRI} of 1.93 V yields a N_{PRI} x N_{SEC1} x N_{SEC2} turns ratio of 1:8:8. Since the TPS55010 is flexible on the adjusting the primary side, a couple iterations of selecting turns ratio may help find a solution that is good for multiple applications with the same transformer.

$$\frac{N_{SEC1} + N_{SEC2}}{N_{PRI}} = \frac{V_{OPOS} - V_{ONEG} + 2 \times V_{FD}}{V_{PRI}} \tag{38}$$

9.3.2.3 Voltage Feedback

Selecting 10 kΩ for the R_{LS} , R_{HS} is calculated to be 13.28 kΩ using Equation 39. Choose 13.7 kΩ as the nearest standard value.

$$R_{HS} = R_{LS} \times \left(\frac{V_{PRI} - 0.829V}{0.829V} \right) \tag{39}$$

9.3.2.4 Selecting the Switching Frequency and Primary Inductance

For this design example, the switching frequency is selected to be 400 kHz. Using Equation 6, the timing resistor value is 243 kΩ. $L_O$max and $L_O$min are calculated to be 2.31 µH and 1.09 µH respectively assuming a current limit of 2 A. Also check that the inductance doesn't exceed the value calculated by Equation 14 to ensure there is enough current ripple for the PWM control system. Selecting a primary inductance of the 2 µH, the positive and negative peak current are calculated as 1.38 A and -2.19 A in the primary which do not exceed the current limits of the power switch. The rms currents can be calculated and used to determine the power dissipation in the device. The magnetizing ripple current is calculated as 1.48 A using Equation 45.

The highside FET and lowside FET rms currents are calculated as 0.478 A and 0.681 A, respectively using Equation 46 and Equation 47. The sum of these currents, i.e. 1.16 A is the primary side rms current for the magnetics.

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$$I_{OPN} = \left(I_{OPOS} \frac{N_{SEC1}}{N_{PRI}} + I_{ONEG} \frac{N_{SEC2}}{N_{PRI}} \right) \quad (40)$$

$$L_{OMAX} = \frac{V_{IN} \times D \times (1 - D)}{2 \times I_{OPN} \times f_{SW}} \quad (41)$$

$$L_{OMIN} = \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{SW} \times (I_{HSCL} - I_{OPN})} \quad (42)$$

$$ILpri_pospk \approx I_{OPN} + \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{SW} \times L_{OPRI}} \quad (43)$$

$$ILpri_negpk \approx -I_{OPN} \times \left(\frac{1 + D}{1 - D} \right) - \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{SW} \times L_{OPRI}} \quad (44)$$

$$Im_ripple = \frac{V_{IN} \times D \times (1 - D)}{f_{sw} \times L_{OPRI}} \quad (45)$$

$$I_{HS_rms} \approx \left(D \times I_{OPN}^2 + \frac{D}{12} \times Im_ripple^2 \right)^{\frac{1}{2}} \quad (46)$$

$$I_{LS_rms} \approx \left(\frac{3 \times D - 1}{3 \times (1 - D)} \times I_{OPN}^2 + \frac{Im_ripple}{3} \times I_{OPN} + \frac{1 - D}{12} \times Im_ripple^2 \right)^{\frac{1}{2}} \quad (47)$$

9.3.2.4.1 Primary Side Capacitor

The ΔV_{PRI} voltage should be less than 2% of V_{PRI}. The rated RMS current of C_{PRI} should be greater than Equation 48. For this design example, the charging current and time need to be calculated using Equation 49 and Equation 50. The I_{CPRI_ch} is 0.63 A and the t_{CPRI} is 1.56 µs. Assuming the ΔV_{PRI} is 0.193 V, the primary side capacitance is 25.4 µF using Equation 48. The rms current is 1.16 A from Equation 48. A 47 µF/6.3V X5R ceramic capacitor is used.

$$I_{CPRI_rms} \approx I_{LS_rms} + I_{HS_rms} \quad (48)$$

$$I_{CPRI_ch} \approx ILpri_pospk \times \sqrt{\frac{D + (1 - D) \times \frac{ILpri_pospk}{ILpri_pospk - ILpri_negpk}}{3}} \quad (49)$$

$$t_{CPRI} \approx \frac{D}{f_{SW}} + \frac{(1 - D)}{f_{SW}} \times \frac{ILpri_pospk}{ILpri_pospk - ILpri_negpk} \quad (50)$$

$$C_{PRI} = \frac{\left(I_{CPRI_ch} \times t_{CPRI}\right)}{\Delta V_{PRI}} \quad (51)$$

9.3.2.4.2 Secondary Side Diode

The diodes should be selected to handle the voltage stresses and rms currents calculated in Equation 52 and Equation 54. Typically, a low duty cycle or high turns ratio design will have a larger voltage stress on the diode

At the maximum input voltage of 5.5 V, the V_{diode_max} voltage is calculated at 43.56 V. The rms current is calculated as 0.059 A. The diode peak current is 0.130 A using Equation 53 and the power dissipated in the diode is 0.02 W. The B1100 diode will be used which is rated for 100 V and 1 A.

$$V_{diode_max} = (V_{IN_max} - V_{PRI}) \times \frac{N_{SEC1}}{N_{PRI}} + V_{OPOS} = (V_{IN_max} - V_{PRI}) \times \frac{N_{SEC2}}{N_{PRI}} + V_{ONEG} \quad (52)$$

$$I_{diode_peak} = 2 \times \frac{I_{OPOS}}{1 - D} = 2 \times \frac{I_{ONEG}}{1 - D} \quad (53)$$

$$I_{diode_rms} = 2 \times I_{OPOS} \times \left(\frac{1}{3 \times (1 - D)}\right)^{\frac{1}{2}} = 2 \times I_{ONEG} \times \left(\frac{1}{3 \times (1 - D)}\right)^{\frac{1}{2}} \quad (54)$$

$$P_{diode} = V_{FD} \times I_{OPOS} = V_{FD} \times I_{ONEG} \quad (55)$$

9.3.2.4.3 Secondary Side Capacitor

The ΔV_{COPOS} and ΔV_{CONEG} voltage should be 0.25% to 1% of the respective nominal voltage. The converter transfers energy each switching period to the secondary, since the converter has primary side feedback, at light or no load conditions the output voltage may rise above the desired output. If the application will experience a no load condition, attention to the capacitor voltage ratings should be considered. Adding a ballast load, zener diode or linear regulator can help prevent the overvoltage at light or no load.

The output capacitance is calculated to be 0.51 µF assuming a ΔV_{COPOS} of 75 mV using Equation 56 and the rms current is 0.043 A from Equation 57. 10 µF/25 V capacitors are used for V_{OPOS} and V_{ONEG} output.

$$C_O = \frac{I_{OPOS} \times D}{f_{SW} \times \Delta V_{COPOS}} = \frac{I_{ONEG} \times D}{f_{SW} \times \Delta V_{CONEG}} \quad (56)$$

$$I_{CO_rms} = \sqrt{I_{diode_rms}^{2} - I_{OPOS}^{2}} \quad (57)$$

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9.3.2.4.4 Input Capacitor

The ΔV_{CIN} voltage should be 0.25% to 1% of V_{IN}. The TPS55010 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 2.2 µF of effective capacitance or larger coupled to VIN and GND pins and in some applications additional bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The input ripple current can be calculated using Equation 59, select a capacitor with a larger ripple current rating.

In applications with significant unload transients, the bulk input capacitance must be sized to include energy transfer from the primary side capacitor to the input capacitor. The input capacitor should be larger than the values calculated in Equation 58 and Equation 32. For this design, the input capacitance is calculated 12.4 µF using Equation 58 and the rms current is 0.495 A. A 47 µF/10 V X5R ceramic capacitor is used on the input. A 0.1 µF ceramic capacitor is placed as close to the VIN and GND pins as possible for a good bias supply.

$$C_{IN} = \frac{I_{OPN} \times D}{f_{SW} \times \Delta V_{CIN}} \tag{58}$$

$$I_{CIN_rms} = ILpri_pospk \times \sqrt{\frac{D}{3}} \tag{59}$$

9.3.2.5 Compensation

Compensation of the dual output design is the same as the single output presented in Compensation. Using the Model of the PWM modulator in the SLVC363 excel tool the target frequency is 34 kHz and the modulator gain at this frequency is -1.04 dB. Using Equation 34 to Equation 36 the final nearest standard values for the compensation are R_C = 11 kΩ, C_C = 3900 pF and C_{HF} = 68 pF.

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9.3.2.6 Application Curves

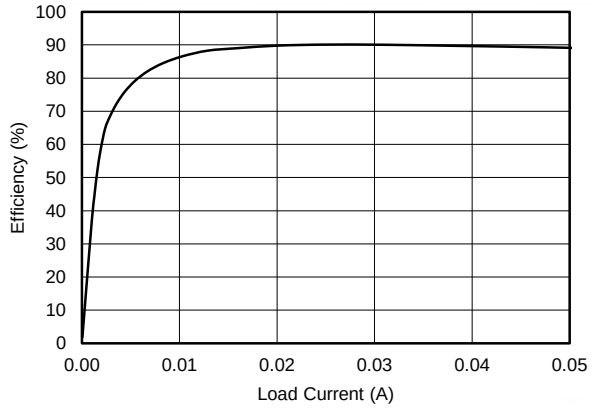


Figure 42. Efficiency vs Output Current

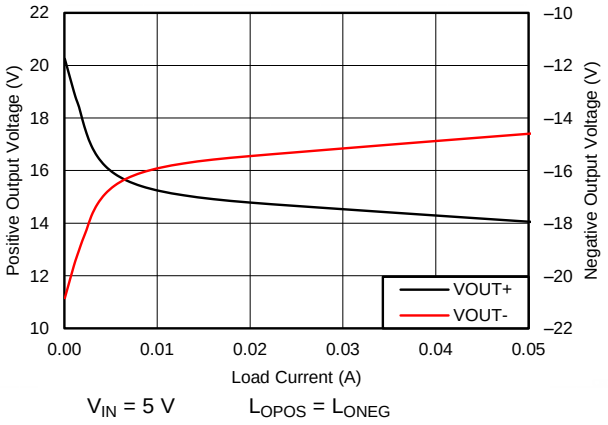


Figure 43. Output Voltage vs Output Current

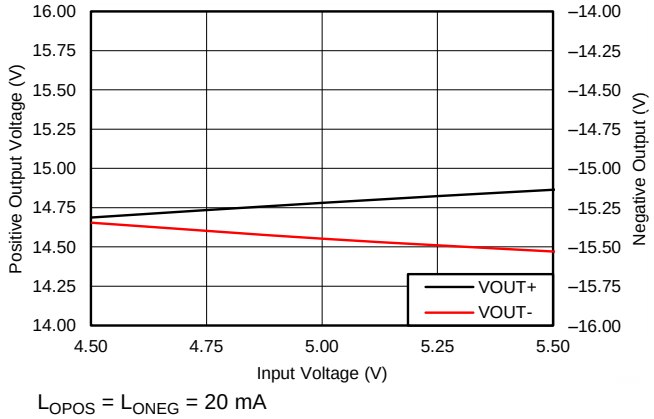


Figure 44. Output Voltage vs Input Voltage

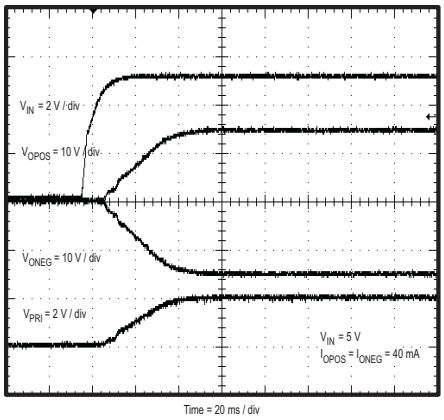


Figure 45. Power Up with Input Voltage

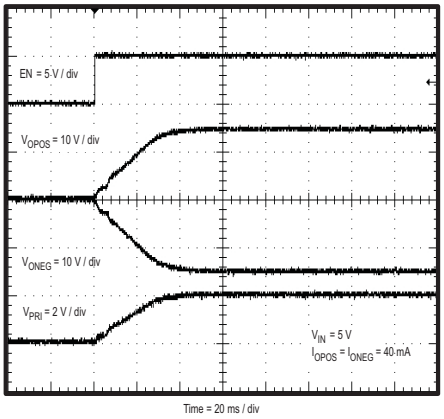


Figure 46. Power Up with Enable Pin

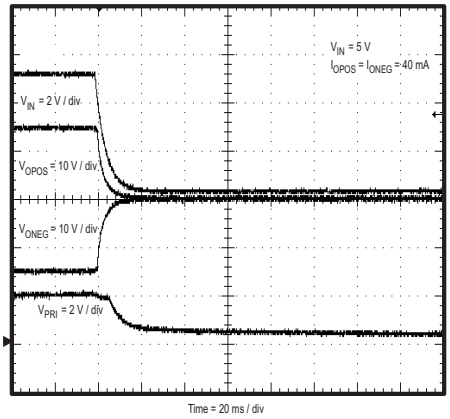


Figure 47. Power Down with Input Voltage

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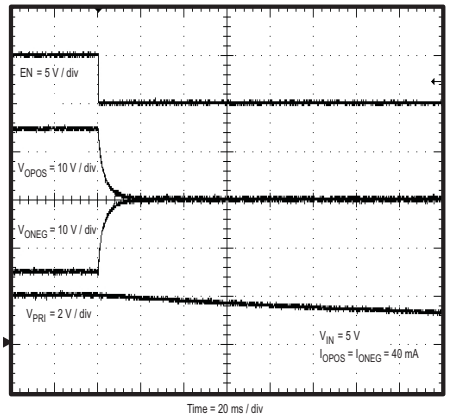


Figure 48. Power Down with Enable Pin

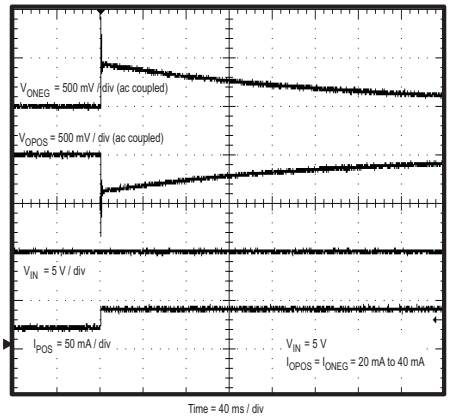


Figure 49. Load Step Response

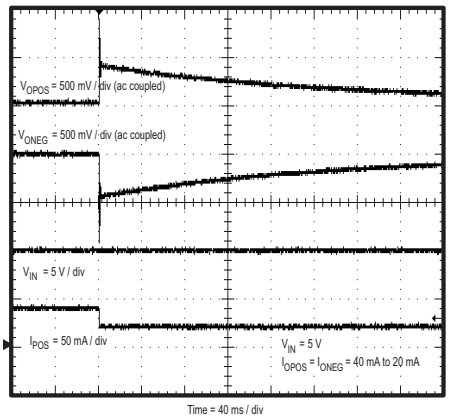


Figure 50. Load Step Response

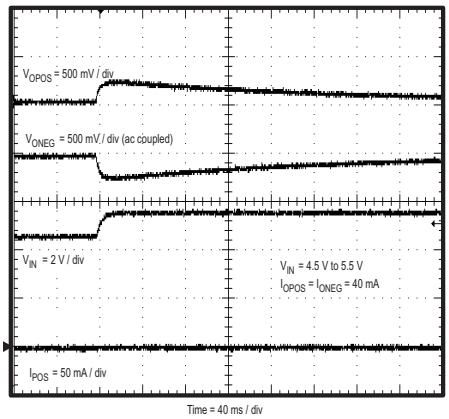


Figure 51. Line Step Response

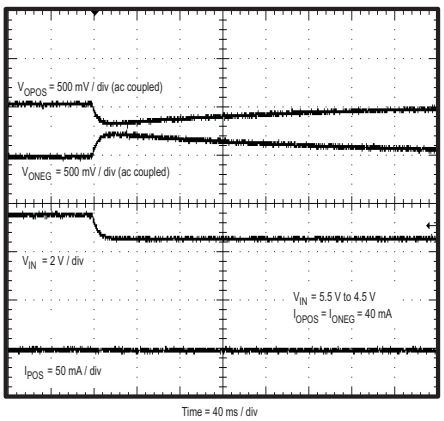


Figure 52. Line Step Response

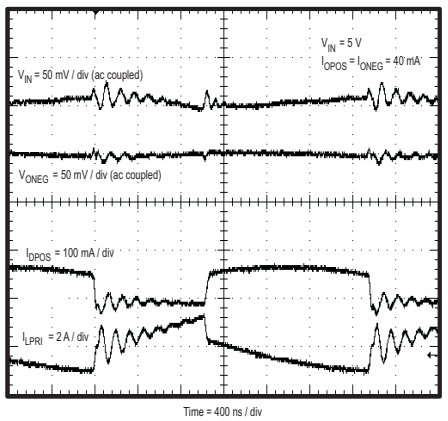


Figure 53. Steady State Waveforms

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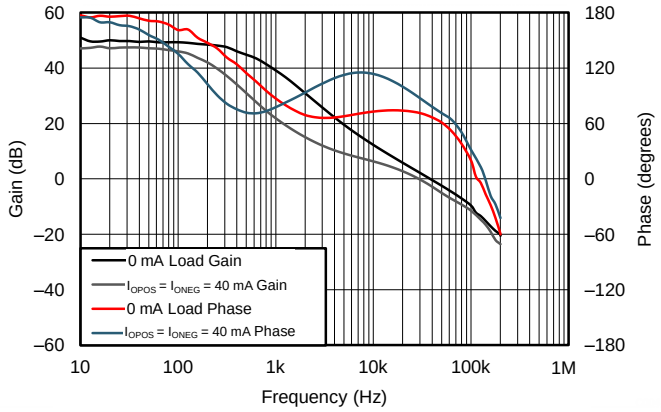


Figure 54. Loop Response

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10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.95 V and 6 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS55010 IC additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 μF is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 55 for a PCB layout example. The GND pins should be tied directly to the thermal pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors.

- Locate the input bypass capacitor as close to the IC as possible.
- The PH pin should be routed to the primary side of the transformer.
- Since the PH connection is the switching node, the transformer should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The boot capacitor must also be located close to the device.
- The sensitive analog ground connections for the feedback voltage divider, compensation component, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown.
- The RT/CLK pin is particularly sensitive to noise so the R_T resistor should be located as close as possible to the IC and routed with minimal lengths of trace. Avoid connecting y capacitor on nodes which experience high dv/dt.

11.2 Layout Example

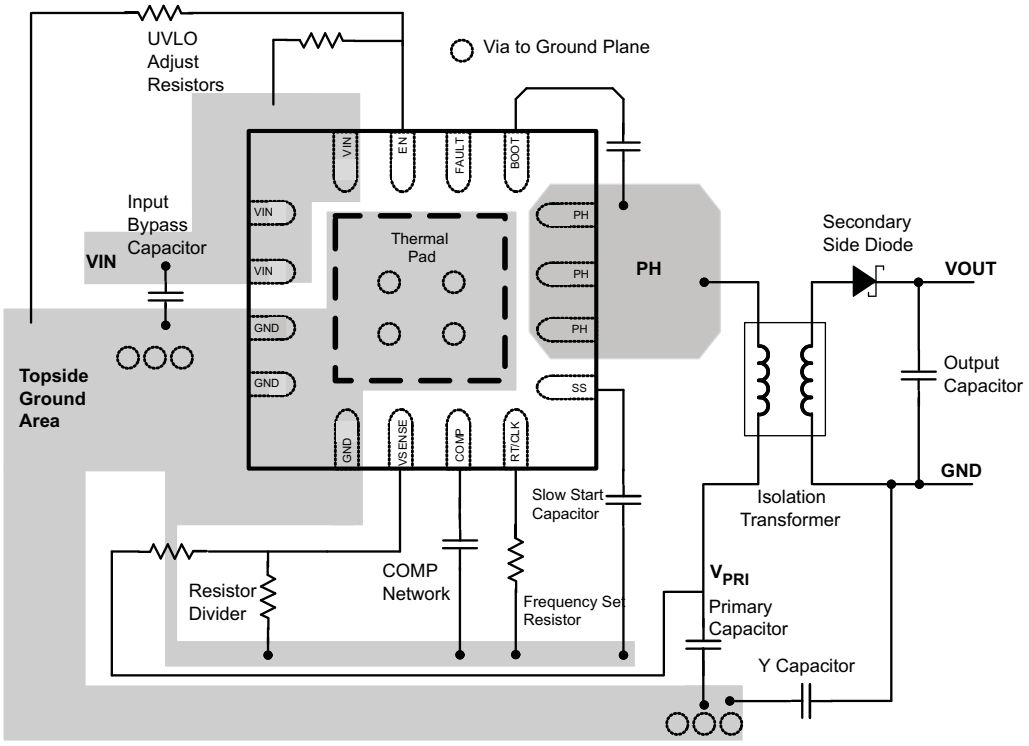


Figure 55. PCB Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 商标

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All other trademarks are the property of their respective owners.

12.3 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55010RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55010	Samples
TPS55010RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

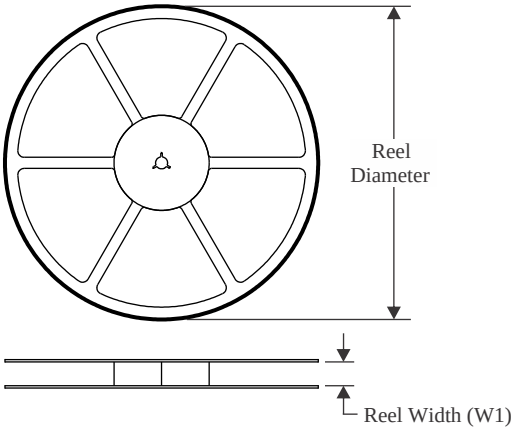
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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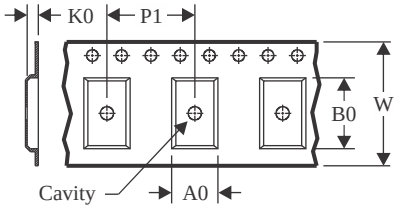
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

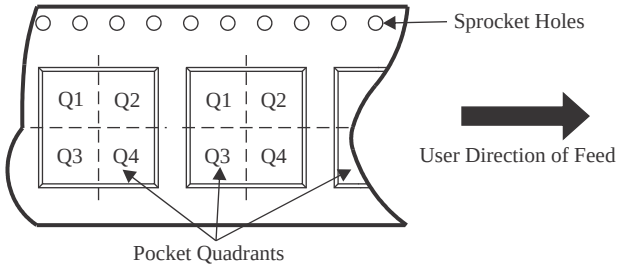


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

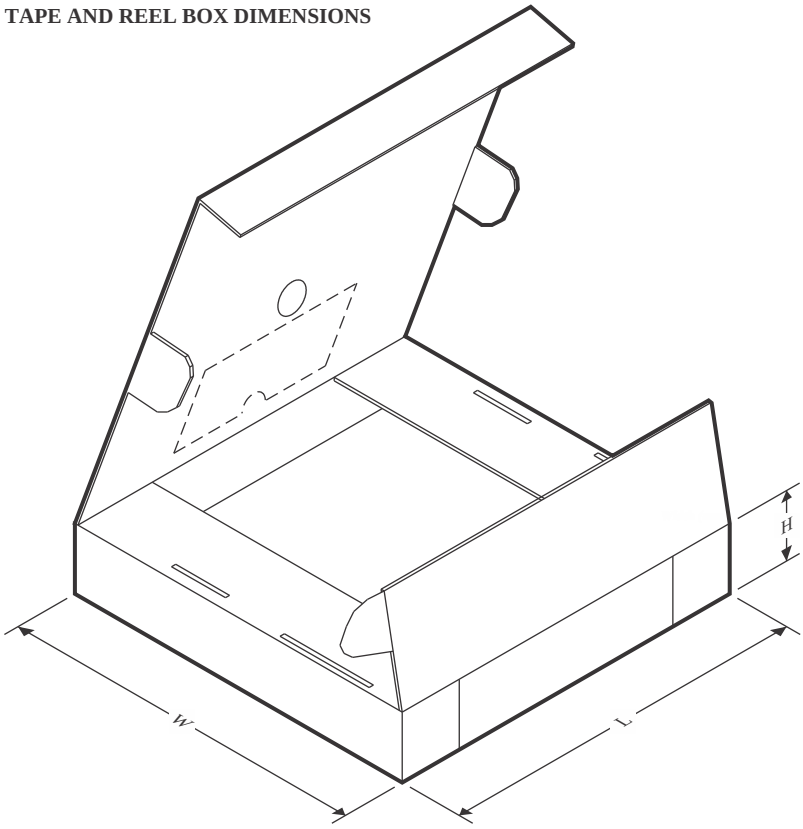
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55010RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55010RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55010RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS55010RTET	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

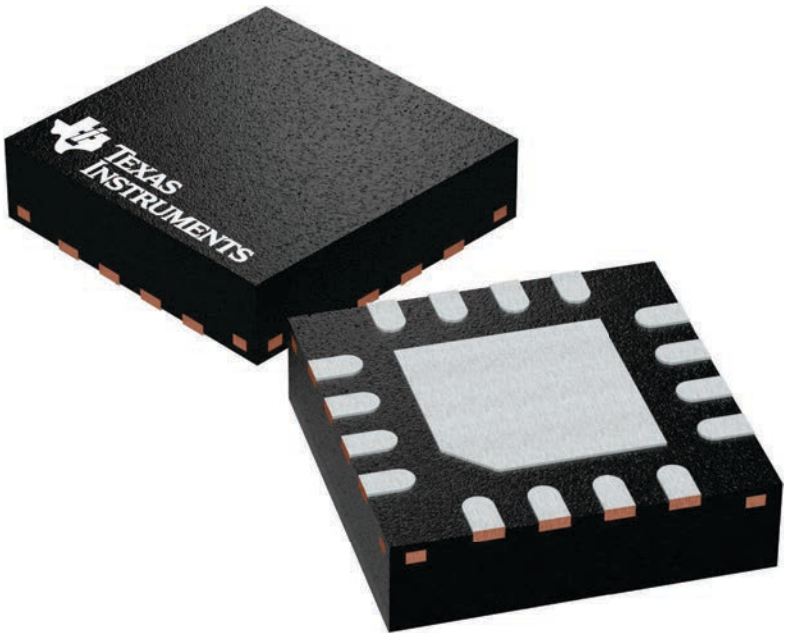
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

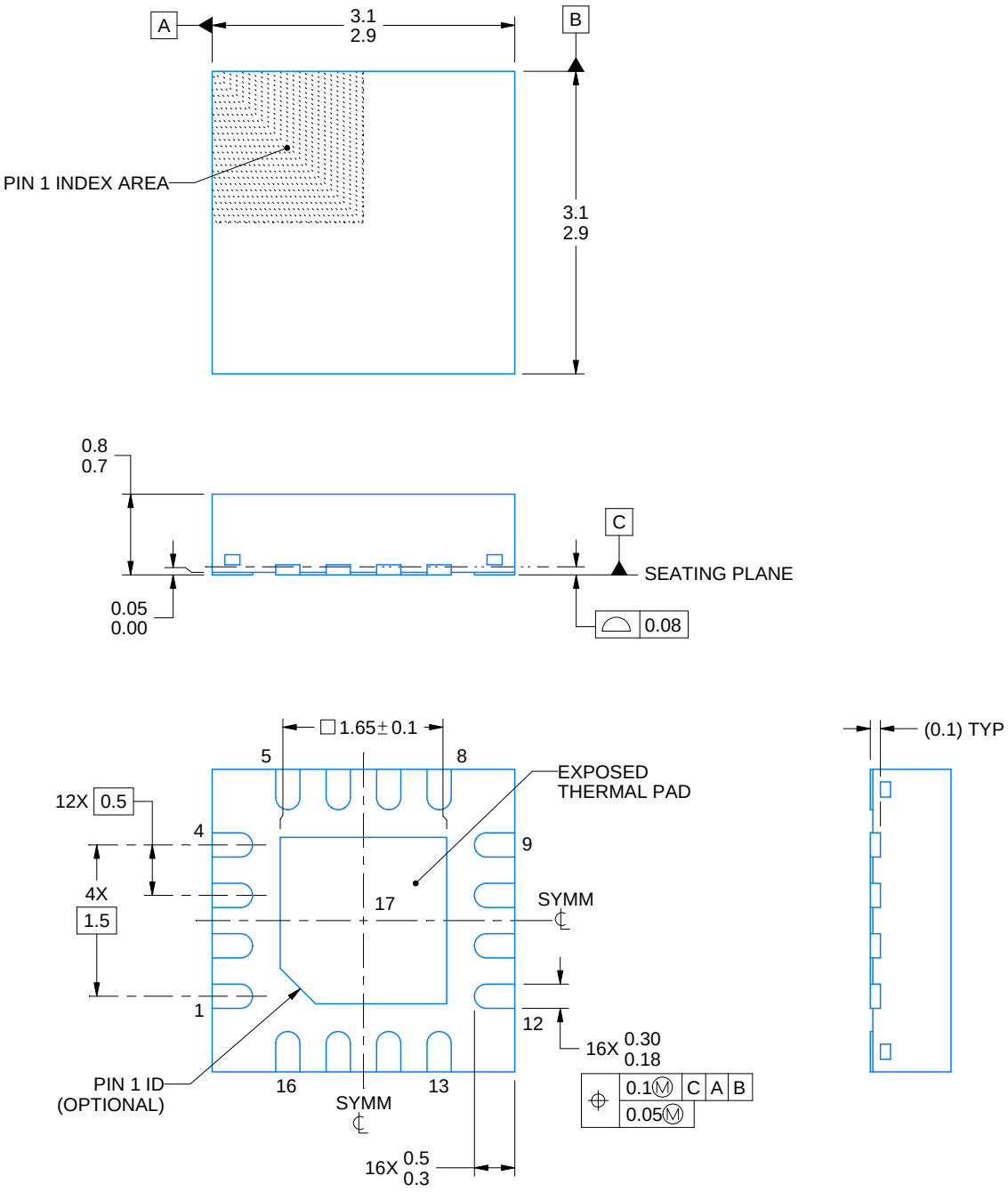


RTE0016F

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

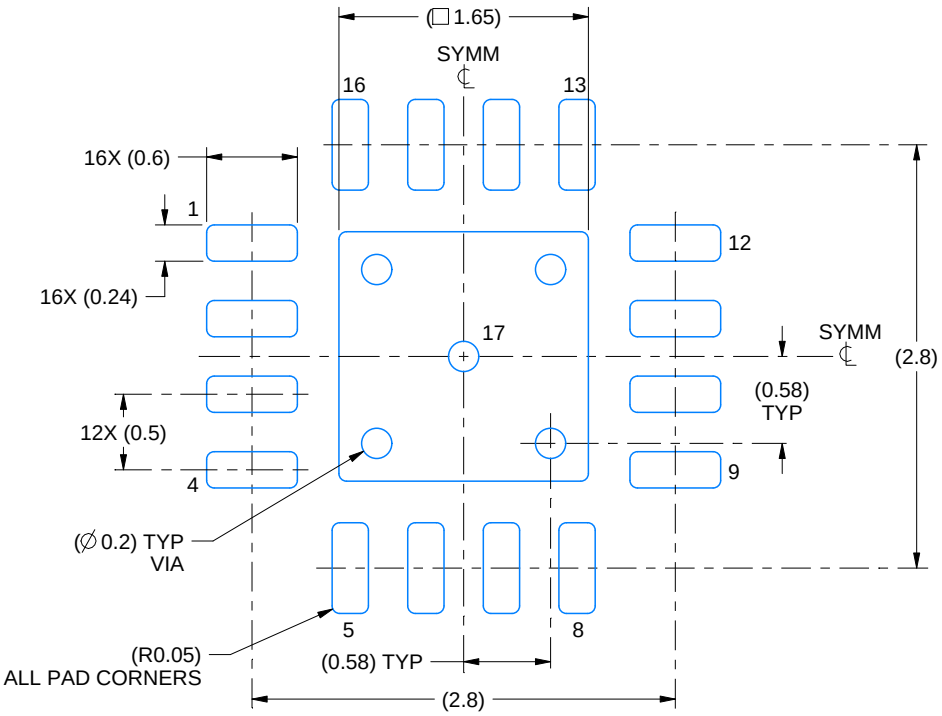
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

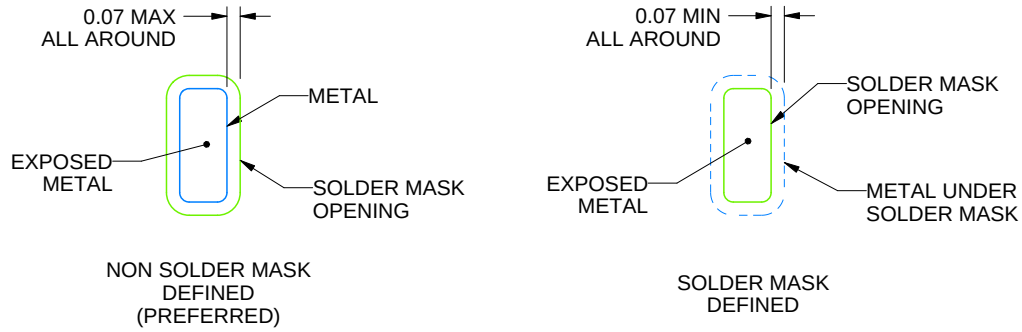
RTE0016F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

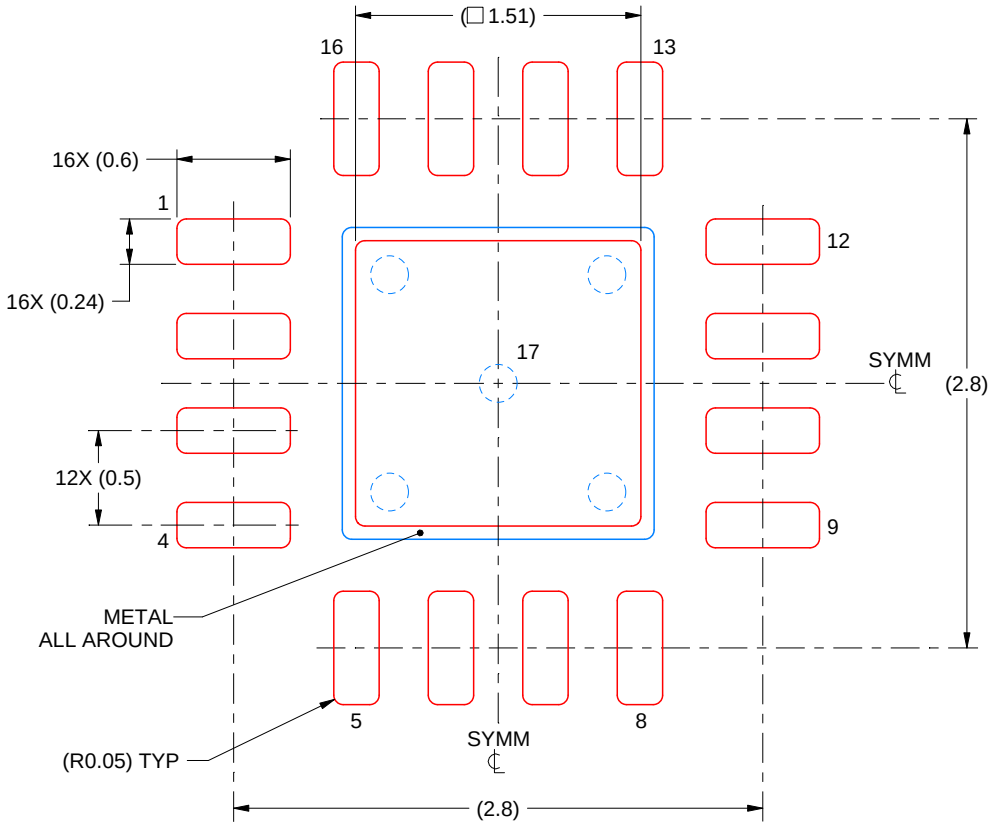


SOLDER MASK DETAILS

4219119/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219119/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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