IEEE 1394b THREE-PORT CABLE TRANSCEIVER/ARBITER

FEATURES

- Fully Supports Provisions of IEEE P1394b Revision 1.33+ at 1-Gigabit Signaling Rates
- Fully Supports Provisions of IEEE 1394a-2000 and 1394-1995 Standard for High Performance Serial Bus
- Fully Interoperable With Firewire, i.LINK, and SB1394™, Implementation of IEEE Std 1394
- Provides Three Fully Backward Compatible, (1394a-2000 Fully Compliant) Bilingual P1394b Cable Ports at up to 800 Megabits per Second (Mbits/s)
- Provides Three 1394a-2000 Fully Compliant Cable Ports at 100/200/400 Mbits/s
- Full 1394a-2000 Support Includes:
  - Connection Debounce
  - Arbitrated Short Reset
  - Multispeed Concatenation
  - Arbitration Acceleration
  - Fly-By Concatenation
  - Port Disable/Suspend/Resume
  - Extended Resume Signaling for Compatibility With Legacy DV Devices
- Power-Down Features to Conserve Energy in Battery Powered Applications
- Low-Power Sleep Mode
- Fully Compliant With Open Host Controller Interface (HCI) Requirements
- Cable Power Presence Monitoring
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Register Bits Give Software Control of Contender Bit, Power Class Bits, Link Active Control Bit, and 1394a-2000 Features
- Data Interface to Link-Layer Controller Pin Selectable From 1394a-2000 Mode (2/4/8 Parallel Bits at 49.152 MHz) or 1394b Mode (8 Parallel Bits at 98.304 MHz)
- Interface to Link-Layer Controller Supports Low Cost TI Bus-Holder Isolation
- Interoperable With Link-Layer Controllers Using 3.3-V Supplies
- Interoperable With Other 1394 Physical Layers (PHYs) Using 1.8-V, 3.3-V, and 5-V Supplies
- Low Jitter, External Crystal Oscillator Provides Transmit and Receive Data at 100/200/400/800 Mbits/s, and Link-Layer Controller Clock at 49.152 MHz and 98.304 MHz
- Separate Bias (TPBIAS) for Each Port
- Low Cost, High Performance 80-Pin TQFP (PFP) Thermally Enhanced Package and 168-Pin ZAJ (BGA) Package
- Software Device Reset (SWR)
- Fail-Safe Circuitry Senses Sudden Loss of Power to the Device and Disables the Ports to Ensure That the TSB81BA3E Does Not Load the TPBIAS of Any Connected Device and Blocks any Leakage From the Port Back to Power Plane
- The TSB81BA3E Has a 1394a-2000 Compliant Common-Mode Noise Filter on the Incoming Bias Detect Circuit to Filter Out Cross-Talk Noise
- The TSB81BA3E Is Port Programmable to Force 1394a Mode to Allow Use of 1394a Connectors (1394b Signaling Must Not Be Put Across 1394a Connectors or Cables)
- Internal Voltage Regulator Option

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DESCRIPTION

The TSB81BA3E provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB81BA3E is designed to interface with a link-layer controller (LLC), such as the TSB82AA2, TSB12LV21, TSB12LV26, TSB12LV32, TSB42AA4, TSB42AB4, TSB12LV01B, or TSB12LV01C. It also may be connected cable port to cable port to an integrated 1394 Link + PHY layer such as the TSB43AB2.

The TSB81BA3E can be powered by a single 3.3-V supply when the VREG_PD terminal (terminal 73 on the PFP package and terminal B7 on the ZAJ package) is tied to GND. VREG_PD enables the internal 3.3-V to 1.95-V regulator which provides the 1.95-V to the core. The When VREG_PD is pulled high to VDD through at least a 1-kΩ resistor the TSB81BA3E internal regulator is off and the device can be powered by two separate external regulated supplies: 3.3-V for the I/Os and 1.95-V for the core. The core voltage is supplied to the PLLVDD-CORE and DVDD-CORE terminals to the requirements in the recommended operating conditions (1.95-V nominal). The PLLVDD-CORE terminals must be separated from the DVDD-CORE terminals. The PLLVDD-CORE and the DVDD-CORE terminals must be decoupled with 1 uF capacitors to stabilze the respective supply. Additional 0.10uF and 0.01uF high-frequency bypass capacitors may also be used. The separation between DVDD-CORE and PLLVDD-CORE may be implemented by separate power supply rails, or by a single power supply rail, where the DVDD-CORE and PLLVDD-CORE are separated by a filter network to keep noise from the PLLVDD-CORE supply.

The TSB81BA3E requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. A 49.152-MHz clock signal is supplied to the associated LLC for synchronization of the two devices and is used for resynchronization of the received data when operating the PHY-link interface in compliance with the IEEE 1394a-2000 standard. A 98.304-MHz clock signal is supplied to the associated LLC for synchronization of the two devices when operating the PHY-link interface in compliance with the IEEE P1394b standard. The power down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

Data bits to be transmitted through the cable ports are received from the LLC on two-, four-, or eight-bit parallel paths (depending on the requested transmission speed and PHY-link interface mode of operation). They are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbits/s (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

The PHY-link interface can follow either the IEEE 1394a-2000 protocol or the IEEE 1394b-2002 protocol. When using a 1394a-2000 LLC such as the TSB12LV26, the BMODE terminal must be deasserted. The PHY-link interface then operates in accordance with the legacy 1394a-2000 standard. When using a 1394b LLC such as the TSB82AA2, the BMODE terminal must be asserted. The PHY-link interface then conforms to the P1394b standard.

The cable interface can follow either the IEEE 1394a-2000 protocol or the 1394b protocol on all ports. The mode of operation is determined by the interface capabilities of the ports being connected. When any of the three ports is connected to a 1394a-2000 compliant device, the cable interface on that port operates in the 1394a-2000 data-strobe mode at a compatible S100, S200, or S400 speed. When a bilingual port is connected to a 1394b compliant node, the cable interface on that port operates per the P1394b standard at S400B or S800 speed. The TSB81BA3E automatically determines the correct cable interface connection method for the bilingual ports.

NOTE:

The BMODE terminal does not select the cable interface mode of operation. The BMODE terminal selects the PHY-link interface mode of operation and affects the arbitration modes on the cable. When the BMODE terminal is deasserted, BOSS arbitration is disabled.

During packet reception the serial data bits are split into two-, four-, or eight-bit parallel streams (depending upon the indicated receive speed and the PHY-link interface mode of operation), resynchronized to the local system clock and sent to the associated LLC. The received data is also transmitted (repeated) on the other connected and active cable ports.

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Both the twisted pair A (TPA) and the twisted pair B (TPB) cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration when connected to a 1394a-2000 compliant device. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during 1394a-mode arbitration and sets the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted pair bias (TPBIAS) voltage.

When connected to a 1394a-2000 compliant node, the TSB81BA3E provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains three independent TPBIAS circuits (one for each port). This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 μF.

The line drivers in the TSB81BA3E are designed to work with external 112-Ω termination resistor networks to match the 110-Ω cable impedance. One termination network is required at each end of a twisted-pair cable. Each network is composed of a pair of series-connected ~56-Ω resistors. The midpoint of the pair of resistors that are connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that are directly connected to the TPB terminals is coupled to ground through a parallel RC network with recommended values of 5 kΩ and 270 pF. The values of the external line-termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. A precision external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents.

When the power supply of the TSB81BA3E is off while the twisted-pair cables are connected, the TSB81BA3E transmitter and receiver circuitry present a high-impedance signal to the cable that does not load the device at the other end of the cable.

When the TSB81BA3E is used without one or more of the ports brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the port must be forced to the 1394a-only mode (Data-Strobe-only mode), then the TPB+ and TPB– terminals can be tied together and then pulled to ground; or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS terminal can be connected to a 1-μF capacitor to ground or left unconnected.

To operate a port as a 1394b bilingual port, the force data-strobe-only terminal for the port (DS0, DS1, or DS2) needs to be pulled to ground through a 1-kΩ resistor. The port must be operated in the 1394b bilingual mode whenever a 1394b bilingual or a 1394b beta-only connector is connected to the port. To operate the port as a 1394a-only port, the force data-strobe-only terminal (DS0, DS1, or DS2) needs to be pulled to 3.3 V V_{CC} through a 1-kΩ resistor. The only time the port must be forced to the data-strobe-only mode is if the port is connected to a 1394a connector (either 6 pin, which is recommended, or 4 pin). This mode is provided to ensure that 1394b Signaling is never sent across a 1394a cable.

The TESTM, TESTW, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM and TESTW terminals must be connected to V_{DD} through a 1-kΩ resistor. The SE and SM terminals must be tied to ground through a 1-kΩ resistor.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They may be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the TSB81BA3E, this bit may only be set by a write to the PHY register set. If a node desires to be a contender for IRM or BM, then the node software must set this bit in the PHY register set.

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The LPS (link power status) terminal works with the LKON/DS2 terminal to manage the power usage in the node. The LPS signal from the LLC is used with the LCtrl bit (see Table 1 and Table 2 in the *Application Information* section) to indicate the active/power status of the LLC. The LPS signal also resets, disables, and initializes the PHY-LLC interface (the state of the PHY-LCC interface is controlled solely by the LPS input regardless of the state of the LCtrl bit).

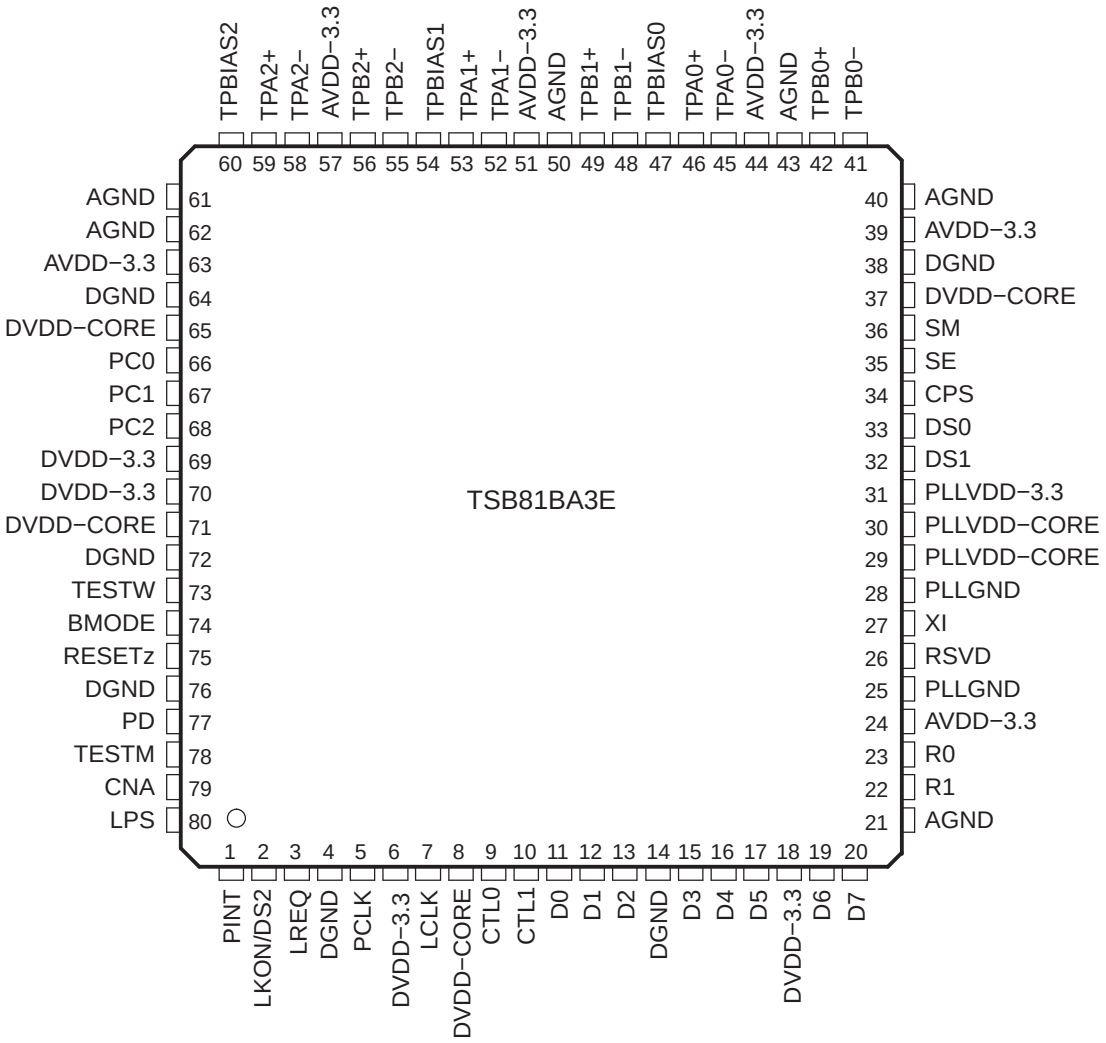
The LPS input is considered inactive if it remains low for more than the LPS_RESET time (see the LPS terminal definition) and is considered active otherwise. When the TSB81BA3E detects that the LPS input is inactive, the PHY-LLC interface is placed into a low-power reset state in which the CTL and D outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than the LPS_DISABLE time (see the LPS terminal definition), then the PHY-LLC interface is put into a low-power disabled state in which the PCLK output is also held inactive. The TSB81BA3E continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and the LPS input is again observed active, the PHY initializes the interface and returns to normal operation. The PHY-LLC interface is also held in the disabled state during hardware reset. When the LPS terminal is returned to an active state after being sensed as having entered the LPS_DISABLE time, the TSB81BA3E issues a bus reset. This broadcasts the node self-ID packet, which contains the updated L bit state (the PHY LLC now being accessible).

The PHY uses the LKON/DS2 terminal to notify the LLC to power up and become active. When activated, the output LKON/DS2 signal is a square wave. The PHY activates the LKON/DS2 output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the LKON/DS2 output when the LLC becomes active (both LPS sensed as active and the LCtrl bit set to 1). The PHY also deasserts the LKON/DS2 output when a bus reset occurs, unless a PHY interrupt condition exists, which would otherwise cause LKON/DS2 to be active. If the PHY is power cycled and the power class is 0 through 4, then the PHY asserts LKON/DS2 for approximately 167 μs or until both the LPS is active and the LCTRL bit is 1.

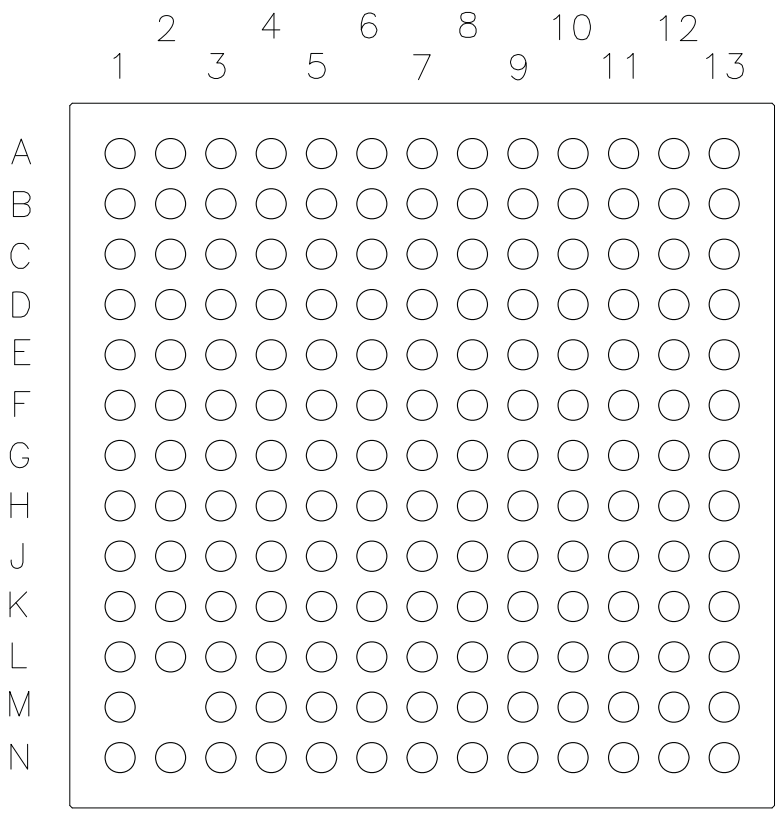
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PIN ASSIGNMENTS

PFP PACKAGE
(TOP VIEW)

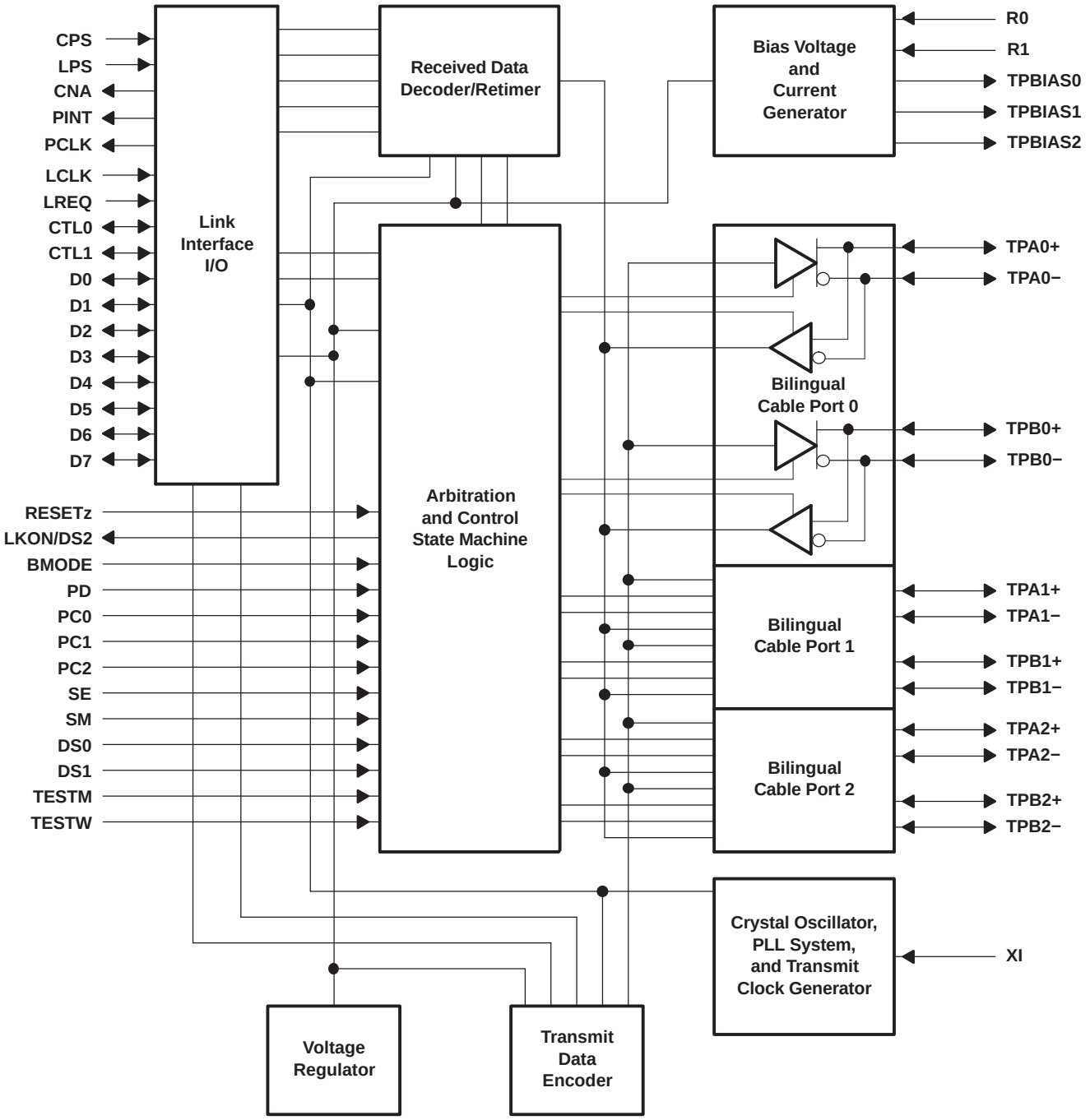


ZAJ PACKAGE
(TOP VIEW)



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FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL					DESCRIPTION
		PFP PACKAGE	ZAJ PACKAGE		
NAME	TYPE	NO.	NO.	I/O	
AGND(1)	Supply	21, 40, 43, 50, 61, 62	See DGND	–	Analog circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
AVDD-3.3	Supply	24, 39, 44, 51, 57, 63	M4, F10, H10, J10, E10	–	Analog circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10-μF filtering capacitors are also recommended. These supply terminals are separated from the PLLVDD-CORE, PLLVDD-3.3, DVDD-CORE, and DVDD-3.3 terminals internal to the device to provide noise isolation. The PLLVDD-3.3, AVDD, and DVDD-3.3 terminals must be tied together with a low dc impedance connection on the circuit board.
BMODE	CMOS	74	B6	I	Beta-mode input. This terminal determines the PHY-link interface connection protocol. When logic-high (asserted), the PHY-link interface complies with the 1394b-2002 B PHY-link interface. When logic-low (deasserted), the PHY-link interface complies with the legacy 1394a-2000 standard. When using an LLC such as the 1394b-2002 TSB82AA2, this terminal must be pulled high. When using an LLC such as the 1394a-2000 TSB12LV26, this terminal must be tied low. NOTE: The PHY-link interface cannot be changed between the different protocols during operation.
CNA	CMOS	79	A2	O	Cable not active output. This terminal is asserted high when there are no ports receiving incoming bias voltage. When any port receives bias, this terminal goes low.
CPS	CMOS	34	N9	I	Cable-power status input. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This transition from cable power sensed to cable power not sensed can be used to generate an interrupt to the LLC.
CTL0 CTL1	CMOS	9 10	F1 G1	I/O	Control I/Os. These bidirectional signals control communication between the TSB81BA3E and the LLC. Bus holders are built into these terminals.
D0-D7	CMOS	11, 12, 13, 15, 16, 17, 19, 20	H1, H2, J2, J1, K2, K1, L1, M1	I/O	Data I/Os. These are bidirectional data signals between the TSB82BA3 and the LLC. Bus holders are built into these terminals.
DGND(1)	Supply	4, 14, 38, 64, 72, 76	E5, F4, F5, F6, F7, F9, G4, G5, G6, G7, G8, G9, G10, H4, H5, H6, H7, H8, J4, J5, J6, J7, J8, K7, L7	–	Digital circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
DS0	CMOS	33	N8	I	Data-strobe-only mode for port 0. 1394a-only port 0 enable programming terminal. On hardware reset, this terminal allows the user to select whether port 0 acts like a 1394b bilingual port (terminal at logic 0) or as a 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or less resistor (to enable 1394b bilingual mode) or high through a 1-kΩ or less resistor (to enable 1394a-2000-only mode). A bus holder is built into this terminal.
DS1	CMOS	32	M7	I	Data-strobe-only mode for port 1. 1394a-only port 1 enable programming terminal. On hardware reset, this terminal allows the user to select whether port 1 acts like a 1394b bilingual port (terminal at logic 0) or as a 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or less resistor (to enable 1394b bilingual mode) or high through a 1-kΩ or less resistor (to enable 1394a-2000-only mode). A bus holder is built into this terminal.

(1) All AGND and DGND terminals are internally tied together in the ZAJ package.

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TERMINAL FUNCTIONS (continued)

TERMINAL					DESCRIPTION
		PFP PACKAGE	ZAJ PACKAGE		
NAME	TYPE	NO.	NO.	I/O	
DVDD-CORE	Supply	8, 37, 65, 71	D9, K9, D8	–	Digital core circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. An additional 1-μF capacitor is required for voltage regulation. These supply terminals are separated from the DVDD-3.3, PLLVDD-CORE, PLLVDD-3.3, and AVDD terminals internal to the device to provide noise isolation.
DVDD-3.3	Supply	6, 18, 69, 70	E4, K5, K6	–	Digital 3.3-V circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower-frequency 10-μF filtering capacitors are also recommended. The DVDD-3.3 terminals must be tied together at a low-impedance point on the circuit board. These supply terminals are separated from the PLLVDD-CORE, PLLVDD-3.3, DVDD-CORE, and AVDD terminals internal to the device to provide noise isolation. The PLLVDD-3.3, AVDD, and DVDD-3.3 terminals must be tied together with a low dc impedance connection on the circuit board.
LCLK	CMOS	7	G2	I	Link clock. Link-provided 98.304-MHz clock signal to synchronize data transfers from link to the PHY when the PHY-link interface is in the 1394b mode. A bus holder is built into this terminal.
LKON/DS2	CMOS	2	D2	I/O	Link-on output/Data-strobe-only input for port 2. This terminal may be connected to the link-on input terminal of the LLC through a 1-kΩ resistor if the link-on input is available on the link layer. Data-strobe-only mode for port 2. 1394a-only port 0 enable programming terminal. On hardware reset, this terminal allows the user to select whether port 2 acts like a 1394b bilingual port (terminal at logic 0) or as a 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or less resistor to enable 1394b bilingual mode or high through a 1-kΩ or less resistor to enable 1394a-2000-only mode. A bus holder is built into this terminal. After hardware reset, this terminal is the link-on output, which notifies the LLC or other power-up logic to power up and become active. The link-on output is a square wave signal with a period of approximately 163 ns (8 PCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high impedance. The link-on output is activated if the LLC is inactive (the LPS input inactive or the LCtrl bit cleared) and when one: a. The PHY receives a link-on PHY packet addressed to this node. b. The PEI (port-event interrupt) register bit is 1. c. Any of the CTOI (configuration-timeout interrupt), CPSI (cable-power-status interrupt), or STOI (state-time-out interrupt) register bits is 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. d. The PHY is power-cycled and the power class is 0 through 4. Once activated, the link-on output is active until the LLC becomes active (both the LPS input active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus-reset occurs unless the link-on output is otherwise active because one of the interrupt bits is set (that is, the link-on output is active due solely to the reception of a link-on PHY packet). In the case of power-cycling the PHY, the LKON signal must stop after 167 μs if the preceding conditions have not been met. NOTE: If an interrupt condition exists, which otherwise would cause the link-on output to be activated if the LLC were inactive, then the link-on output is activated when the LLC subsequently becomes inactive.

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TERMINAL FUNCTIONS (continued)

TERMINAL					DESCRIPTION
		PFP PACKAGE	ZAJ PACKAGE		
NAME	TYPE	NO.	NO.	I/O	
LPS	CMOS	80	D3	I	Link power status input. This terminal monitors the active/power status of the link-layer controller (LLC) and controls the state of the PHY-LLC interface. This terminal must be connected to either the V_{DD} supplying the LLC through an approximately 1-kΩ resistor or to a pulsed output that is active when the LLC is powered. A pulsed signal must be used when an isolation barrier exists between the LLC and PHY (see Figure 8). The LPS input is considered inactive if it is sampled low by the PHY for more than an LPS_RESET time (~2.6 μs), and is considered active otherwise (that is, asserted steady high or an oscillating signal with a low time less than 2.6 μs). The LPS input must be high for at least 22 ns to be observed as high by the PHY. When the TSB81BA3E detects that the LPS input is inactive, it places the PHY-LLC interface into a low-power reset state. In the reset state, the CTL (CTL0 and CTL1) and D (D0 to D7) outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than an LPS_DISABLE time (~26 μs), then the PHY-LLC interface is put into a low-power disabled state in which the PCLK output is also held inactive. The LLC state that is communicated in the self-ID packet is considered active only if both the LPS input is active and the LCtrl register bit is set to 1. The LLC state that is communicated in the self-ID packet is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.
LREQ	CMOS	3	E1	I	LLC request input. The LLC uses this input to initiate a service request to the TSB81BA3E. A bus holder is built into this terminal.
PC0 PC1 PC2	CMOS	66 67 68	C11 A9 B8	I	Power class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying the terminals high through a 1-kΩ or smaller resistor or by tying directly to ground through a 1-kΩ or smaller resistor. Bus holders are built into these terminals.
PCLK	CMOS	5	F2	O	PHY clock. Provides a 98.304-MHz clock signal, synchronized with data transfers, to the LLC when the PHY-link interface is operating in the 1394b mode (BMODE asserted). PCLK output provides a 49.152-MHz clock signal, synchronized with data transfers, to the LLC when the PHY-link interface is in legacy 1394a-2000 (BMODE input deasserted).
PD	CMOS	77	B3	I	Power-down input. A high on this terminal turns off all internal circuitry except the cable-active monitor circuits, which control the CNA output. Asserting the PD input high also activates an internal pulldown on the $\overline{\text{RESET}}$ terminal to force a reset of the internal control logic.
PINT	CMOS	1	E3	O	PHY interrupt. The PHY uses this output to serially transfer status and interrupt information to the link when PHY-link interface is in the 1394b mode. A bus holder is built into this terminal.
PLLGND	Supply	25, 28	F8, N4	–	PLL circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
PLLVDD-CORE	Supply	29, 30	N6	–	PLL core circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. An additional 1-μF capacitor is required for voltage regulation. The PLLVDD-CORE terminals must be separate from the DVDD-CORE terminals. These supply terminals are separated from the DVDD-CORE, DVDD-3.

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TERMINAL FUNCTIONS (continued)

TERMINAL					DESCRIPTION
		PFP PACKAGE	ZAJ PACKAGE		
NAME	TYPE	NO.	NO.	I/O	
PLLVDD-3.3	Supply	31	N7	–	PLL 3.3-V circuit power terminal. A combination of high-frequency decoupling capacitors near the terminal are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10-μF filtering capacitors are also recommended. This supply terminal is separated from the DVDD-CORE, DVDD-3.3, PLLVDD-CORE, and AVDD-3.3 terminals internal to the device to provide noise isolation. The DVDD-3.3 terminals must be tied together at a low-impedance point on the circuit board. The PLLVDD-3.3, AVDD-3.3, and DVDD-3.3 terminals must be tied together with a low dc impedance connection.
$\overline{\text{RESET}}$	CMOS	75	A6	I	Logic reset input. Asserting this terminal low resets the internal logic. An internal pullup resistor to V_{DD} is provided so only an external delay capacitor is required for proper power-up operation (see *power-up reset* in the *Applications Information* section). The $\overline{\text{RESET}}$ terminal also incorporates an internal pulldown, which is activated when the PD input is asserted high. This input is otherwise a standard logic input, and can also be driven by an open-drain-type driver.
RSVD	Osc Out	26	M5	O	This terminal must normally be left unconnected. When this terminal is probed, the terminal shows a 98.304-MHz signal. If this is perceived as an EMI problem, then the terminal may be pulled to ground through a 10-kΩ resistor. However, this causes an increase of up to 340 μA in device current consumption.
R0 R1	Bias	23 22	N3 N2	–	Current setting resistor terminals. These terminals are connected to a precision external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ, ±1%, is required to meet the IEEE Std 1394-1995 output voltage limits.
SE	CMOS	35	M10	I	Test control input. This input is used in the manufacturing test of the TSB81BA3E. For normal use this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
SM	CMOS	36	N10	I	Test control input. This input is used in the manufacturing test of the TSB81BA3E. For normal use this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
TESTM	CMOS	78	A3	I	Test control input. This input is used in the manufacturing test of the TSB81BA3E. For normal use this terminal must be pulled high through a 1-kΩ resistor to V_{DD}.
VREG_PD	CMOS	73	B7	I	Voltage regulator power-down input. When asserted logic high, this pin will power-down the internal 3.3V to 1.95V regulator. For single 3.3V supply operation, this pin should be tied to GND. If an external regulator is used to supply the 1.95V PLLVDD-CORE and DVDD-CORE power rails this terminals should be pulled to Vcc through a 1-kΩ resistor to V_{DD}
TPA0– TPA0+ TPB0– TPB0+	Cable	45 46 41 42	K13 J13 M13 L13	I/O	Port-0 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.
TPA1– TPA1+ TPB1– TPB1+	Cable	52 53 48 49	F13 E13 H13 G13	I/O	Port-1 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.
TPA2– TPA2+ TPB2– TPB2+	Cable	58 59 55 56	B13 A13 D13 C13	I/O	Port-2 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.

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TERMINAL FUNCTIONS (continued)

TERMINAL					DESCRIPTION
		PFP PACKAGE	ZAJ PACKAGE		
NAME	TYPE	NO.	NO.	I/O	
TPBIAS0 TPBIAS1 TPBIAS2	Cable	47 54 60	J12 E12 A12	I/O	Twisted-pair bias output and signal detect input. This provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection in 1394a-2000 mode. Each of these terminals, except for an unused port, must be decoupled with a 1-μF capacitor to ground. For the unused port, this terminal can be left unconnected. Please request the S800 1394b layout recommendation documents from your TI representative. When a port is configured as a Beta-mode port (B1, B2, B4) this terminal becomes an input and must be high when a valid signal is present. For optical transceivers, the signal detect of the transceiver must be connected to this terminal. The input is an LVCMOS level input.
XI	Osc In	27	N5	–	Oscillator input. This terminal connects to a 98.304-MHz low jitter external oscillator. The XI terminal is a 1.8-V CMOS input. Oscillator jitter must be 5 ps RMS or better. If only 3.3-V oscillators can be acquired, then great care must be taken to not introduce significant jitter by the means used to level shift from 3.3 V to 1.8 V. If a resistor divider is used, then a high current oscillator and low-value resistors must be used to minimize RC time constants. If a level-shifting circuit is used, then it must introduce very little jitter. Please see layout recommendations document.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range(2)		–0.3	4	V
V_I	Input voltage range(2)		–0.5	V_{DD} + 0.5	V
V_O	Output voltage range at any output		–0.5	V_{DD} + 0.5	V
	Continuous total power dissipation		See Dissipation Ratings Table		
T_A	Operating free-air temperature	TSB81BA3E	0	70	°C
		TSB81BA3EI	–40	85	
T_{stg}	Storage temperature range		65	150	°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground.

Dissipation Ratings

PACKAGE	T_A 25°C POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PFP(2)(3)	5.05 W	52.5 mW/°C	2.69 W	1.9 W
PFP(4)(3)	3.05 W	31.7 mW/°C	1.62 W	1.15 W

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
(2) 2-oz. trace and copper pad with solder.
(3) For more information, see the Texas Instruments application note *PowerPAD™ Thermally Enhanced Package*, (SLMA002).
(4) 2-oz. trace and copper pad without solder.

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RECOMMENDED OPERATING CONDITIONS

			MIN	TYP(1)	MAX	UNIT
3.3 V_{DD}	Supply voltage	Source power node	3.0	3.3	3.6	V
		Nonsource power node	3.0(2)	3.3	3.6	
Core V_{DD}	Supply voltage		1.85	1.95	2.05	V
V_{IH}	High-level input voltage	LREQ, CTL0, CTL1, D0-D7, LCLK	2.6			V
		LKON/DS2, PC0, PC1, PC2, PD, BMODE	0.7 × V_{DD}			
		RESETz	0.6 × V_{DD}			
V_{IL}	Low-level input voltage	LREQ, CTL0, CTL1, D0-D7, LCLK			1.2	V
		LKON/DS2, PC0, PC1, PC2, PD, BMODE			0.2 × V_{DD}	
		RESETz			0.3 × V_{DD}	
V_{OD}	1394b Differential output voltage			700		mV
V_{CM}	1394b Common-mode output voltage			1.5		V
I_{DD}	Supply current in low power/suspend(3)	V_{DD} = 3.3 V		4		mA
		V_{DD} = 3 V		3		mA
$I_{OL/OH}$	Output current	CTL0, CTL1, D0-D7, CNA, LKON/DS2, PINT, and PCLK	–4		4	mA
I_O	Output current	TPBIAS outputs	–5.6		1.3	mA
T_A	Operating ambient temperature range	TSB81BA3E	0		70	°C
T_J	Junction temperature(4)	TSB81BA3E	0		105	°C
V_{ID}	1394b Differential input voltage	Cable inputs, during data reception	200		800	mV
V_{ID}	1394a Differential input voltage	Cable inputs, during data reception	118		260	mV
		Cable inputs, during arbitration	168		265	
V_{IC}	1394a Common-mode input voltage	TPB cable inputs, source power node	0.4706		2.515	V
		TPB cable inputs, nonsource power node	0.4706		2.015(2)	
t_{pu}	Power-up reset time	RESETz input	2(5)			ms
	Receive input jitter	TPA, TPB cable inputs, S100 operation			±1.08	ns
		TPA, TPB cable inputs, S200 operation			±0.5	
		TPA, TPB cable inputs, S400 operation			±0.315	
	Receive input skew	Between TPA and TPB cable inputs, S100 operation			±0.8	ns
		Between TPA and TPB cable inputs, S200 operation			±0.55	
		Between TPA and TPB cable inputs, S400 operation			±0.5	

(1) All typical values are at V_{DD} = 3.3 V and T_A = 25°C.
(2) For a node that does not source power, see Section 4.2.2.2 in IEEE 1394a-2000.
(3) The low power/suspend mode assumes that the device is not receiving packets and it is toning.
(4) The junction temperature reflects simulated conditions. The customer is responsible for verifying junction temperature.
(5) Time after valid clock received at PHY XI input terminal.

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ELECTRICAL CHARACTERISTICS

Driver

over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	56 Ω, See Figure 1	172		265	mV
I_{DIFF}	Driver difference current, TPA+, TPA–, TPB+, TPB–	Drivers enabled, speed signaling off	–1.05(1)		1.05(1)	mA
I_{SP200}	Common-mode speed signaling current, TPB+, TPB–	S200 speed signaling enabled	–4.84(2)		–2.53(2)	mA
I_{SP400}	Common-mode speed signaling current, TPB+, TPB–	S400 speed signaling enabled	–12.4(2)		–8.1(2)	mA
V_{OFF}	Off-state differential voltage	Drivers disabled, See Figure 1			20	mV

(1) Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
(2) Limits defined as absolute limit of each of TPB+ and TPB– driver currents.

Receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	4	7		kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	–30		30	mV
V_{TH-CB}	Cable bias detect threshold, TPBx cable inputs	Drivers disabled	0.6		1	V
V_{TH+}	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
V_{TH-}	Negative arbitration comparator threshold voltage	Drivers disabled	–168		–89	mV
$V_{TH-SP200}$	Speed signal threshold	TPBIAS-TPA common-mode voltage, drivers disabled	49		131	mV
$V_{TH-SP400}$	Speed signal threshold		314		396	mV

Device

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	3.3 V_{DD}	(1)			120	150	mA
		Core V_{DD}				79		
V_{TH}	Power status threshold, CPS input(2)		400-kΩ resistor(2)		4.7		7.5	V
V_{OH}	High-level output voltage, CTL0, CTL1, D0-D7, PCLK, LKON/DS2 outputs		V_{DD} = 3 to 3.6 V, I_{OH} = 4 mA		2.8			V
V_{OL}	Low-level output voltage, CTL0, CTL1, D0-D7, PCLK, LKON/DS2 outputs		I_{OL} = 4 mA				0.4	V
I_{BH+}	Positive peak bus holder current, D0-D7, CTL0-CTL1, LREQ		V_{DD} = 3.6 V, V_I = 0 V to V_{DD}		0.05		1	mA
I_{BH-}	Negative peak bus holder current, D0-D7, CTL0-CTL1, LREQ		V_{DD} = 3.6 V, V_I = 0 V to V_{DD}		–1.0		–0.05	mA
I_{OZ}	Off-state output current, CTL0, CTL1, D0-D7, LKON/DS2 I/Os		V_O = V_{DD} or 0 V	TSB81BA3E			±5	µA
				TSB81BA3EI			±20	
I_{IRST}	Pullup current, $\overline{\text{RESET}}$ input		V_I = 1.5 V or 0 V		–90		–20	µA
V_O	TPBIAS output voltage		At rated I_O current		1.665		2.015	V

(1) Repeat max packet (one port receiving maximum size isochronous packet–8192 bytes, sent on every isochronous interval, S800, data value of 0xCCCCCCCCh; two ports repeating; all ports with beta-mode connection), $V_{DD3.3}$ = 3.3 V, V_{DDCORE} = 1.95 V, T_A = 25°C.
(2) Measured at cable-power side of resistor.

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Electrical Characteristics (continued)
Thermal Characteristics

PARAMETER		TEST CONDITIONS[1]		TYP PFP Package	TYP ZAJ Package	UNIT
θ_{ja}	Junction-to-free-air thermal resistance	Low K JEDEC Test Board, 1s (single signal layer), no air flow		50	88.7	°C/W
θ_{ja}	Junction-to-free-air thermal resistance	High K JEDEC Test Board 2s2p (double signal layer, double buried power plane)	No air flow	24.8	46.2	°C/W
			400 LFM			
			200 LFM			
θ_{jc}	Junction-to-case-thermal resistance	Cu Cold Plate Measurement Process		21.5	23.5	°C/W
θ_{jb}	Junction-to-board thermal resistance	EIA/JESD 51-8		8.37	27.8	
Ψ_{jt}	Junction-to-top of package	EIA/JESD 51-2		0.46	0.45	°C/W
Ψ_{jb}	Junction-to-board	EIA/JESD 51-6		8.2	27.4	°C/W

(1) For more details, please refer to TI application note on IC Package Thermal Metrics (SPRA953A)

Switching Characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	TP differential rise time, transmit		10% to 90%,	At 1394 connector	0.5		1.2	ns
t_f	TP differential fall time, transmit		90% to 10%,	At 1394 connector	0.5		1.2	ns
t_{su}	Setup time, CTL0, CTL1, D1-D7, LREQ to PCLK	1394a-2000	50% to 50%,	See Figure 2	2.5			ns
t_h	Hold time, CTL0, CTL1, D1-D7, LREQ after PCLK	1394a-2000	50% to 50%,	See Figure 2	0			ns
t_{su}	Setup time, CTL0, CTL1, D1-D7, LREQ to LCLK_PMC	1394b	50% to 50%,	See Figure 2	2.5			ns
t_h	Hold time, CTL0, CTL1, D1-D7, LREQ after LCLK_PMC	1394b	50% to 50%,	See Figure 2	0			ns
t_d	Delay time, PCLK to CTL0, CTL1, D1-D7, PINT	1394a-2000 and 1394b	50% to 50%,	See Figure 3	0.5		7	ns

PARAMETER MEASUREMENT INFORMATION

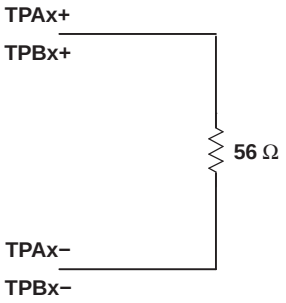


Figure 1. Test Load Diagram

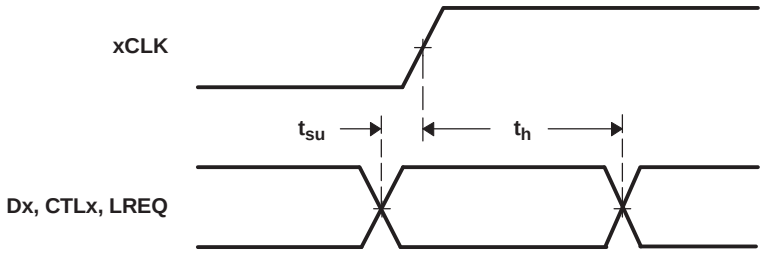


Figure 2. Dx, CTLx, LREQ Input Setup and Hold Time Waveforms

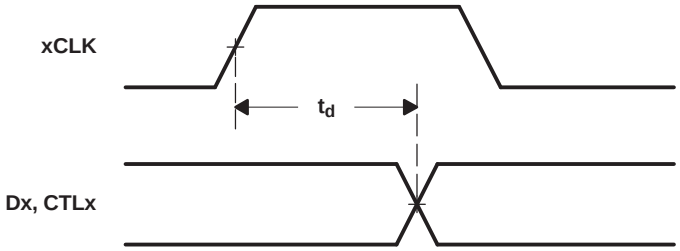


Figure 3. Dx and CTLx Output Delay Relative to xCLK Waveforms

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APPLICATION INFORMATION

Please obtain from the TI website or your local TI representative the reference schematics, reference layouts, debug documents, and software recommendations for the TSB81BA3E.

Internal Register Configuration

There are 16 accessible internal registers in the TSB81BA3E. The configuration of the registers at addresses 0h through 7h (the base registers) is fixed, while the configuration of the registers at addresses 8h through Fh (the paged registers) is dependent upon which 1 of 8 pages, numbered 0h through 7h, is currently selected. The selected page is set in base register 7h. Note that while this register set is compatible with 1394a--2000 register sets, some fields have been redefined and this register set contains additional fields.

Table 1 shows the configuration of the base registers, and Table 2 gives the corresponding field descriptions. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2 through 6 are reserved.

Table 1. Base Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Num_Ports (0011b)				
0011	PHY_Speed (111b)			SREN	Delay (1111b)			
0100	LCtrl	C	Jitter (000b)			Pwr_Class		
0101	WDIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Max Legacy SPD			BLINK	Bridge		Rsvd	
0111	Page_Select			Rsvd	Port_Select			

Table 2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus reset until the self-ID has completed as indicated by an unsolicited register 0 status transfer from the PHY to the LLC.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial bus cable power through a 400-kΩ resistor. A 0 in this bit indicates that the cable-power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus reset. The RHB bit is reset to 0 by a hardware reset and is unaffected by a bus reset. If two nodes on a single bus have their root holdoff bit set, then the result is not defined. To prevent two nodes from having their root-holdoff bit set, this bit must only be written using a PHY configuration packet.
IBR	1	Rd/Wr	Initiate bus reset. This bit instructs the PHY to initiate a long (166-µs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus reset is initiated. The IBR bit is reset to 0 after a hardware reset or a bus reset. Care must be exercised when writing to this bit to not change the other bits in this register. It is recommended that whenever possible a bus reset be initiated using the ISBR bit and not the IBR bit.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value sets the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet). **It is strongly recommended that this field only be changed using PHY configuration packets.**
Extended	3	Rd	Extended register definition. For the TSB81BA3E, this field is 111b, indicating that the extended register set is implemented.

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Table 2. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Num_Ports	4	Rd	Number of ports. For the TSB81BA3E, this field indicates the number of ports implemented in the PHY. This field is 3.
PHY_Speed	3	Rd	PHY speed capability. For the TSB81BA3E, this field is no longer used. This field is 111b. Speeds for 1394b PHYs must be checked on a port-by-port basis.
Delay	4	Rd	PHY repeater data delay. This field indicates the worst-case repeater data delay of the PHY, expressed as 144+ (delay × 20) ns. For the TSB81BA3E, this field is 02h. This value is the repeater delay for the S400B case, which is slower than the S800B or 1394a cases. Since the IEEE 1394B−2002 Std Phy register set only has a single field for the delay parameter, the slowest value is used. If a network uses only S800B or 1394a connections, then a delay value of 00h may be used. The worst case Phy repeater delay is 197 ns for S400B and 127 ns for S800B cable speeds (trained, raw bit speed).
LCtrl	1	Rd/Wr	Link-active status control. This bit controls the indicated active status of the LLC reported in the self-ID packet. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC bit in the node self-ID packet is set active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software-controllable means to indicate the LLC self-ID active status in lieu of using the LPS input terminal. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus reset. NOTE: The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information continue to be presented on the interface, and any requests indicated on the LREQ input are processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to 0 on hardware reset. After hardware reset, this bit can only be set via a software register write. This bit is unaffected by a bus reset.
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst-case difference between the fastest and slowest repeater data delay, expressed as (jitter+1) × 20 ns. For the TSB81BA3E, this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node power consumption and source characteristics and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is reset to the state specified by the PC0-PC2 input terminals upon a hardware reset, and is unaffected by a bus reset. See Table 9.
WDIE	1	Rd/Wr	Watchdog interrupt enable. This bit, if set to 1, enables the port event interrupt (PIE) bit to be set when resume operations begin on any port, or when any of the CTOI, CPSI, or STOI interrupt bits are set and the link interface is nonoperational. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus reset. This bit, if set to 1, instructs the PHY to initiate a short (1.3 μs) arbitrated bus reset at the next opportunity. This bit is reset to 0 by a bus reset. It is recommended that short bus reset is the only reset type initiated by software. IEC 61883-6 requires that a node initiate short bus resets to minimize any disturbance to an audio stream. NOTE: Legacy IEEE Std 1394-1995-compliant PHYs are not capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times out during tree-ID start and might indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the CTOI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the LKON/DS2 output to notify the LLC to service the interrupt. NOTE: If the network is configured in a loop, then only those nodes that are part of the loop generate a configuration time-out interrupt. All other nodes instead time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus reset. This bit is only set when the bus topology includes 1394a nodes; otherwise, 1394b loop healing prevents loops from being formed in the topology.
CPSI	1	Rd/Wr	Cable power status interrupt. This bit is set to 1 when the CPS input transitions from high to low, indicating that cable power might be too low for reliable operation. This bit is reset to 1 by hardware reset. It can be cleared by writing a 1 to this register bit. If the CPSI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the LKON/DS2 output to notify the LLC to service the interrupt.

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Table 2. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus reset to occur). This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the STOI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the LKON/DS2 output to notify the LLC to service the interrupt.
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 on any change in the connected, bias, disabled, or fault bits for any port for which the port interrupt enable (PEI) bit is set. Additionally, if the resuming port interrupt enable (WDIE) bit is set, then the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in 1394a-2000 (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in 1394b mode. NOTE: The use of accelerated arbitration is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. The EAA bit is set only if the attached LLC is 1394a-2000-compliant. If the LLC is not 1394a-2000 or 1394b-2002-compliant, then the use of the arbitration acceleration enhancements can interfere with isochronous traffic by excessively delaying the transmission of cycle-start packets.
EMC	1	Rd/Wr	Enable multispeed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in 1394a-2000. This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in 1394b mode. NOTE: The use of multispeed concatenation is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. However, use of multispeed concatenation requires that the attached LLC be 1394a-2000 or 1394b-2002-compliant.
Max Legacy SPD	3	Rd	Maximum legacy-path speed. This field holds the maximum speed capability of any legacy node (1394a-2000 or 1394-1995-compliant) as indicated in the self-ID packets received during bus initialization. Encoding is the same as for the PHY_SPEED field (but limited to S400 maximum).
BLINK	1	Rd	Beta-mode link. This bit indicates that a Beta-mode-capable link is attached to the PHY. This bit is set by the BMODE input terminal on the TSB81BA3E.
Bridge	2	Rd/Wr	This field controls the value of the bridge (brdg) field in self-ID packet. The power reset value is 0. Details for when to set these bits are specified in the IEEE 1394.1 bridging specification.
Page_Select	3	Rd/Wr	Page_Select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by a hardware reset and is unaffected by bus reset.
Port_Select	4	Rd/Wr	Port_Select. This field selects the port when accessing per-port status or control (for example, when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus reset.

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. Table 3 shows the configuration of the port status page registers, and Table 4 gives the corresponding field descriptions. If the selected port is unimplemented, then all registers in the port status page are read as 0.

Table 3. Page 0 (Port Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Astat		Bstat		Ch	Con	RxOK	Dis
0001	Negotiated_speed			PIE	Fault	Standby_fault	Disscrm	B_Only (0)
0010	DC_connected	Max_port_speed			LPP	Cable_speed		
0011	Connection_unreliable	Reserved			Beta_mode	Reserved		
0100	Port_error							
0101	Reserved					Loop_disable	In_standby	Hard_disable
0110	Reserved							
0111	Reserved							

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Table 4. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Astat	2	Rd	TPA line state. This field indicates the instantaneous TPA line state of the selected port, encoded as follows: **Code** **Arb Value** 11 Z 01 1 10 0 00 invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the Astat field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus reset. NOTE: The Con bit indicates that the port is physically connected to a peer PHY, but this does not mean that the port is necessarily active. For 1394b-coupled connections, the Con bit is set when a port detects connection tones from the peer PHY and operating-speed negotiation is completed.
RxOK	1	Rd	Receive OK. In 1394a-2000 mode this bit indicates the reception of a debounced TPBias signal. In Beta mode, this bit indicates the reception of a continuous electrically valid signal. Note: RxOK is set to false during the time that only connection *tones* are detected in Beta mode.
Dis	1	Rd/Wr	Port disabled control. If this bit is 1, then the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset. When this bit is set, the port cannot become active; however, the port still tones, but does not establish an active connection.
Negotiated_speed	3	Rd	Indicates the maximum speed negotiated between this PHY port and its immediately connected port. The encoding is as for Max_port_speed. It is set during connection when in Beta mode or to a value established during self-ID when in 1394a-2000 mode.
PIE	1	Rd/Wr	Port-event-interrupt enable. When this bit is 1, a port event on the selected port sets the port-event-interrupt (PEI) bit and notifies the link. This bit is reset to 0 by a hardware reset and is unaffected by bus reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume fault or suspend fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
Standby_fault	1	Rd/Wr	This bit is set to 1 if an error is detected during a standby operation and cleared on exit from the standby state. A write of 1 to this bit or receipt of the appropriate remote command packet clears it to 0. When this bit is cleared, standby errors are cleared.
Disscrm	1	Rd/Wr	Disable scrambler. If this bit is set to 1, then the data sent during packet transmission is not scrambled.
B_Only	1	Rd	Beta-mode operation only. For the TSB81BA3E, this bit is set to 0 for all ports.
DC_connected	1	Rd	If this bit is set to 1, the port has detected a dc connection to the peer port by means of a 1394a-style connect-detect circuit.

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Table 4. Page 0 (Port Status) Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Max_port_speed	3	Rd/Wr	Max_port_speed The maximum speed at which a port is allowed to operate in Beta mode. The encoding is: 000 = S100 001 = S200 010 = S400 011 = S800 100 = S1600 101 = S3200 110 = reserved 111 = reserved An attempt to write to the register with a value greater than the hardware capability of the port results in the maximum value that the port is capable of being stored in the register. The port uses this register only when a new connection is established in the Beta mode or when a port is programmed as a Beta-only port. When a port is programmed as a bilingual port, it is fixed at S400 for the Beta speed and is not updated by a write to this register. The power reset value is the maximum speed capable of the port. Software can modify this value to force a port to train at a lower-than-maximum speed (when in a Beta-only mode), but no lower than the minimum speed.
LPP(Local_plug_present)	1	Rd	This flag is set permanently to 1.
Cable_speed	3	Rd	This variable is set to the maximum speed that the port is capable of. The encoding is the same as for Max_port_speed.
Connection_unreliable	1	Rd/Wr	If this bit is set to 1, then a Beta-mode speed negotiation has failed or synchronization has failed. A write of 1 to this field resets the value to 0.
Beta_mode	1	Rd	Operating in Beta mode. If this bit is 1, the port is operating in Beta mode; it is equal to 0 otherwise (that is, when operating in 1394a-2000 mode, or when disconnected). If Con is 1, RxOK is 1, and Beta_mode is 0, then the port is active and operating in the 1394a-2000 mode.
Port_error	8	Rd/Wr	Incremented when the port receives an invalid codeword, unless the value is already 255. Cleared when read (including being read by means of a remote access packet). Intended for use by a single bus-wide diagnostic program.
Loop_disable	1	Rd	This bit is set to 1 if the port has been placed in the loop-disable state as part of the loop-free build process (the PHYs at either end of the connection are active, but if the connection itself were activated, then a loop would exist). Cleared on bus reset and on disconnection.
In_standby	1	Rd	This bit is set to 1 if the port is in standby power-management state.
Hard_disable	1	Rd/Wr	No effect unless the port is disabled. If this bit is set to 1, the port does not maintain connectivity status on an ac connection when disabled. The values of the Con and RxOK bits are forced to 0. This flag can be used to force renegotiation of the speed of a connection. It can also be used to place the device into a lower-power state because when hard-disabled, a port no longer tones to maintain 1394b ac-connectivity status.

The vendor identification page identifies the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. Table 5 shows the configuration of the vendor identification page, and Table 6 shows the corresponding field descriptions.

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Table 5. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Compliance							
0001	Reserved							
0010	Vendor_ID0							
0011	Vendor_ID1							
0100	Vendor_ID2							
0101	Product_ID0							
0110	Product_ID1							
0111	Product_ID2							

Table 6. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the TSB81BA3E, this field is 02h, indicating compliance with the 1394b-2002 specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the TSB81BA3E, this field is 08_00_28h (Texas Instruments) (the MSB is at register address 1010b).
Product_ID	24	Rd	Product identifier. For the TSB81BA3E, this field can be either 83_13_07h (the MSB is at register address 1101b).

The vendor-dependent page provides access to the special control features of the TSB81BA3E, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. Table 7 shows the configuration of the vendor-dependent page and Table 8 shows the corresponding field descriptions.

Table 7. Page 7 (Vendor-Dependent) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Reserved						Reserved	
0001	Reserved for test							
0010	Reserved for test							
0011	Reserved for test							
0100	Reserved for test							
0101	Reserved for test							
0110	SWR	Reserved for test						
0111	Reserved for test							

Table 8. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
SWR	1	Rd/Wr	Software hard reset. Writing a 1 to this bit forces a hard reset of the PHY (same effect as momentarily asserting the $\overline{\text{RESET}}$ terminal low). This bit is always read as a 0.

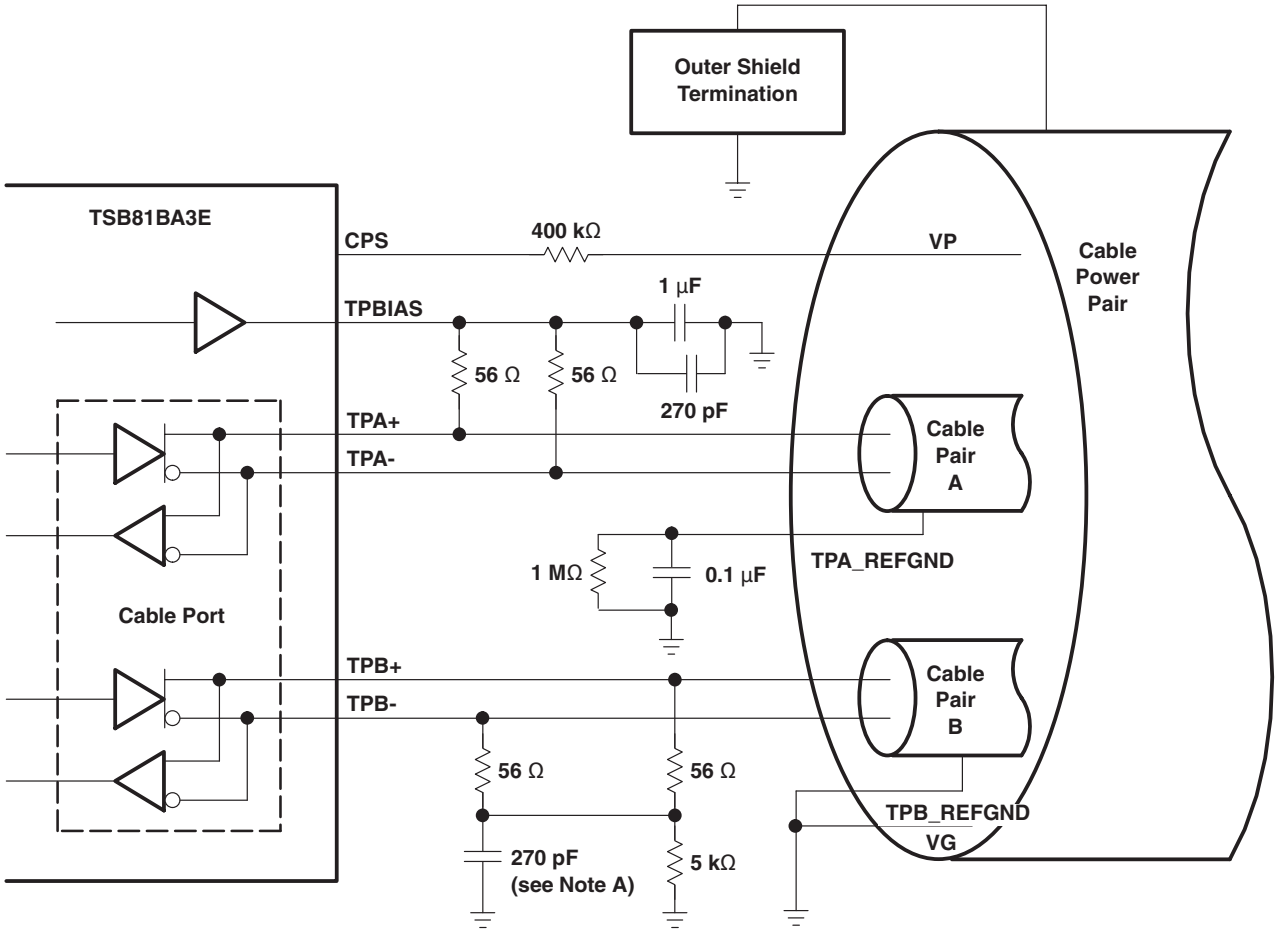
Power-Class Programming

The PC0-PC2 terminals are programmed to set the default value of the power-class indicated in the pwr field (bits 21−23) of the transmitted self-ID packet. Descriptions of the various power-classes are given in Table 9. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

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Table 9. Power-Class Descriptions

PC0-PC2	DESCRIPTION
000	Node does not need power and does not repeat power
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node can be powered from the bus and is using up to 3 W; no additional power is needed to enable the link. The node can also provide power to the bus. The amount of bus power that it provides can be found in the configuration ROM.
101	Reserved for future standardization.
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.



NOTE A: The IEEE Std 1394- 1995 calls for a 250-pF capacitor, which is a nonstandard component value. A 270-pF capacitor is recommended.

Figure 4. Typical TP Cable Connections

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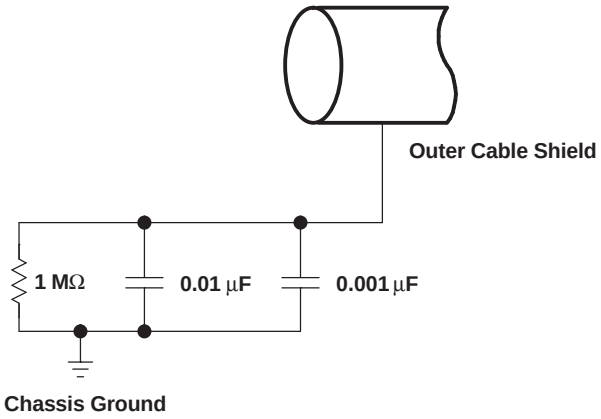


Figure 5. Typical DC-Isolated Outer Shield Termination

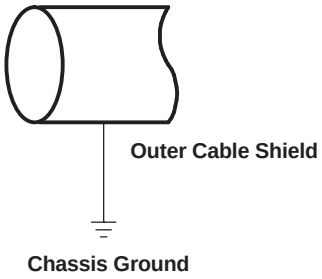


Figure 6. Non-DC-Isolated Outer Shield Termination

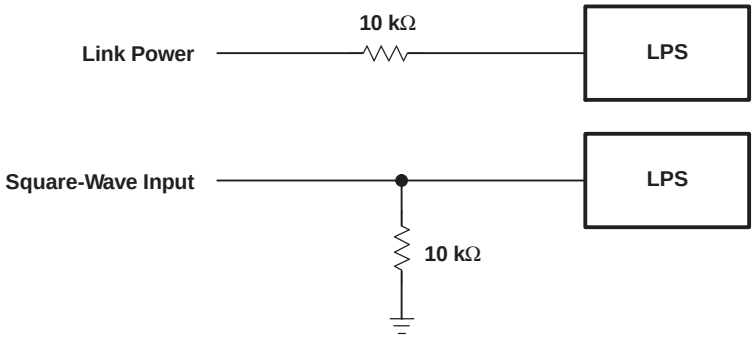


Figure 7. Nonisolated Connection Variations for LPS

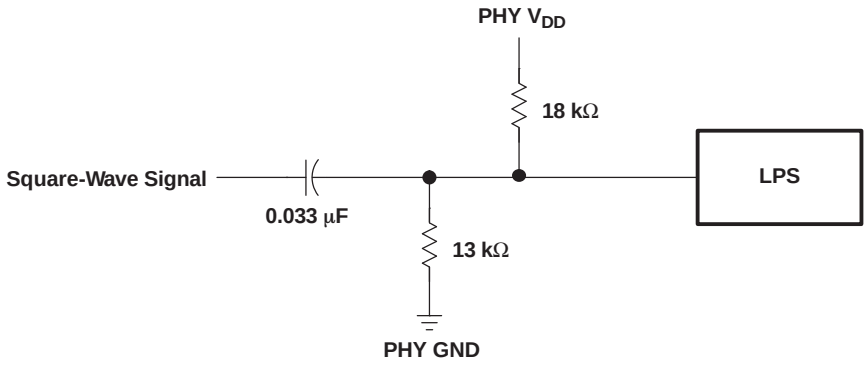


Figure 8. Isolated Circuit Connection for LPS

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Designing With PowerPAD™ Devices (PFP Package Only)

The TSB81BA3E is housed in a high performance, thermally enhanced, 80-terminal PFP PowerPAD™ package. Use of the PowerPAD™ package does not require any special considerations except to note that the PowerPAD™, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD™ PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD™ of connection etches or vias under the package. The recommended option, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the maximum size required for the keepout area for the 80-terminal PFP PowerPAD™ package is 10 mm × 10 mm. The actual PowerPAD™ size for the TSB81BA3E is 6 mm × 6 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD™ package. The thermal land varies in size, depending on the PowerPAD™ package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the Texas Instruments *PowerPAD™ Thermally Enhanced Package* application report (SLMA002) available via the Texas Instruments web page at http://www.ti.com.

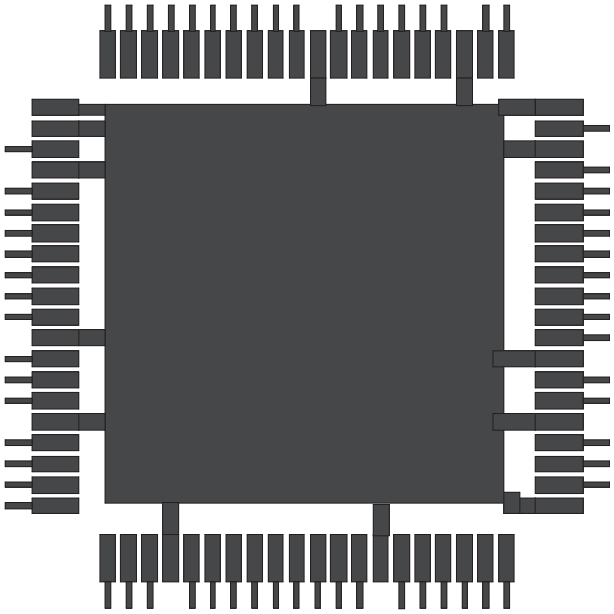


Figure 9. Example of a Thermal Land for the TSB81BA3E PHY

The thermal land must be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size ought to be as large as possible without shorting the device signal terminals. The thermal land can be soldered to the exposed thermal pad using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout* (SLLA020).

Using the TSB81BA3E with a Non-1394b Link Layer

The TSB81BA3E implements the PHY-LLC interface specified in the 1394b Supplement. This interface is based on the interface described in Section 14 of IEEE P1394b (draft 1.33). When using a LLC compliant with this interface, the BMODE input must be tied high.

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The TSB81BA3E also functions with a LLC that is compliant with the older 1394 standards. This interface is compatible with both the older Annex J interface specified in the IEEE Std 1394--1995 (with the exception of the Annex J isolation interfacing method) and the PHY-LLC interface specified in 1394a--2000. When using a LLC compliant with this interface, the BMODE input must be tied low.

Using the TSB81BA3E With a 1394-1995 or 1394a-2000 Link Layer

When the BMODE input is tied low, the TSB81BA3E implements the PHY-LLC interface specified in the 1394a-2000 Supplement. This interface is based on the interface described in informative Annex J of IEEE Std 1394-1995, which is the interface used in the oldest Texas Instruments PHY devices. The PHY-LLC interface specified in 1394a-2000 is compatible with the older Annex J. However, the TSB81BA3E does not support the Annex J isolation interfacing method. When implementing the 1394a-2000 interface, certain signals are not used:

- The PINT output (terminal 1) can be left open.
- The LCLK_PMC input (terminal 7) must be tied directly to ground or through a pulldown resistor of ~1 kΩ or less, unless the PMC mode is desired (see LCLK_PMC terminal description).

All other signals are connected to their counterparts on the 1394a link-layer controller. The PCLK output corresponds to the SCLK input signal on most LLCs.

The 1394a-2000 Supplement includes enhancements to the Annex J interface that should be comprehended when using the TSB81BA3E with a 1394-1995 LLC device.

- A new LLC service request was added which allows the LLC to temporarily enable and disable asynchronous arbitration accelerations. If the LLC does not implement this new service request, then the arbitration enhancements must not be enabled (see the EAA bit in PHY register 5).
- The capability to perform multispeed concatenation (the concatenation of packets of differing speeds) was added to improve bus efficiency (primarily during isochronous transmission). If the LLC does not support multispeed concatenation, then multispeed concatenation must not be enabled in the PHY (see the EMC bit in PHY register 5).
- To accommodate the higher transmission speeds expected in future revisions of the standard, 1394a-2000 extended the speed code in bus requests from 2 bits to 3 bits, increasing the length of the bus request from 7 bits to 8 bits. The new speed codes were carefully selected so that new 1394a-2000 PHY and LLC devices would be compatible, for speeds from S100 to S400, with legacy PHY and LLC devices that use the 2-bit speed codes. The TSB81BA3E correctly interprets both 7-bit bus requests (with 2-bit speed code) and 8-bit bus requests (with 3-bit speed codes). Moreover, if a 7-bit bus request is immediately followed by another request (for example, a register read or write request), then the TSB81BA3E correctly interprets both requests. Although the TSB81BA3E correctly interprets 8-bit bus requests, a request with a speed code exceeding S400 while in 1394a-2000 PHY-link interface mode results in the TSB81BA3E transmitting a null packet (data prefix followed by data end, with no data in the packet).

Power-Up Reset

To ensure proper operation of the TSB81BA3E, the $\overline{\text{RESET}}$ terminal must be asserted low for a minimum of 2 ms from the time that PHY power reaches the minimum required supply voltage and the input clock to the PHY is valid. When using a passive capacitor on the $\overline{\text{RESET}}$ terminal to generate a power-on-reset signal, the minimum reset time is ensured if the value of the capacitor satisfies the following equation (the value must be no smaller than approximately 0.1 μF):

$$C_{min} = (0.0077 \times T) + 0.085 + (\text{external_oscillator_start-up_time} \times 0.05)$$

where C_{min} is the minimum capacitance on the RESETz terminal in μF, T is the V_{DD} ramp time, 10%−90%, in ms, external_oscillator_start-up_time is the time from power applied to the external oscillator till the oscillator outputs a valid clock in ms. If a fundamental mode crystal is used rather than an oscillator then the start−up time parameter may be set to zero.

Crystal Selection

The TSB81BA3E is designed to use an external 98.304-MHz crystal oscillator connected to the XI terminal to provide the reference clock. This clock, in turn, drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S800 media data rates.

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A variation of less than ±100 ppm from nominal for the media data rates is required by IEEE Std 1394. Adjacent PHYs may therefore have a difference of up to 200 ppm from each other in their internal clocks, and PHYs must be able to compensate for this difference over the maximum packet length. Larger clock variations may cause resynchronization overflows or underflows, resulting in corrupted packet data.

For the TSB81BA3E, the PCLK output may be used to measure the frequency accuracy and stability of the internal oscillator and PLL from which it is derived. When operating the PHY-LLC interface with a non-1394b LLC, the frequency of the PCLK output must be within ±100 ppm of the nominal frequency of 49.152 MHz. When operating the PHY-LLC interface with a 1394b LLC, the frequency of the PCLK output must be within ±100 ppm of the nominal frequency of 98.304 MHz.

The following are some typical specifications for an oscillator used with the TSB81BA3E physical layer from TI to achieve the required frequency accuracy and stability:

- RMS jitter of 5 picoseconds or better
- RMS phase noise jitter of 1 picosecond or less over the range 12 kHz to 20 MHz or better
- Frequency tolerance at 25°C: Total frequency variation for the complete circuit is ±100 ppm. A device with ±30 ppm or ±50 ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A device with ±30 ppm or ±50 ppm frequency stability is recommended for adequate margin.

NOTE:

The total frequency variation must be kept below ±100 ppm from nominal with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability may be made as long as the total frequency variation is less than ±100 ppm. For example, the frequency tolerance of the crystal may be specified at 50 ppm and the temperature tolerance may be specified at 30 ppm to give a total of 80 ppm possible variation due to the oscillator alone. Aging also contributes to the frequency variation.

It is strongly recommended that part of the verification process for the design is to measure the frequency of the PCLK output of the PHY. This should be done with a frequency counter with an accuracy of 6 digits or better.

Bus Reset

It is recommended, that when the user has a choice, the user should initiate a bus reset by writing to the initiate-short-bus-reset (ISBR) bit (bit 1, PHY register 0101b). Care must be taken to not change the value of any of the other writeable bits in this register when the ISBR bit is written to.

In the TSB81BA3E, the initiate-bus-reset (IBR) bit can be set to 1 to initiate a bus reset and initialization sequence; however, it is recommended to use the ISBR bit instead. The IBR bit is located in PHY register 1 along with the root-holdoff bit (RHB) and gap-count register. As required by the 1394b Supplement, this configuration maintains compatibility with older Texas Instruments PHY designs which were based on either the suggested register set defined in Annex J of IEEE Std 1394-1995 or the 1394a-2000 Supplement. Therefore, whenever the IBR bit is written, the RHB and gap-count register are also necessarily written.

It is recommended that the RHB and gap-count register only be updated by PHY configuration packets. The TSB81BA3E is 1394a- and 1394b-compliant, and therefore, both the reception and transmission of PHY configuration packets cause the RHB and gap-count register to be loaded, unlike older IEEE Std 1394-1995-compliant PHYs which decode only received PHY configuration packets.

The gap-count register is set to the maximum value of 63 after two consecutive bus resets without an intervening write to the gap-count register, either by a write to PHY register 1 or by a PHY configuration packet. This mechanism allows a PHY configuration packet to be transmitted and then a bus reset to be initiated so as to verify that all nodes on the bus have updated their RHBs and gap-count register values, without having the gap-count register set back to 63 by the bus reset. The subsequent connection of a new node to the bus, which initiates a bus reset, then causes the gap-count register of each node to be set to 63. Note, however, that if a subsequent bus reset is instead initiated by a write to register 1 to set the IBR bit, then all other nodes on the bus have their gap-count register values set to 63, while this node's gap-count register remains set to the value just loaded by the write to PHY register 1.

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Therefore, in order to maintain consistent gap-count registers throughout the bus, the following rules apply to the use of the IBR bit, RHB, and gap-count register in PHY register 1:

- Following the transmission of a PHY configuration packet, a bus reset must be initiated to verify that all nodes have correctly updated their RHBs and gap-count register values, and to ensure that a subsequent new connection to the bus causes the gap-count register to be set to 63 on all nodes in the bus. If this bus reset is initiated by setting the IBR bit to 1, then the RHB and gap-count register must also be loaded with the correct values consistent with the just-transmitted PHY configuration packet. In the TSB81BA3E, the RHB and gap-count register have been updated to their correct values on the transmission of the PHY configuration packet and so these values can first be read from register 1 and then rewritten.
- Other than to initiate the bus reset, which must follow the transmission of a PHY configuration packet, when the IBR bit is set to 1 to initiate a bus reset, the gap-count register value must also be set to 63 to be consistent with other nodes on the bus, and the RHB must be maintained with its current value.
- The PHY register 1 must not be written to except to set the IBR bit. The RHB and gap-count register must not be written without also setting the IBR bit to 1.
- To avoid these problems, all bus resets initiated by software must be initiated by writing the ISBR bit (bit 1 PHY register 0101b). Care must be taken to not change the value of any of the other writeable bits in this register when the ISBR bit is written to. Also, the only means to change the gap count of any node must be by means of the PHY configuration packet, which changes all nodes to the same gap count.

PRINCIPLES OF OPERATION (1394a-2000 INTERFACE)

The TSB81BA3E is designed to operate with an LLC such as the Texas Instruments TSB12LV21B, TSB12LV26, TSB12LV32, TSB42AA4, or TSB12LV01B when the BMODE terminal is tied low. Details of operation for the Texas Instruments LLC devices are found in the respective LLC data sheets. The following paragraphs describe the operation of the PHY-LLC interface. This interface is formally defined in IEEE 1394a-2000, Section 5A.

The interface to the LLC consists of the PCLK, CTL0-CTL1, D0-D7, LREQ, LPS, and LKON/DS2 terminals on the TSB81BA3E, as shown in Figure 10.

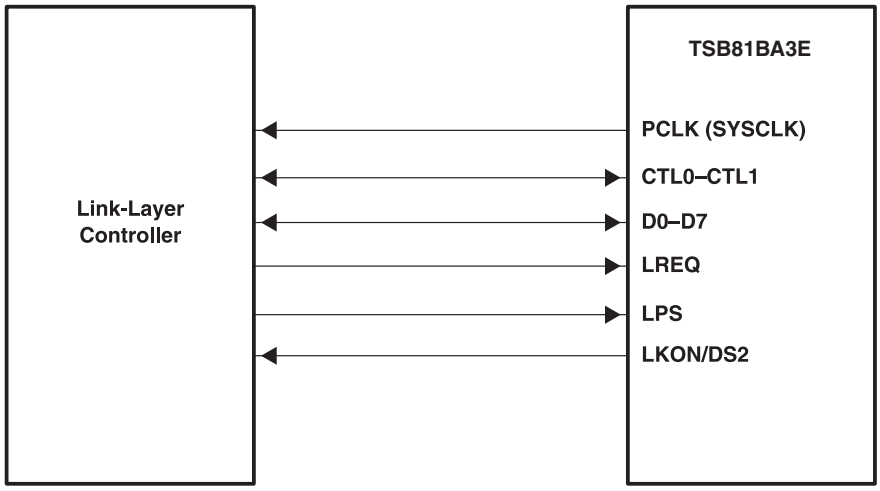


Figure 10. PHY-LLC Interface

The PCLK terminal provides a 49.152-MHz interface system clock. All control and data signals are synchronized to and sampled on the rising edge of PCLK. This terminal serves the same function as the SYSCLK terminal of 1394a-2000-compliant PHY devices.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the TSB81BA3E and LLC.

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The D0-D7 terminals form a bidirectional data bus, which transfers status information, control information, or packet data between the devices. The TSB81BA3E supports S100, S200, and S400 data transfers over the D0-D7 data bus. In S100 operation, only the D0 and D1 terminals are used; in S200 operation, only the D0-D3 terminals are used; and in S400 operation, all D0-D7 terminals are used for data transfer. When the TSB81BA3E is in control of the D0-D7 bus, unused Dn terminals are driven low during S100 and S200 operations. When the LLC is in control of the D0-D7 bus, unused Dn terminals are ignored by the TSB81BA3E.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY to request access to the serial bus for packet transmission, read or write PHY registers, or control arbitration acceleration.

The LPS and LKON/DS2 terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC and can be used to reset the PHY-LLC interface or to disable PCLK. The LKON/DS2 terminal sends a wake-up notification to the LLC or external circuitry and indicates an interrupt to the LLC when either LPS is inactive or the PHY register L bit is 0.

The TSB81BA3E normally controls the CTL0-CTL1 and D0-D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY.

There are four operations that may occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a service request to read or write a PHY register, to request the PHY to gain control of the serial-bus in order to transmit a packet, or to control arbitration acceleration.

1. The PHY can initiate a status transfer either autonomously or in response to a register read request from the LLC.
2. The PHY initiates a receive operation whenever a packet is received from the serial bus.
3. The PHY initiates a transmit operation after winning control of the serial bus following a bus request by the LLC.
4. The transmit operation is initiated when the PHY grants control of the interface to the LLC.

Table 10 and Table 11 show the encoding of the CTL0-CTL1 bus.

Table 10. CTL Encoding When PHY Has Control of the Bus

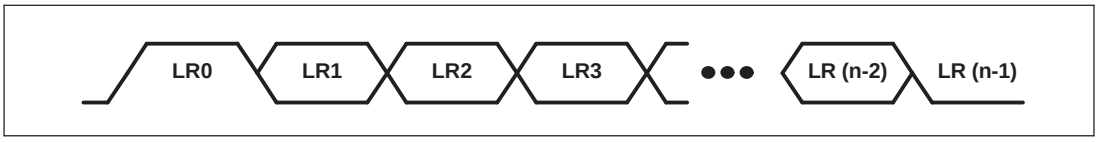
CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC.
1	0	Receive	An incoming packet is being sent from the PHY to the LLC.
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet.

Table 11. CTL Encoding When LLC Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed).
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission or indicating that another packet is to be transmitted (concatenated) without arbitrating.
1	0	Transmit	An outgoing packet is being sent from the LLC to the PHY.
1	1	Reserved	None

LLC Service Request

To request access to the bus, to read or write a PHY register, or to send a link notification to PHY, the LLC sends a serial bit stream on the LREQ terminal as shown in Figure 11.



Each cell represents one clock sample period, and n is the number of bits in the request stream.

Figure 11. LREQ Request Stream

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The length of the stream varies depending on the type of request as shown in Table 12.

Table 12. Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	7 or 8
Read register request	9
Write register request	17
Acceleration control request	6

Regardless of the type of request, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream. The second through fourth bits of the request stream indicate the type of the request. In the following descriptions, bit 0 is the most significant and is transmitted first in the request bit stream. The LREQ terminal is normally low.

Table 13 shows the encoding for the request type.

Table 13. Request Type Encoding

LR1-LR3	NAME	DESCRIPTION
000	ImmReq	Immediate bus request. On detection of idle, the PHY takes control of the bus immediately without arbitration.
001	IsoReq	Isochronous bus request. On detection of idle, the PHY arbitrates for the bus without waiting for a subaction gap.
010	PriReq	Priority bus request. The PHY arbitrates for the bus after a subaction gap, ignores the fair protocol.
011	FairReq	Fair bus request. The PHY arbitrates for the bus after a subaction gap, follows the fair protocol.
100	RdReg	PHY returns the specified register contents through a status transfer.
101	WrReg	Write to the specified register
110	AccelCtl	Enable or disable asynchronous arbitration acceleration
111	Reserved	Reserved

For a bus request, the length of the LREQ bit stream is 7 or 8 bits as shown in Table 14.

Table 14. Bus Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1-3	Request type	Indicates the type of bus request (See Table 13)
4-6	Request speed	Indicates the speed at which the PHY sends the data for this request (See Table 15 for the encoding of this field)
7	Stop bit	Indicates the end of the transfer (always 0). If bit 6 is 0, then this bit can be omitted.

Table 15 shows the 3-bit request format field used in bus requests.

Table 15. Bus Request Speed Encoding

LR4-LR6	DATA RATE
000	S100
010	S200
100	S400
All Others	Invalid

NOTE:

The TSB81BA3E accepts a bus request with an invalid speed code and processes the bus request normally. However, during packet transmission for such a request, the TSB81BA3E ignores any data presented by the LLC and transmits a null packet.

For a read register request, the length of the LREQ bit stream is 9 bits as shown in Table 16.

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Table 16. Read Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1-3	Request type	A 100 indicates this is a read register request.
4-7	Address	Identifies the address of the PHY register to be read
8	Stop bit	Indicates the end of the transfer (always 0)

For a write register request, the length of the LREQ bit stream is 17 bits as shown in Table 17.

Table 17. Write Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1-3	Request type	A 101 indicates this is a write register request.
4-7	Address	Identifies the address of the PHY register to be written to
8-15	Data	Gives the data that is to be written to the specified register address
16	Stop bit	Indicates the end of the transfer (always 0)

For an acceleration control request, the length of the LREQ data stream is 6 bits as shown in Table 18.

Table 18. Acceleration Control Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1-3	Request type	A 110 indicates this is an acceleration control request.
4	Control	Asynchronous period arbitration acceleration is enabled if 1 and disabled if 0
5	Stop bit	Indicates the end of the transfer (always 0)

For fair or priority access, the LLC sends the bus request (FairReq or PriReq) at least one clock after the PHY-LLC interface becomes idle. If the CTL terminals are asserted to the receive state (10b) by the PHY, then any pending fair or priority request is lost (cleared). Additionally, the PHY ignores any fair or priority requests if the receive state is asserted while the LLC is sending the request. The LLC can then reissue the request one clock after the next interface idle.

The cycle master node uses a priority bus request (PriReq) to send a cycle start message. After receiving or transmitting a cycle start message, the LLC can issue an isochronous bus request (IsoReq). The PHY clears an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the LLC must issue an immediate bus request (ImmReq) during the reception of the packet addressed to it. This is required to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the receive packet ends, the PHY immediately grants control of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC does not transmit an acknowledge, but instead cancels the transmit operation and immediately releases the interface; the LLC must not use this grant to send another type of packet. After the interface is released, the LLC can proceed with another request.

The LLC can make only one bus request at a time. Once the LLC issues any request for bus access (ImmReq, IsoReq, FairReq, or PriReq), it cannot issue another bus request until the PHY indicates that the bus request was lost (bus arbitration lost and another packet received), or won (bus arbitration won and the LLC granted control). The PHY ignores new bus requests while a previous bus request is pending. All bus requests are cleared on a bus reset.

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the LLC at the next opportunity through a status transfer. If a received packet interrupts the status transfer, then the PHY continues to attempt the transfer of the requested register until it is successful. A write or read register request can be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the LLC. A bus reset does not clear a pending read register request.

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The TSB81BA3E includes several arbitration acceleration enhancements, which allow the PHY to improve bus performance and throughput by reducing the number and length of interpacket gaps. These enhancements include autonomous (fly-by) isochronous packet concatenation, autonomous fair and priority packet concatenation onto acknowledge packets, and accelerated fair and priority request arbitration following acknowledge packets. The enhancements are enabled when the EAA bit in PHY register 5 is set.

The arbitration acceleration enhancements can interfere with the ability of the cycle master node to transmit the cycle start message under certain circumstances. The acceleration control request is therefore provided to allow the LLC temporarily to enable or disable the arbitration acceleration enhancements of the TSB81BA3E during the asynchronous period. The LLC typically disables the enhancements when its internal cycle counter rolls over, indicating that a cycle-start message is imminent, and then re-enables the enhancements when it receives a cycle-start message. The acceleration control request can be made at any time and is immediately serviced by the PHY. Additionally, a bus reset or isochronous bus request causes the enhancements to be re-enabled, if the EAA bit is set.

Status Transfer

A status transfer is initiated by the PHY when there is status information to be transferred to the LLC. The PHY waits until the interface is idle before starting the transfer. The transfer is initiated by the PHY asserting status (01b) on the CTL terminals, along with the first two bits of status information on the D[0:1] terminals. The PHY maintains CTL = Status for the duration of the status transfer. The PHY might prematurely end a status transfer by asserting something other than status on the CTL terminals. This occurs if a packet is received before the status transfer completes. The PHY continues to attempt to complete the transfer until all status information has been successfully transmitted. At least one idle cycle occurs between consecutive status transfers.

The PHY normally sends just the first 4 bits of status to the LLC. These bits are status flags that are needed by the LLC state machines. The PHY sends an entire 16-bit status packet to the LLC after a read register request, or when the PHY has pertinent information to send to the LLC or transaction layers. The only defined condition where the PHY automatically sends a register to the LLC is after self-ID, where the PHY sends the physical-ID register that contains the new node address. All status transfers are either 4 or 16 bits unless interrupted by a received packet. The status flags are considered to have been successfully transmitted to the LLC immediately on being sent, even if a received packet subsequently interrupts the status transfer. Register contents are considered to have been successfully transmitted only when all 8 bits of the register have been sent. A status transfer is retried after being interrupted only if any status flags remain to be sent, or if a register transfer has not yet completed.

Table 19 shows the definition of the bits in the status transfer, and Figure 12 shows the timing.

Table 19. Status Bits

BIT(s)	NAME	DESCRIPTION
0	Arbitration reset gap	Indicates that the PHY has detected that the bus has been idle for an arbitration reset gap time (as defined in the IEEE 1394a-2000 standard). This bit is used by the LLC in the busy/retry state machine.
1	Subaction gap	Indicates that the PHY has detected that the bus has been idle for a subaction gap time (as defined in the IEEE 1394a-2000 standard). This bit is used by the LLC to detect the completion of an isochronous cycle.
2	Bus reset	Indicates that the PHY has entered the bus reset state
3	Interrupt	Indicates that a PHY interrupt event has occurred. An interrupt event might be a configuration time-out, a cable-power voltage falling too low, a state time-out, or a port status change.
4-7	Address	This field holds the address of the PHY register whose contents are being transferred to the LLC.
8-15	Data	This field holds the register contents.

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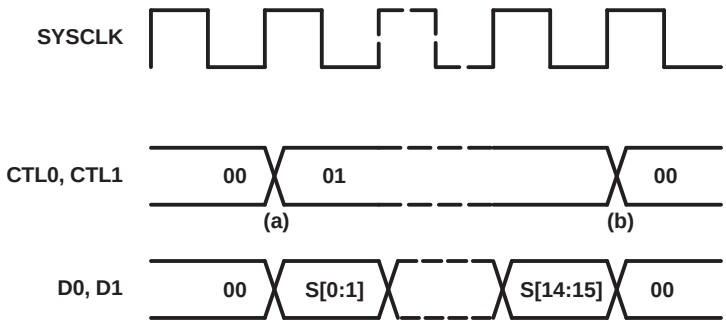


Figure 12. Status Transfer Timing

The sequence of events for a status transfer is as follows:

a. Status transfer initiated. The PHY indicates a status transfer by asserting status on the CTL lines along with the status data on the D0 and D1 lines (only 2 bits of status are transferred per cycle). Normally (unless interrupted by a receive operation), a status transfer is either 2 or 8 cycles long. A 2-cycle (4-bit) transfer occurs when only status information is to be sent. An 8-cycle (16-bit) transfer occurs when register data is to be sent in addition to any status information.

b. Status transfer terminated. The PHY normally terminates a status transfer by asserting idle on the CTL lines. The PHY can also interrupt a status transfer at any cycle by asserting receive on the CTL lines to begin a receive operation. The PHY asserts at least one idle cycle between consecutive status transfers.

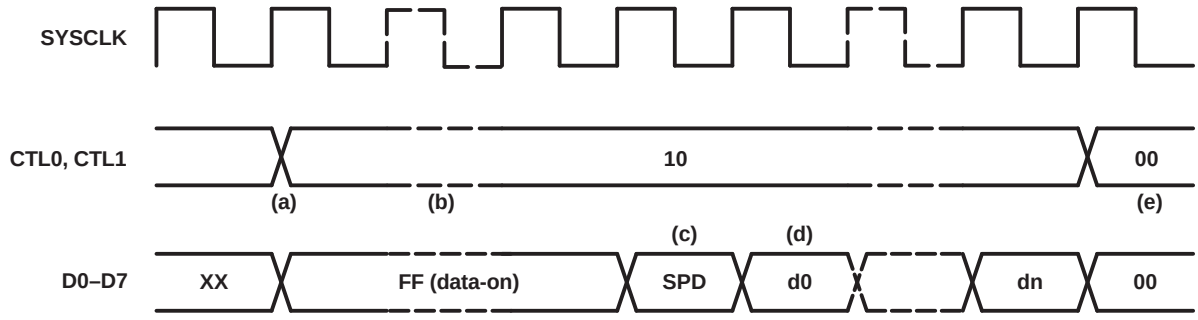
Receive

Whenever the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting receive on the CTL terminals and a logic 1 on each of the D bus terminals (data-on indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in Table 20) on the D terminals, followed by packet data. The PHY holds the CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting idle on the CTL terminals. All received packets are transferred to the LLC. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY, or whenever the LLC immediately releases the bus without transmitting any data. In this case, the PHY asserts receive on the CTL terminals with the data-on indication (all 1s) on the D bus terminals, followed by Idle on the CTL terminals, without any speed code or data being transferred. In all cases, in normal operation, the TSB81BA3E sends at least one data-on indication before sending the speed code or terminating the receive operation.

The TSB81BA3E also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the LLC. This packet is transferred to the LLC just as any other received self-ID packet.

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NOTE A: SPD = Speed code, see NO TAG. d0–dn = Packet data

A. SPD = Speed code, see Table 20 d0-dn = Packet data

Figure 13. Normal Packet Reception Timing

The sequence of events for a normal packet reception is as follows:

a. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.

b. Data-on indication. The PHY can assert the data-on indication code on the D lines for one or more cycles preceding the speed code.

c. Speed code. The PHY indicates the speed of the received packet by asserting a speed code on the D lines for one cycle immediately preceding packet data. The link decodes the speed code on the first receive cycle for which the D lines are not the data-on code. If the speed code is invalid or indicates a speed higher than that which the link is capable of handling, then the link must ignore the subsequent data.

d. Receive data. Following the data-on indication (if any) and the speed code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.

e. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

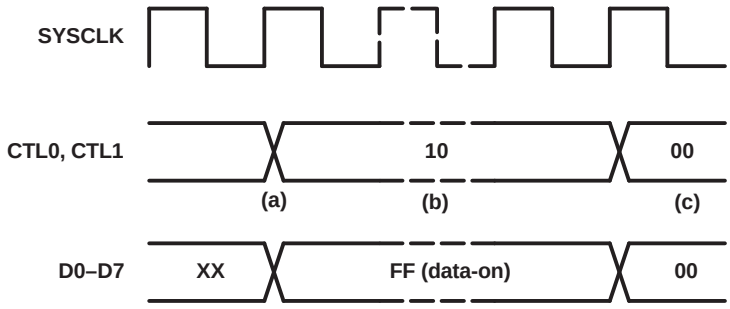


Figure 14. Null Packet Reception Timing

The sequence of events for a null packet reception is as follows:

a. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.

b. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.

c. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

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Table 20. Receive Speed Codes

D0-D7[1]	DATA RATE
00XX XXXX	S100
0100 XXXX	S200
0101 0000	S400
11YY YYYY	data-on indication

(1) X = Output as 0 by PHY, ignored by LLC.
Y = Output as 1 by PHY, ignored by LLC.

Transmit

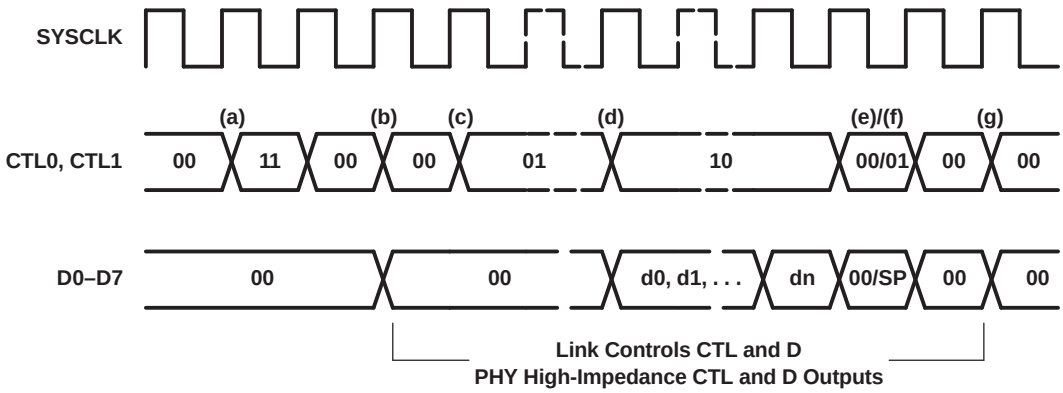
When the LLC issues a bus request through the LREQ terminal, the PHY arbitrates to gain control of the bus. If the PHY wins arbitration for the serial bus, then the PHY-LLC interface bus is granted to the LLC by asserting the grant state (11b) on the CTL terminals for one PCLK cycle, followed by idle for one clock cycle. The LLC then takes control of the bus by asserting either idle (00b), hold (01b) or transmit (10b) on the CTL terminals. Unless the LLC is immediately releasing the interface, the LLC can assert the idle state for at most one clock before it must assert either hold or transmit on the CTL terminals. The hold state is used by the LLC to retain control of the bus while it prepares data for transmission. The LLC can assert hold for zero or more clock cycles (that is, the LLC need not assert hold before transmit). The PHY asserts data-prefix on the serial bus during this time.

When the LLC is ready to send data, the LLC asserts transmit on the CTL terminals as well as sending the first bits of packet data on the D lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The LLC then asserts either hold or idle on the CTL terminals for one clock cycle and then asserts idle for one additional cycle before releasing the interface bus and putting the CTL and D terminals in a high-impedance state. The PHY then regains control of the interface bus.

The hold state asserted at the end-of-packet transmission indicates to the PHY that the LLC requests to send another packet (concatenated packet) without releasing the serial bus. The PHY responds to this concatenation request by waiting the required minimum packet separation time and then asserting grant as before. This function can be used to send a unified response after sending an acknowledge or to send consecutive isochronous packets during a single isochronous period. Unless multispeed concatenation is enabled, all packets transmitted during a single bus ownership must be of the same speed (because the speed of the packet is set before the first packet). If multispeed concatenation is enabled (when the EMSC bit of PHY register 5 is set), then the LLC must specify the speed code of the next concatenated packet on the D terminals when it asserts hold on the CTL terminals at the end of a packet. The encoding for this speed code is the same as the speed code that precedes received packet data as given in Table 20.

After sending the last packet for the current bus ownership, the LLC releases the bus by asserting idle on the CTL terminals for two clock cycles. The PHY begins asserting idle on the CTL terminals one clock after sampling idle from the link. Note that whenever the D and CTL terminals change direction between the PHY and the LLC, an extra clock period is allowed so that both sides of the interface can operate on registered versions of the interface signals.

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NOTE A: SPD = Speed code, see NO TAG. d0–dn = Packet data

A. SPD = Speed code, see Table 20 d0-dn = Packet data

Figure 15. Normal Packet Transmission Timing

The sequence of events for a normal packet transmission is as follows:

a. Transmit operation initiated. The PHY asserts grant on the CTL lines followed by idle to hand over control of the interface to the link so that the link can transmit a packet. The PHY releases control of the interface (that is, it places its CTL and D outputs in a high-impedance state) following the idle cycle.

b. Optional idle cycle. The link can assert at most one idle cycle preceding assertion of either hold or transmit. This idle cycle is optional; the link is not required to assert idle preceding either hold or transmit.

c. Optional hold cycles. The link can assert hold for up to 47 cycles preceding assertion of transmit. These hold cycle(s) are optional; the link is not required to assert hold preceding transmit.

d. Transmit data. When data is ready to be transmitted, the link asserts transmit on the CTL lines along with the data on the D lines.

e. Transmit operation terminated. The transmit operation is terminated by the link asserting hold or idle on the CTL lines. The link asserts hold to indicate that the PHY is to retain control of the serial bus in order to transmit a concatenated packet. The link asserts idle to indicate that packet transmission is complete and the PHY can release the serial bus. The link then asserts idle for one more cycle following this hold or idle cycle before releasing the interface and returning control to the PHY.

f. Concatenated packet speed code. If multispeed concatenation is enabled in the PHY, then the link asserts a speed code on the D lines when it asserts hold to terminate packet transmission. This speed code indicates the transmission speed for the concatenated packet that is to follow. The encoding for this concatenated packet speed code is the same as the encoding for the received packet speed code (see Table 20). The link cannot concatenate an S100 packet onto any higher-speed packet.

g. After regaining control of the interface, the PHY asserts at least one idle cycle before any subsequent status transfer, receive operation, or transmit operation.

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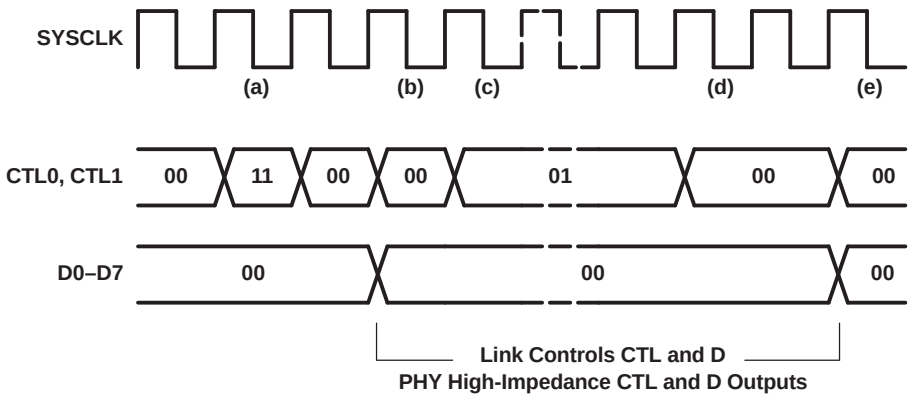


Figure 16. Cancelled/Null Packet Transmission

The sequence of events for a cancelled/null packet transmission is as follows:

a. Transmit operation initiated. PHY asserts grant on the CTL lines followed by idle to hand over control of the interface to the link.

b. Optional idle cycle. The link can assert at most one idle cycle preceding assertion of hold. This idle cycle is optional; the link is not required to assert idle preceding hold.

c. Optional hold cycles. The link can assert hold for up to 47 cycles preceding assertion of idle. These hold cycle(s) are optional; the link is not required to assert hold preceding idle.

d. Null transmit termination. The null transmit operation is terminated by the link asserting two cycles of idle on the CTL lines and then releasing the interface and returning control to the PHY. Note that the link can assert idle for a total of three consecutive cycles if it asserts the optional first idle cycle but does not assert hold. It is recommended that the link assert three cycles of idle to cancel a packet transmission if no hold cycles are asserted. This ensures that either the link or PHY controls the interface in all cycles.

e. After regaining control of the interface, the PHY asserts at least one idle cycle before any subsequent status transfer, receive operation, or transmit operation.

Interface Reset and Disable

The LLC controls the state of the PHY-LLC interface using the LPS signal. The interface can be placed into a reset state, a disabled state, or be made to initialize and then return to normal operation. When the interface is not operational (whether reset, disabled, or in the process of initialization), the PHY cancels any outstanding bus request or register read request, and ignores any requests made via the LREQ line. Additionally, any status information generated by the PHY is not queued and does not cause a status transfer on restoration of the interface to normal operation.

The LPS signal can be either a level signal or a pulsed signal, depending on whether the PHY-LLC interface is a direct connection or is made across an isolation barrier. When an isolation barrier exists between the PHY and LLC, the LPS signal must be pulsed. In a direct connection, the LPS signal can be either a pulsed or a level signal. Timing parameters for the LPS signal are given in Table 21.

Table 21. LPS Timing Parameters

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{LPSL}	LPS low time (when pulsed)(1)	0.09	2.6	µs
t_{LPSH}	LPS high time (when pulsed)(1)	0.021	2.6	µs
t_{LPS_DUTY}	PS duty cycle (when pulsed)(2)	20%	60%	
t_{LPS_RESET}	Time for PHY to recognize LPS deasserted and reset the interface	2.6	2.68	µs

(1) The specified t_{LPSL} and t_{LPSH} times are worst-case values appropriate for operation with the TSB81BA3E. These values are broader than those specified for the same parameters in the 1394a-2000 Supplement (that is, an implementation of LPS that meets the requirements of 1394a-2000 operates correctly with the TSB81BA3E).

(2) A pulsed LPS signal must have a duty cycle (ratio of t_{LPSH} to cycle period) in the specified range to ensure proper operation when using an isolation barrier on the LPS signal (for example, as shown in Figure 8).

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Table 21. LPS Timing Parameters (continued)

SYMBOL	DESCRIPTION		MIN	MAX	UNIT
$t_{LPS_DISABLE}$	Time for PHY to recognize LPS deasserted and disable the interface		26.03	26.11	µs
$t_{RESTORE}$	Time to permit optional isolation circuits to restore during an interface reset		15	23 (3)	µs
$t_{CLK_ACTIVATE}$	Time for PCLK to be activated from reassertion of LPS	PHY not in low-power state		60	ns
		PHY in low-power state	5.3	7.3	ms

(3) The maximum value for $t_{RESTORE}$ does not apply when the PHY-LLC interface is disabled, in which case an indefinite time can elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface, it is necessary that the LLC ensure that LPS is deasserted for less than $t_{LPS_DISABLE}$.

The LLC requests that the interface be reset by deasserting the LPS signal and terminating all bus and request activity. When the PHY observes that LPS has been deasserted for t_{LPS_RESET}, it resets the interface. When the interface is in the reset state, the PHY sets its CTL and D outputs in the logic 0 state and ignores any activity on the LREQ signal. Figure 17 shows the timing for interface reset.

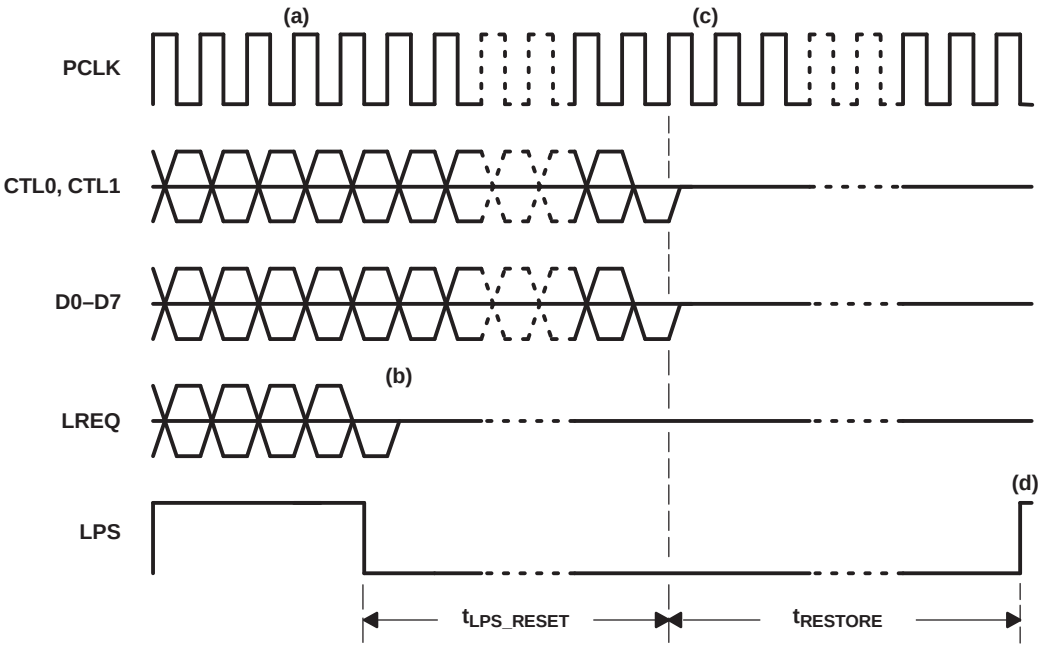


Figure 17. Interface Reset

The sequence of events for resetting the PHY-LLC interface is as follows:

a. Normal operation. Interface is operating normally, with LPS asserted, PCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line. In Figure 17, the LPS signal is shown as a nonpulsed level signal. However, it is permissible to use a pulsed signal for LPS in a direct connection between the PHY and LLC; a pulsed signal is required when using an isolation barrier.

b. LPS deasserted. The LLC deasserts the LPS signal and, within 1 µs, terminates any request or interface bus activity, places its CTL and D outputs into the high-impedance state, and drives its LREQ output low.

c. Interface reset. After t_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.

d. Interface restored. After the minimum $t_{RESTORE}$ time, the LLC can again assert LPS active. When LPS is asserted, the interface is initialized as described in the following paragraph.

If the LLC continues to keep the LPS signal deasserted, it then requests that the interface be disabled. The PHY disables the interface when it observes that LPS has been deasserted for $t_{LPS_DISABLE}$. When the interface is disabled, the PHY sets its CTL and D outputs as previously stated for interface reset, but also stops PCLK activity. The interface is also placed into the disabled condition on a hardware reset of the PHY. Figure 18 shows the timing for the interface disable.

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When the interface is disabled, the PHY enters a low-power state if none of its ports are active.

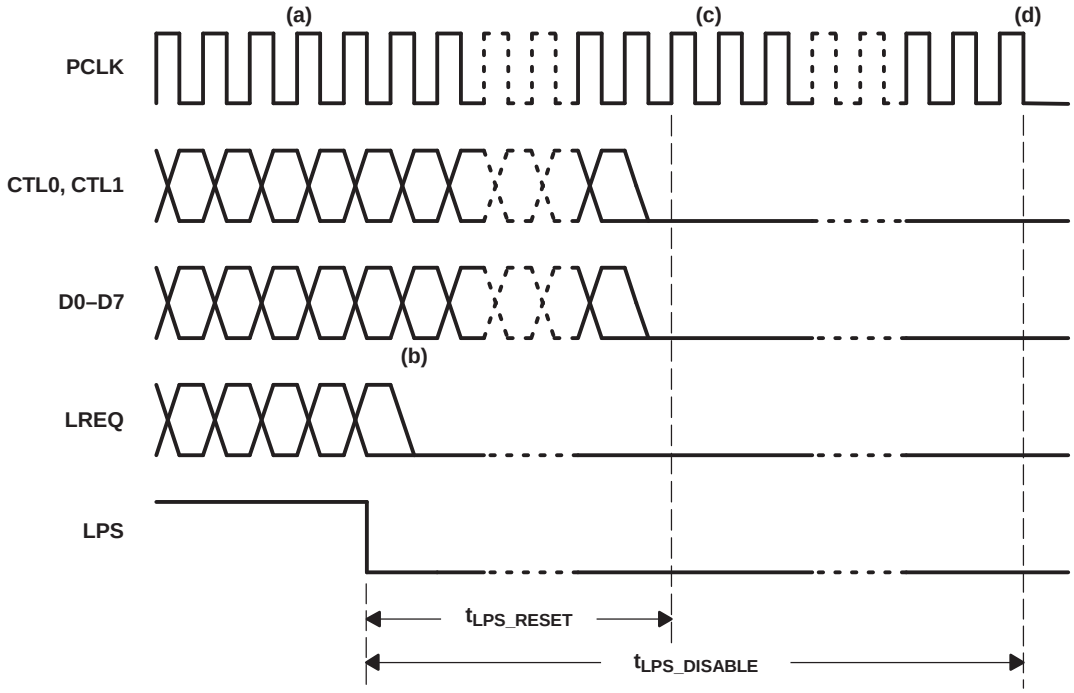


Figure 18. Interface Disable

The sequence of events for disabling the PHY-LLC is as follows:

a. Normal operation. Interface is operating normally, with LPS active, PCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.

b. LPS deasserted. The LLC deasserts the LPS signal and, within 1 s, terminates any request or interface bus activity, places its CTL and D outputs into a high-impedance state, and drives its LREQ output low.

c. Interface reset. After t_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.

d. Interface disabled. If the LPS signal remains inactive for $t_{LPS_DISABLE}$ time, then the PHY terminates PCLK activity by driving the PCLK output low. The PHY-LLC interface is now in the disabled state.

After the interface has been reset, or reset and then disabled, the interface is initialized and restored to normal operation when LPS is reasserted by the LLC. Figure 19 shows the timing for interface initialization.

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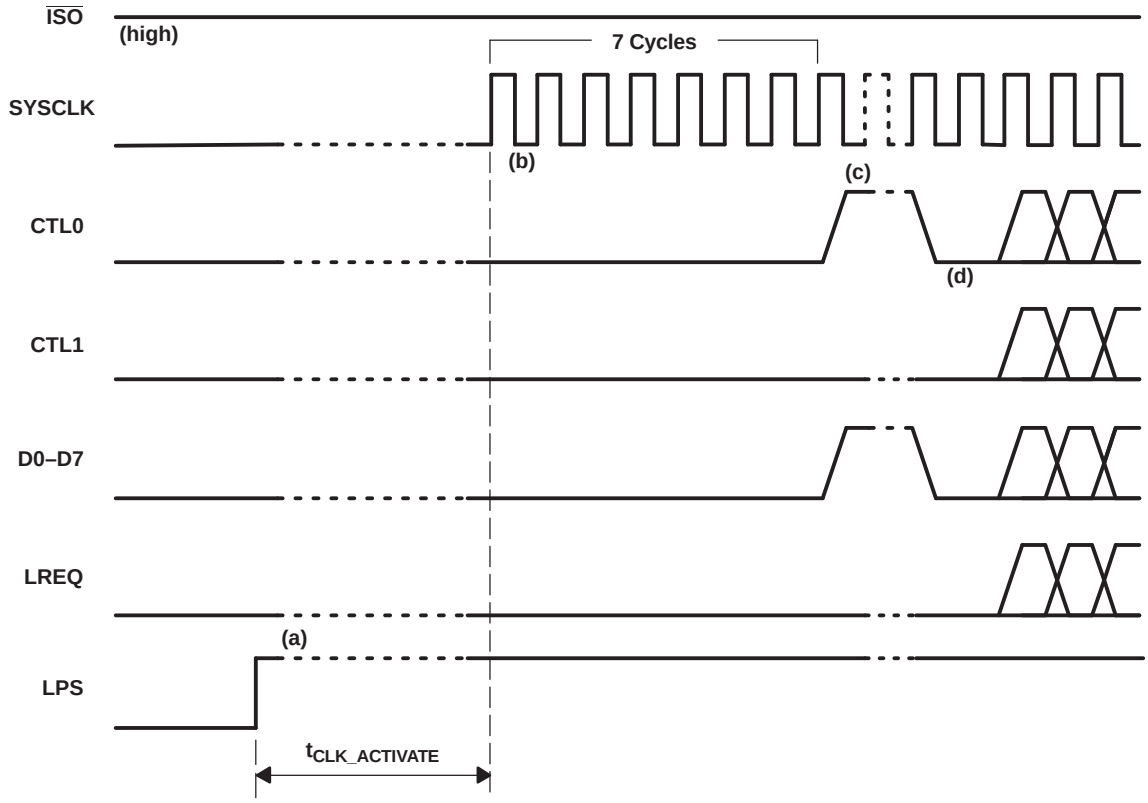


Figure 19. Interface Initialization

The sequence of events for initialization of the PHY-LLC is as follows:

a. LPS reasserted. After the interface has been in the reset or disabled state for at least the minimum $t_{RESTORE}$ time, the LLC causes the interface to be initialized and restored to normal operation by reasserting the LPS signal. (In Figure 19, the interface is shown in the disabled state with PCLK inactive. However, the interface initialization sequence described here is also executed if the interface is merely reset but not yet disabled.)

b. PCLK activated. If the interface is disabled, then the PHY reactivates its PCLK output when it detects that LPS has been reasserted. If the PHY has entered a low-power state, then it takes between 5.3 ms and 7.3 ms for PCLK to be restored; if the PHY is not in a low-power state, then the PCLK is restored within 60 ns. The PCLK output is a 50% duty cycle square wave with a frequency of 49.152 MHz ±100 ppm (period of 20.345 ns). During the first 7 cycles of PCLK, the PHY continues to drive the CTL and D terminals low. The LLC is also required to drive its CTL and D outputs low for one of the first 6 cycles of PCLK but otherwise to place its CTL and D outputs in the high-impedance state. The LLC continues to drive its LREQ output low during this time.

c. Receive indicated. On the eighth PCLK cycle following reassertion of LPS, the PHY asserts the receive state on the CTL lines and the data-on indication (all 1s) on the D lines for one or more cycles.

d. Initialization complete. The PHY asserts the idle state on the CTL lines and logic 0 on the D lines. This indicates that the PHY-LLC interface initialization is complete and normal operation can commence. The PHY now accepts requests from the LLC via the LREQ line.

The TSB81BA3E is designed to operate with an LLC such as the Texas Instruments TSB82AA2 when the BMODE terminal is tied high. Details of operation for the Texas Instruments LLC devices are found in the respective LLC data sheets. The following paragraphs describe the operation of the PHY-LLC interface. This interface is formally specified in the IEEE 1394b-2002 standard.

The interface to the LLC consists of the PCLK, LCLK_PMC, CTL0-CTL1, D0-D7, LREQ, PINT, LPS, and LKON/DS2 terminals on the TSB81BA3E, as shown in Figure 20.

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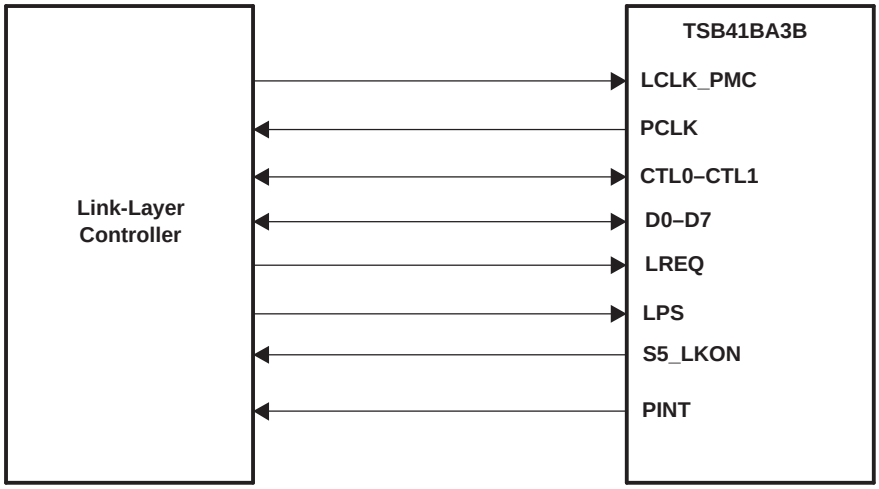


Figure 20. PHY-LLC Interface

The LCLK terminal provides a clock signal to the PHY. The LLC derives this clock from the PCLK signal and is phase-locked to the PCLK signal. All LLC to PHY transfers are synchronous to LCLK.

The PCLK terminal provides a 98.304-MHz interface system clock. All control, data, and PHY interrupt signals are synchronized to the rising edge of PCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the TSB81BA3E and LLC.

The D0−D7 terminals form a bidirectional data bus, which transfers status information, control information, or packet data between the devices. The TSB81BA3E supports S400B and S800 data transfers over the D0−D7 data bus. In S400B and S800 operation all Dn terminals are used.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY to request access to the serial-bus for packet transmission, read or write PHY registers, or control arbitration acceleration. All data on LREQ is synchronous to LCLK.

The LPS and LKON/DS2 terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC, and may be used to reset the PHY-LLC interface or to disable PCLK. The LKON/DS2 terminal sends a wake-up notification to the LLC and indicates an interrupt to the LLC when either LPS is inactive or the PHY register L bit is 0.

The PINT terminal is used by the PHY for the serial transfer of status, interrupt, and other information to the LLC.

The TSB81BA3E normally controls the CTL0-CTL1 and D0-D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY.

There are four operations that may occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a service request to read or write a PHY register or to request the PHY to gain control of the serial-bus in order to transmit a packet.

The PHY may initiate a status transfer either autonomously or in response to a register read request from the LLC.

The PHY initiates a receive operation when a packet is received from the serial-bus.

The PHY initiates a transmit operation after winning control of the serial-bus following a bus-request by the LLC. The transmit operation is initiated when the PHY grants control of the interface to the LLC.

Table 22 and Table 23 show the encoding of the CTL0-CTL1 bus.

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Table 22. CTL Encoding When PHY Has Control of the Bus

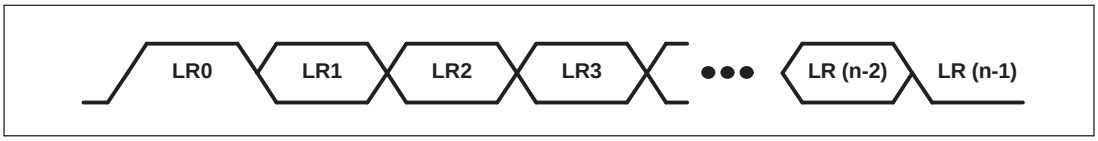
CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC.
1	0	Receive	An incoming packet is being sent from the PHY to the LLC.
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet.

Table 23. CTL Encoding When LLC Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed).
0	1	Transmit	An outgoing packet is being sent from the LLC to the PHY.
1	0	Reserved	Reserved
1	1	Holation	The LLC is holding the bus while data is being prepared for transmission, or the LLC is sending a request to arbitrate for access to the bus, or the LLC is identifying the end of a subaction gap to the PHY.

LLC Service Request

To request access to the bus, to read or write a PHY register, or to send a link notification to PHY, the LLC sends a serial bit stream on the LREQ terminal as shown in Figure 21.



Each cell represents one clock sample period, and n is the number of bits in the request stream.

Figure 21. LREQ Request Stream

The length of the stream varies depending on the type of request as shown in Table 24.

Table 24. Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	11
Read register request	10
Write register request	18
Link notification request	6
PHY-link interface reset request	6

Regardless of the type of request, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream. The second through fifth bits of the request stream indicate the type of the request. In the descriptions in Table 25, bit LR1 is the most significant and is transmitted first in the request bit stream. The LREQ terminal is normally low.

Table 25 shows the encoding for the request type.

Table 25. Request Type Encoding

LR1-LR4	NAME	DESCRIPTION
0000	Reserved	Reserved
0001	Immed_Req	Immediate request. On detection of idle, the PHY arbitrates for the bus.
0010	Next_Even	Next even request. The PHY arbitrates for the bus to send an asynchronous packet in the even fairness interval phase.
0011	Next_Odd	Next odd request. The PHY arbitrates for the bus to send an asynchronous packet in the odd fairness interval phase.

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Table 25. Request Type Encoding (continued)

LR1-LR4	NAME	DESCRIPTION
0100	Current	Current request. The PHY arbitrates for the bus to send an asynchronous packet in the current fairness interval.
0101	Reserved	Reserved
0110	Isoch_Req_Even	Isochronous even request. The PHY arbitrates for the bus to send an isochronous packet in the even isochronous period.
0111	Isoch_Req_Odd	Isochronous odd request. The PHY arbitrates for the bus to send an isochronous packet in the odd isochronous period.
1000	Cyc_Start_Req	Cycle start request. The PHY arbitrates for the bus to send a cycle start packet.
1001	Reserved	Reserved
1010	Reg_Read	Register read request. The PHY returns the specified register contents through a status transfer.
1011	Reg_Write	Register write request. Write to the specified register in the PHY.
1100	Isoch_Phase_Even	Isochronous phase even notification. The link reports to the PHY that: 1) A cycle start packet has been received. 2) The link has set the isochronous phase to even.
1101	Isoch_Phase_Odd	Isochronous phase odd notification. The link reports to the PHY that: 1) A cycle start packet has been received. 2) The link has set the isochronous phase to odd.
1110	Cycle_Start_Due	Cycle start due notification. The link reports to the PHY that a cycle start packet is due for reception.
1111	Reserved	Reserved

For a bus request, the length of the LREQ bit stream is 11 bits as shown in Table 26.

Table 26. Bus Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	Indicates the type of bus request (See Table 25)
5	Request format	Indicates the packet format to be used for packet transmission (See Table 27)
6–9	Request speed	Indicates the speed at which the link sends the data to the PHY (See Table 28 for the encoding of this field)
10	Stop bit	Indicates the end of the transfer (always 0). If bit 6 is 0, then this bit can be omitted.

Table 27 shows the 1-bit request format field used in bus requests.

Table 27. Bus Request Format Encoding

LR5	DATA RATE
0	Link does not request either Beta or legacy packet format for bus transmission
1	Link requests Beta packet format for bus transmission

Table 28 shows the 4-bit request speed field used in bus requests.

Table 28. TBus Request Speed Encoding

LR6-LR9	DATA RATE
0000	S100
0001	Reserved
0010	S200
0011	Reserved
0100	S400
0101	Reserved
0110	S800
All Others	Invalid

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NOTE:

The TSB81BA3E accepts a bus request with an invalid speed code and processes the bus request normally. However, during packet transmission for such a request, the TSB81BA3E ignores any data presented by the LLC and transmits a null packet.

For a read register request, the length of the LREQ bit stream is 10 bits as shown in Table 29.

Table 29. Read Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	A 1010 indicates this is a read register request.
5–8	Address	Identifies the address of the PHY register to be read
9	Stop bit	Indicates the end of the transfer (always 0)

For a write register request, the length of the LREQ bit stream is 18 bits as shown in Table 30.

Table 30. Write Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	A 1010 indicates this is a write register request.
5–8	Address	Identifies the address of the PHY register to be writer
9–16	Data	Gives the data that is to be written to the specified register address
17	Stop bit	Indicates the end of the transfer (always 0)

For a link notification request, the length of the LREQ bit stream is 6 bits as shown in Table 31.

Table 31. Link Notification Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	A 1100, 1101, or 1110 indicates this is a link notification request.
5	Stop bit	Indicates the end of the transfer (always 0)

For fair or priority access, the LLC sends a bus request at least one clock after the PHY-LLC interface becomes idle. The PHY queues all bus requests and can queue one request of each type. If the LLC issues a different request of the same type, then the new request overwrites any nonserviced request of that type. On the receipt (CTL terminals are asserted to the receive state, 10b) of a packet, queued requests are not cleared by the PHY.

The cycle master node uses a cycle start request (Cyc_Start_Req) to send a cycle start message. After receiving or transmitting a cycle start message, the LLC can issue an isochronous bus request (IsoReq). The PHY clears an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the LLC must issue an immediate bus request (Immed_Req) during the reception of the packet addressed to it. This is required to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the received packet ends, the PHY immediately grants control of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC does not transmit an acknowledge, but instead cancels the transmit operation and releases the interface immediately; the LLC must not use this grant to send another type of packet. After the interface is released the LLC can proceed with another request.

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the LLC at the next opportunity through a PHY status transfer. A write or read register request can be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the LLC. A bus reset does not clear a pending read register request.

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Status Transfer

A status transfer is initiated by the PHY when status information is to be transferred to the LLC. Two types of status transfers can occur: bus status transfer and PHY status transfer. Bus status transfers send the following status information: bus reset indications, subaction and arbitration reset gap indications, cycle start indications, and PHY interface reset indications. PHY status transfers send the following information: PHY interrupt indications, unsolicited and solicited PHY register data, bus initialization indications, and PHY-link interface error indications. The PHY uses a different mechanism to send the bus status transfer and the PHY status transfer.

Bus status transfers use the CTL0-CTL1 and D0-D7 terminals to transfer status information. Bus status transfers can occur during idle periods on the PHY-link interface or during packet reception. When the status transfer occurs, a single PCLK cycle of status information is sent to the LLC. The information is sent such that each individual Dn terminal conveys a different bus status transfer event. During any bus status transfer, only one status bit is set. If the PHY-link interface is inactive, then the status information is not sent. When a bus reset on the serial bus occurs, the PHY sends a bus reset indication (via the CTLn and Dn terminals), cancels all packet transfer requests, sets asynchronous and isochronous phases to even, forwards self-ID packets to the link, and sends an unsolicited PHY register 0 status transfer (via the PINT terminal) to the LLC. In the case of a PHY interface reset operation, the PHY-link interface is reset on the following PCLK cycle.

Table 32 shows the definition of the bits during the bus status transfer and Figure 22 shows the timing.

Table 32. Status Bits

STATUS BIT	DESCRIPTION
D0	Bus reset
D1	Arbitration reset gap – odd
D2	Arbitration reset gap – even
D3	Cycle start – odd
D4	Cycle start – even
D5	Subaction gap
D6	PHY interface reset
D7	Reserved

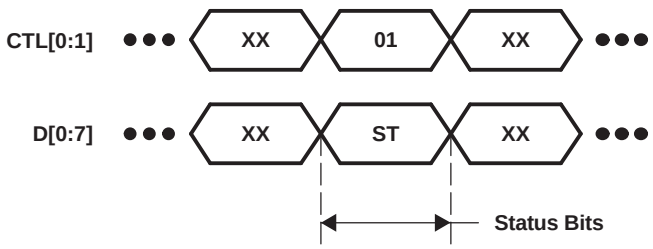
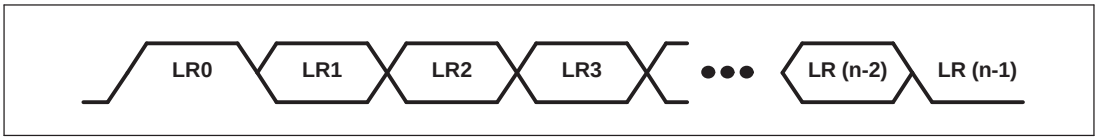


Figure 22. Bus Status Transfer Timing

PHY status transfers use the PINT terminal to send status information serially to the LLC as shown in Figure 23. PHY status transfers (see Table 33) can occur at any time during normal operation. The PHY uses the PHY_INTERRUPT PHY status transfer when required to interrupt the LLC due to a configuration time-out, a cable-power failure, a port interrupt, or an arbitration time-out. When transferring PHY register contents, the PHY uses either the solicited or the unsolicited register read status transfer. The unsolicited register 0 contents are passed to the LLC only during initialization of the serial bus. After any PHY-link interface initialization, the PHY sends a PHY status transfer indicating whether or not a bus reset occurred during the inactive period of the PHY-link interface. If the PHY receives an illegal request from the LLC, then the PHY issues an INTERFACE_ERROR PHY status transfer.

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Each cell represents one clock sample period, and n is the number of bits in the request stream.

Figure 23. PINT (PHY Interrupt) Stream

Table 33. PHY Status Transfer Encoding

PI[1:3]	NAME	DESCRIPTION	NUMBER OF BITS
000	NOP	No status indication	5
001	PHY_INTERRUPT	Interrupt indication: configuration time-out, cable-power failure, port event interrupt, or arbitration state machine time-out.	5
010	PHY_REGISTER_SOL	Solicited PHY register read	17
011	PHY_REGISTER_UNSOL	Unsolicited PHY register read	17
100	PH_RESTORE_NO_RESET	PHY-link interface initialized; no bus resets occurred.	5
101	PH_RESTORE_RESET	PHY-link interface initialized; a bus reset occurred.	5
110	INTERFACE_ERROR	PHY received illegal request.	5
111	Reserved	Reserved	Reserved

Most PHY status transfers are 5 bits long. The transfer consists of a start bit (always 1), followed by a request type (see Table 33), and lastly followed by a stop bit (always 0). The only exception is when the transfer of a register contents occurs. Solicited and unsolicited PHY register read transfers are 17 bits long and include the additional information of the register address and the data contents of the register (see Table 34).

Table 34. Register Read (Solicited and Unsolicited) PHY Status Transfer Encoding

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	A 010 or a 011 indicates a solicited or unsolicited register contents transfer.
4–7	Address	Identifies the address of the PHY register whose contents are being transferred
8–15	Data	The contents of the register specified in bits 4 through 7
16	Stop bit	Indicates the end of the transfer (always 0)

Receive

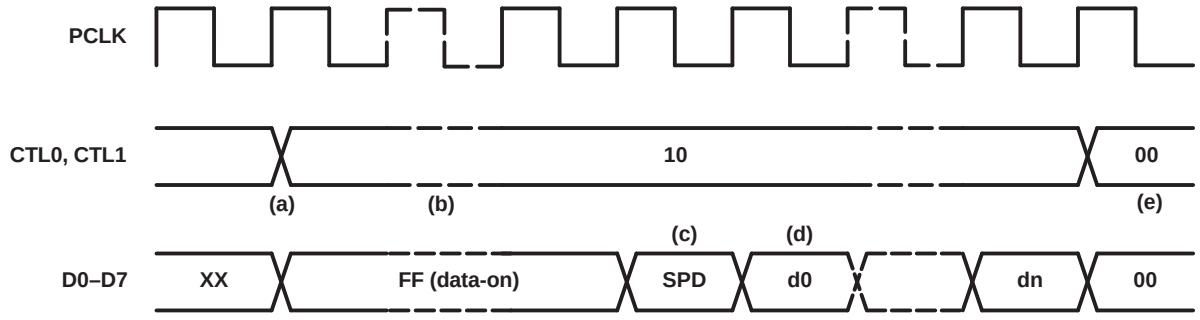
When the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting receive on the CTL terminals and a logic 1 on each of the D terminals (data-on indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in Table 35) on the D terminals, followed by packet data. The PHY holds the CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting idle on the CTL terminals. All received packets are transferred to the LLC. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

The PHY can optionally send status information to the LLC at anytime during the data-on indication. Only bus status transfer information can be sent during a data-on indication. The PHY holds the CTL terminals in the status state for 1 PCLK cycle and modifies the D terminals to the correct status state. Note that the status transfer during the data-on indication does not need to be preceded or followed by a data-on indication.

It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY, or whenever the LLC immediately releases the bus without transmitting any data. In this case, the PHY asserts receive on the CTL terminals with the data-on indication (all 1s) on the D terminals, followed by idle on the CTL terminals, without any speed code or data being transferred. In all cases, in normal operation, the TSB81BA3E sends at least one data-on indication before sending the speed code or terminating the receive operation.

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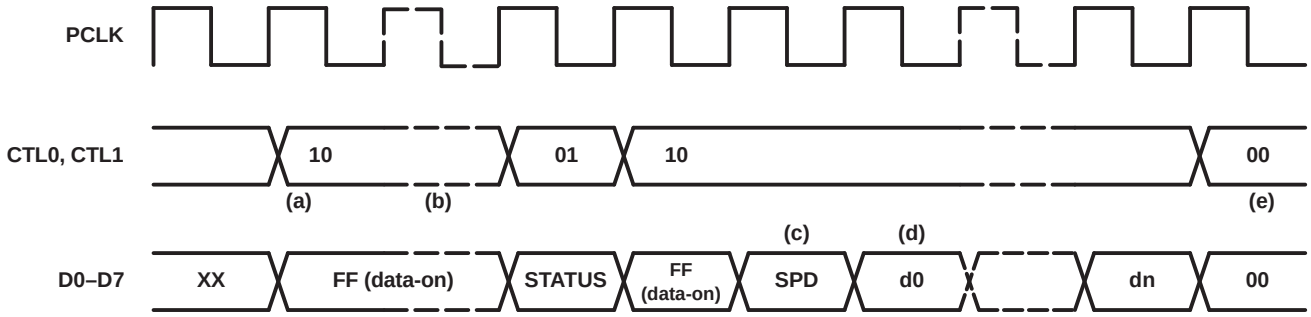
The TSB81BA3E also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the LLC. This packet it transferred to the LLC just as any other received self-ID packet.



NOTE A: SPD = speed code, see NO TAG. d0–dn = packet data

A. SPD = speed code, see Table 35. d0-dn = packet data

Figure 24. Normal Packet Reception Timing



NOTE A: SPD = speed code, see NO TAG. d0–dn = packet data. STATUS = status bits, see NO TAG.

A. SPD = speed code, see Table 35. d0-dn = packet data. STATUS = status bits, see Table 32.

Figure 25. Normal Packet Reception Timing With Optional Bus Status Transfer

The sequence of events for a normal packet reception is as follows:

a. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.

b. Data-on indication. The PHY can assert the data-on indication code on the D lines for one or more cycles preceding the speed code. The PHY can optionally send a bus status transfer during the data-on indication for one PCLK cycle. During this cycle, the PHY asserts status (01b) on the CTL lines while sending status information on the D lines.

c. Speed code. The PHY indicates the speed of the received packet by asserting a speed code on the D lines for one cycle immediately preceding packet data. The link decodes the speed code on the first receive cycle for which the D lines are not the data-on code. If the speed code is invalid or indicates a speed higher than that which the link is capable of handling, then the link must ignore the subsequent data.

d. Receive data. Following the data-on indication (if any) and the speed code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.

e. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

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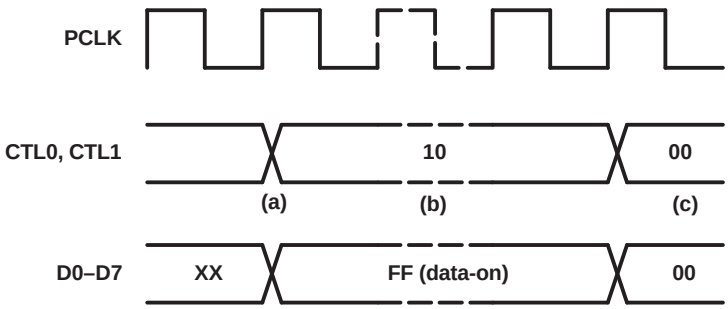


Figure 26. Null Packet Reception Timing

The sequence of events for a null packet reception is as follows:

a. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.

b. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.

c. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

Table 35. Receive Speed Codes and Format

D0-D7(1)	DATA RATE AND FORMAT
0000 0000	S100 legacy
0000 0001	S100 Beta
0000 0100	S200 legacy
0000 0101	S200 Beta
0000 1000	S400 legacy
0000 1001	S400 Beta
0000 1101	S800 Beta
1111 1111	Data-on indication
All others	Reserved

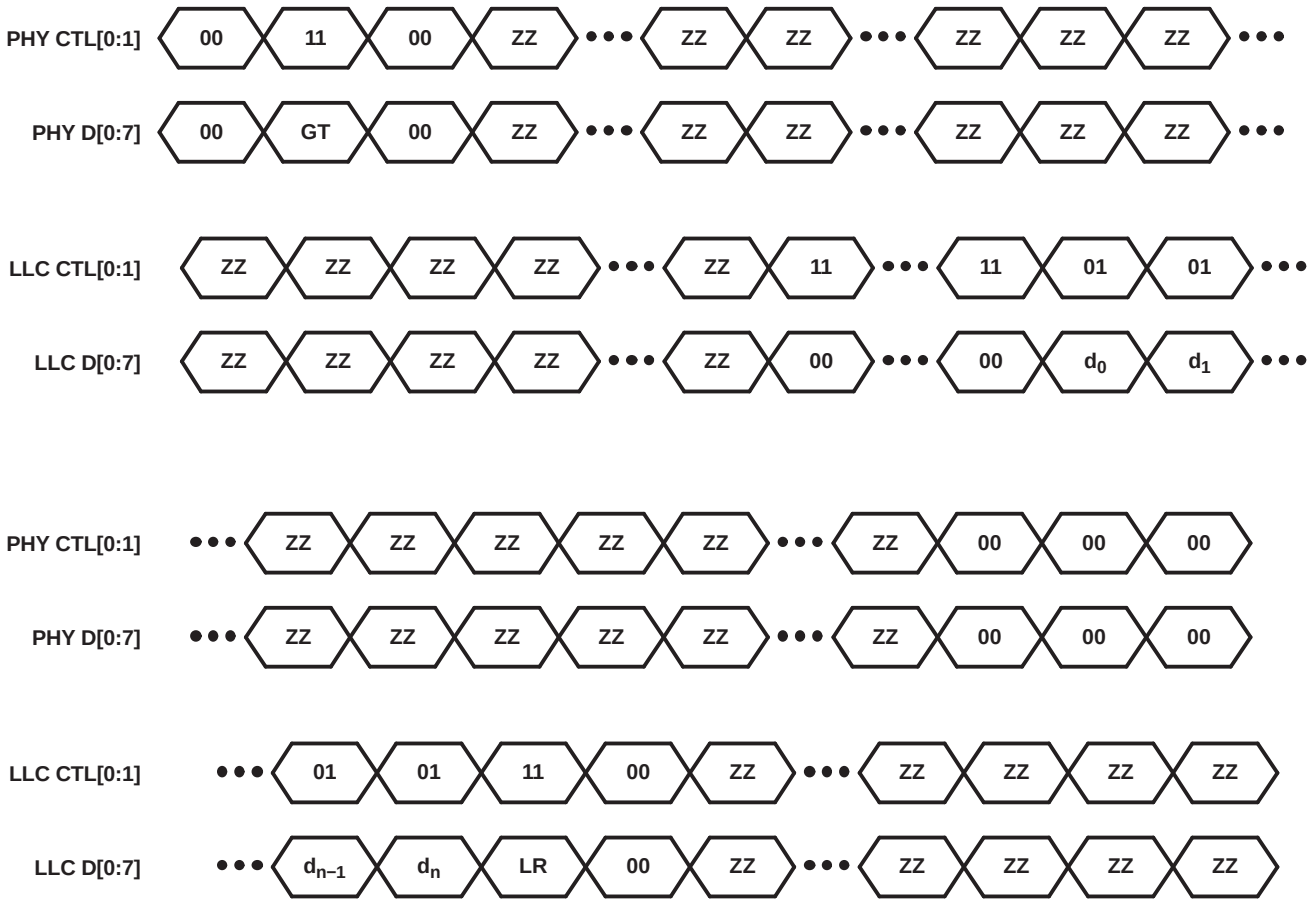
(1) Y = Output as 1 by PHY, ignored by LLC.
X = Output as 0 by PHY, ignored by LLC

Transmit

When the LLC issues a bus request through the LREQ terminal, the PHY arbitrates to gain control of the bus. If the PHY wins arbitration for the serial bus, then the PHY-LLC interface bus is granted to the LLC by asserting the grant state (11b) on the CTL terminals and the grant type on the D terminals for one PCLK cycle, followed by idle for one clock cycle. The LLC then takes control of the bus by asserting either idle (00b), hold (11b), or transmit (01b) on the CTL terminals. If the PHY does not detect a hold or transmit state within eight PCLK cycles, then the PHY takes control of the PHY-link interface. The hold state is used by the LLC to retain control of the bus while it prepares data for transmission. The LLC can assert hold for zero or more clock cycles (that is, the LLC need not assert hold before transmit). During the hold state, the LLC is expected to drive the D lines to 0. The PHY asserts data-prefix on the serial bus during this time.

When the LLC is ready to send data, the LLC asserts transmit on the CTL terminals as well as sending the first bits of packet data on the D lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The LLC then asserts either hold or idle on the CTL terminals for one clock cycle. If the hold is asserted, then the hold is immediately followed by one clock cycle of idle. The link then releases the PHY-link interface by putting the CTL and D terminals in a high-impedance state. The PHY then regains control of the PHY-link interface.

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GT = grant type LR = link request type d0−dn = packet data

Figure 27. Transmit Packet Timing With Optional Link Request

The hold state asserted at the end of packet transmission allows the LLC to make an additional link request for packet transmission and/or to notify the PHY that the packet marks the end of a subaction. The link requests allowed after packet transmission are listed in Table 36 (note that the link request types allowed during this period are a subset of all of the allowed types of link requests—see Table 25). The associated speed codes and packet format are listed in Table 36 and Table 37, respectively. If the LLC requests to send an additional packet, then the PHY does not necessarily have to grant the request. If the LLC is notifying the PHY of the end of a subaction, then the LLC sets D4 during the hold state at the end of packet transmission.

Table 36. Link Request Type Encoding During Packet Transmission

D1D3	REQUEST TYPE
000	No request
001	Isoch_Req_Odd
010	Isoch_Req_Even
011	Current
100	Next_Even
101	Next_Odd
110	Cyc_Start_Req
111	Reserved

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Table 37. ink Request Speed Code Encoding During Packet Transmission

D5D6	DATA RATE
00	S100
01	S200
10	S400
11	S800

Table 38. Link Request Format Encoding During Packet Transmission

D0	FORMAT
0	Link does not request either Beta or legacy packet format for bus transmission.
1	Link requests Beta packet format for bus transmission.

Table 39. Subaction End Notification Encoding During Packet Transmission

D4	DESCRIPTION
0	Transmitted packet does not represent end of a subaction.
1	Transmitted packet marks the end of a subaction.

The PHY indicates to the link during the GRANT cycle which type of grant is being issued. This indication includes the grant type as well as the grant speed. The link uses the bus grant for transmitting the granted packet type. The link transmits a granted packet type only if its request type exactly matches the granted speed and the granted format.

Table 40. Format Type During Grant Cycle

D0 VALUE DURING GRANT CYCLE	FORMAT
0	Unspecified
1	Beta format

Table 41. Grant Type Values During Grant Cycle

[D1-D3] VALUE DURING GRANT CYCLE	REQUEST TYPE
000	Reserved
001	Reserved
010	Isochronous grant
011	Reserved
100	Reserved
101	Asynchronous grant
110	Cycle start grant
111	Immediate grant

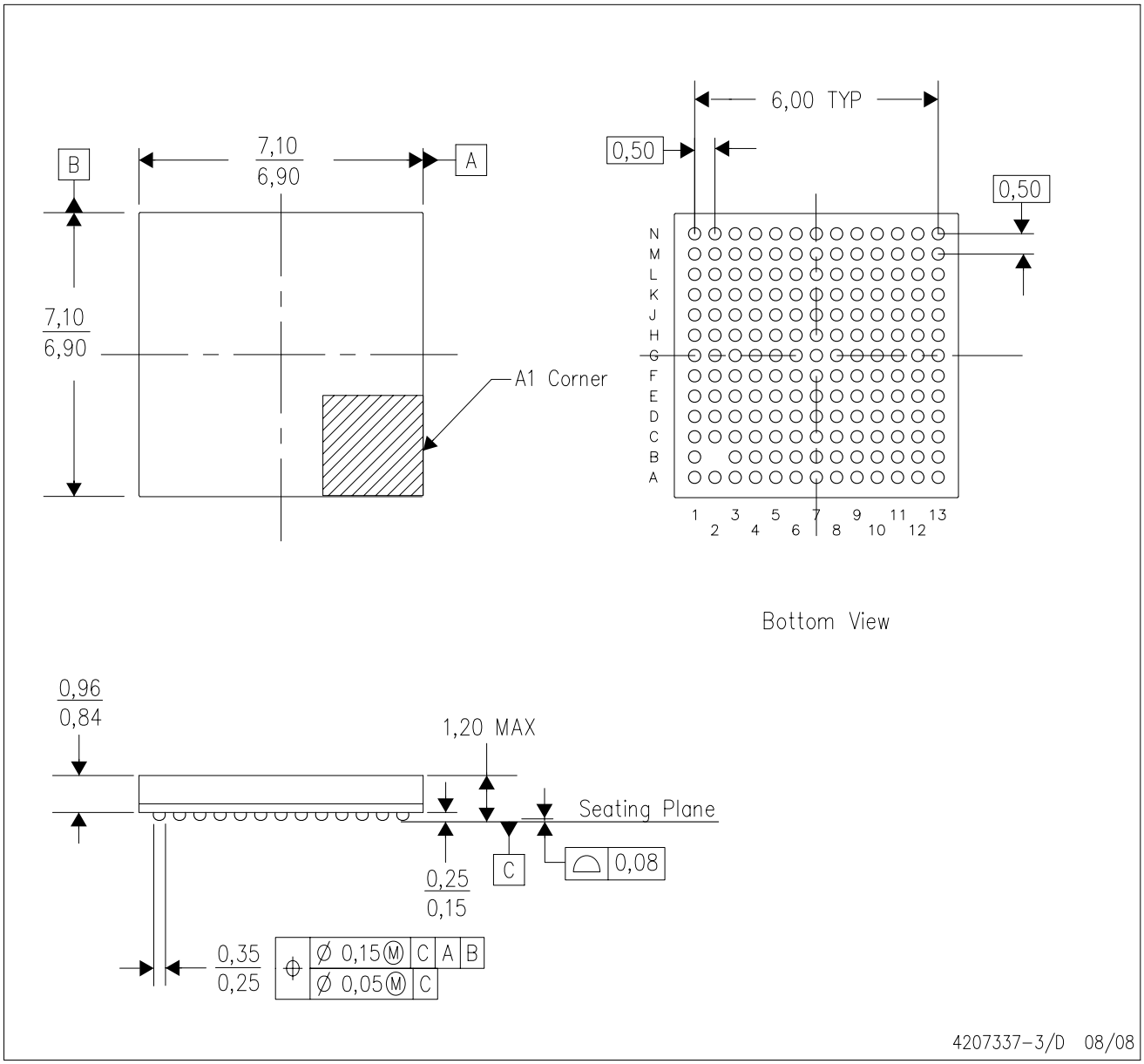
Table 42. Speed Type Values During Grant Cycle

[D5-D6] VALUE DURING GRANT CYCLE	SPEED TYPE
00	S100
01	S200
10	S400
11	S800

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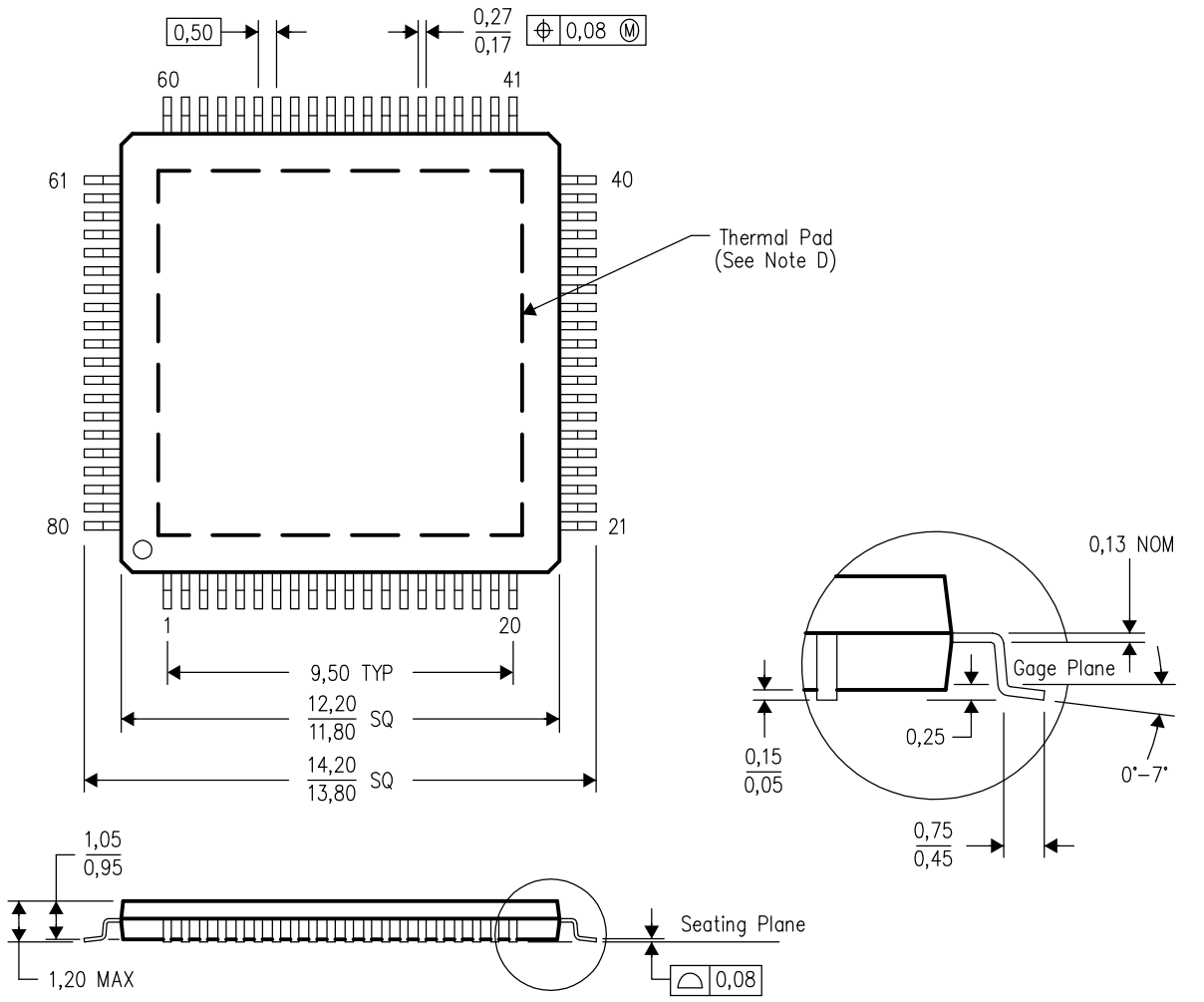
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ZAJ (S–PBGA–N168) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

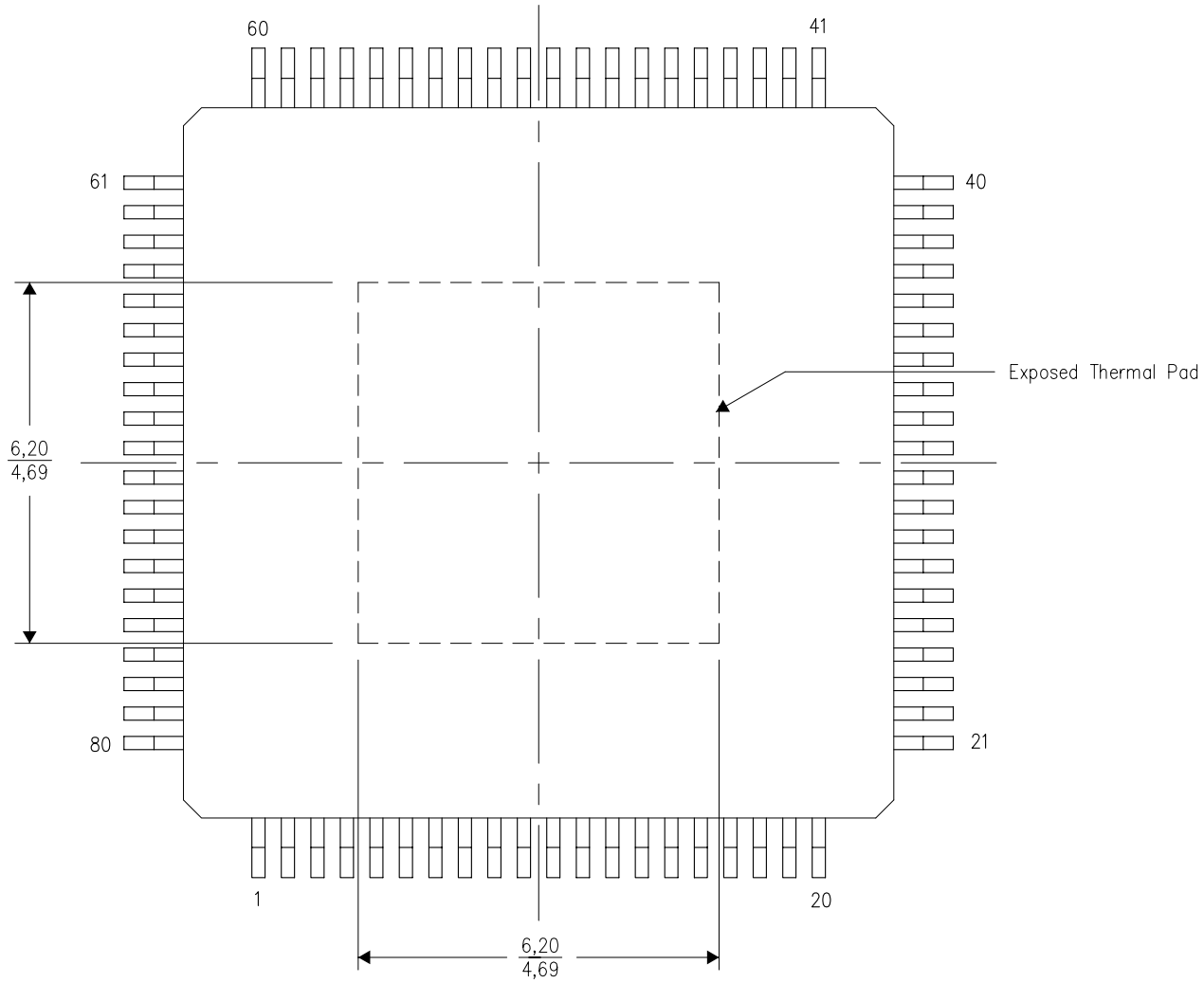
PFP (S–PQFP–G80)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

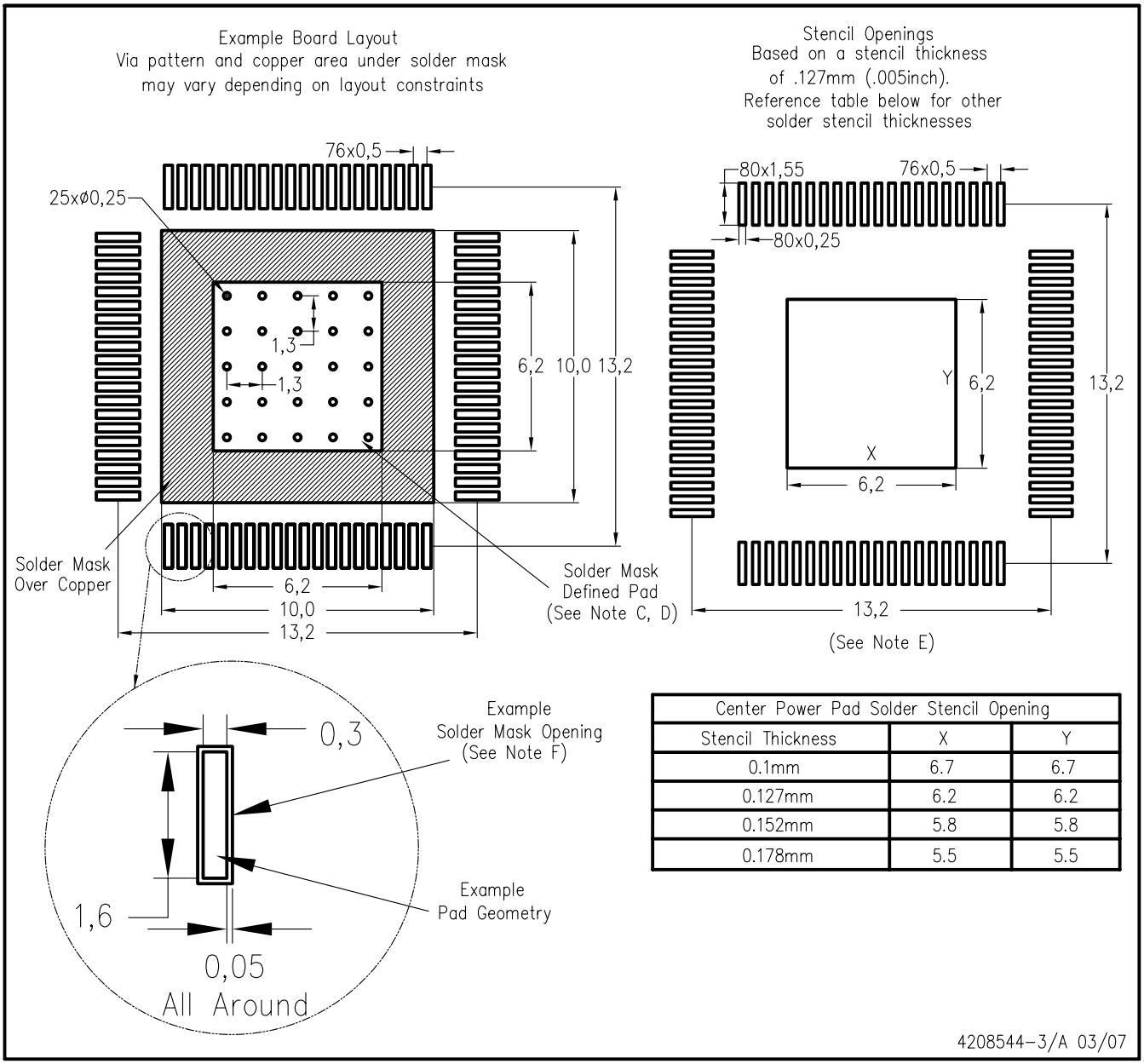


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PFP (S–PQFP–G80) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.7	6.7
0.127mm	6.2	6.2
0.152mm	5.8	5.8
0.178mm	5.5	5.5

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–SM–782 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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