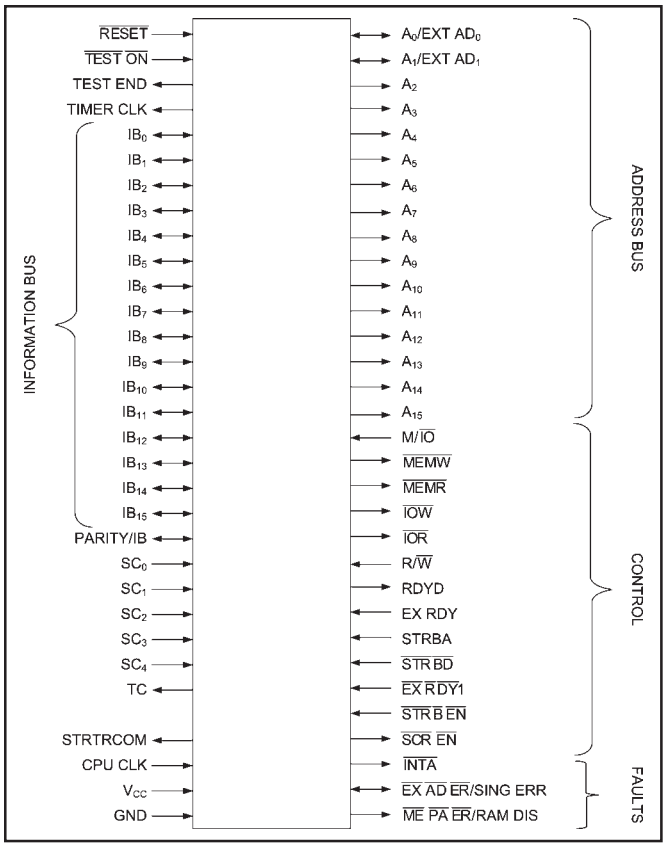
PACE1754
SINGLE CHIP, 40MHz CMOS PROCESSOR INTERFACE CIRCUIT (PIC)

FEATURES

- **The PACE1754 (PIC) is a support chip for the PACE1750A/AE Processor. It eliminates the SSI/ MSI Logic and external system functions required in typical 1750A implementations.**
- **Provides a significant savings in part-count and power dissipation enhancing reliability and overall system speed performance.**
- **Provides an optimal interface when used with the PACE1753 MMU/COMBO in a full 1750A implementation.**
- **Provides the following additional important system functions:**
  - **— Programmable READY for memory and I/O**
  - **— Automatic READY during self-test and internal I/O instructions**
  - **— 100KHz timer clock output provided**
  - **— Programmable system watchdog—ranges from 1 µs to 1 minute**
  - **— Programmable Bus time-out function**
  - **— Memory Parity generation/detection**
  - **— Error detection of unimplemented memory and/or I/O space addressing**
  - **— First failing memory address register for diagnostics**
  - **— High drive three-state address latches**
  - **— Built-in system test program—automatically tests the PACE1750A/AE CPU, PACE1753 MMU/COMBO, PACE1754 PIC and system address lines as well as memory and I/O strobes**
  - **— System configuration decoding and buffering**
  - **— Interrupt acknowledge decoder and strobe**
  - **— Start up ROM support per MIL-STD-1750A**
  - **— Memory or I/O READ/WRITE three-state strobes with external three-state control for DMA applications**
- **20, 30 and 40 MHz operation over full Military Temperature Range**
- **Single 5V ± 10% Power Supply**
- **Power Dissipation over Military Temperature Range**
  - **< 0.25 watts at 20 MHz**
  - **< 0.30 watts at 30 MHz**
  - **< 0.35 watts at 40 MHz**
- **Available in:**
  - **— 64-Pin DIP or Gull Wing (50 Mil Pin centers)**
  - **— 68-Pin Pin Grid Array (PGA) (100 Mil centers)**
  - **— 68-Lead Quad Pack**



PACE1754 PROCESSOR INTERFACE CIRCUIT DESCRIPTION

The PACE1754 Processor Interface Circuit (PIC) is a single chip implementation of many special system functions that are often required when using the PACE1750A/AE, single chip, 40MHz CMOS Microprocessor. The PIC allows a system designer to design a higher performance, more effecient microprocessor system which uses less power and takes up less board space than was previously possible.

In addition to providing significant savings in part count and power dissipation the PIC uses only a 5V ±10%, single supply and operates at 20, 30 and 40 MHz over the fully Military Temperature Range. The PIC provides many important system functions. These functions are governed by respective bit positions in a programmable Control Register which is incorporated in the PIC. The individual bits of the control register are set to select the various features and are set to a specified default value upon Reset.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage Range	0.5V to +7.0V
Input Voltage Range	0.5V to V_{CC} + 0.5V
Storage Temperature Range	–65°C to +150°C
Input Current Range	–30mA to +5mA
Current applied to any output[3]	150mA
Maximum Power Dissipation[2]	1.5W
Lead Temperature Range (soldering 10 seconds)	300°C
Thermal resistance (θ_{JC}):[4]	
Cases X and T	8°C/W
Cases Y and U	5°C/W
Case Z	6°C/W

Notes:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Must withstand the added power dissipation due to short circuit test e.g., I_{OS}.
3. Duration 1 second or less.
4. Device Type Definitions from 5962-88642 SMD:
   - Case X: Dual In-Line
   - Case T: Dual In-Line with Gull-Wing Leads
   - Case Y: Leaded Chip Carrier with Gull-Wing Leads
   - Case U: Leaded Chip Carrier with Unformed Leads
   - Case Z: Pin Grid Array

RECOMMENDED OPERATING CONDITIONS

Case Temperature	GND	V_{CC}
–55°C to +125°C	0	4.5V to +5.5V

DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Conditions[1]
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	V	
V_{IL}	Input LOW Voltage	–0.5	0.8	V	
V_{CD}	Input Clamp Diode Voltage		–1.2	V	V_{CC} = 4.5V, I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	2.4		V	V_{CC} = 4.5V, I_{OH} = –8.0mA
		V_{CC} – 0.2		V	V_{IN} = 0.8V, 2.0V I_{OH} = –300µA
V_{OL}	Output LOW Voltage,		0.5	V	V_{CC} = 4.5V, I_{OL} = 8.0mA
	except A_0 – A_{15}		0.2	V	V_{IN} = 0.8V, 2.0V I_{OL} = 300µA
V_{OL}	Output LOW Voltage,		0.5	V	V_{CC} = 4.5V, I_{OL} = 20.0mA
	A_0 – A_{15}		0.2	V	V_{IN} = 0.8V, 2.0V I_{OL} = 300µA
I_{IH}	Input HIGH Current, except IB_0 – IB_{15}, parity/IB_{16}, SING ERR, A_0/EXT AD_0, A_1/EXT AD_1, STRBA		10	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V
I_{IH}	Input HIGH Current, IB_0 – IB_{15}, parity/IB_{16}, A_0/EXT AD_0, A_1/EXT AD_1		50	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V
I_{IH}	Input HIGH Current, STRBA, SING ERR		500	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V
I_{IL}	Input LOW Current, except IB_0 – IB_{15}, parity/IB_{16}, SING ERR, A_0/EXT AD_0, A_1/EXT AD_1, $\overline{\text{STRBD}}$, $\overline{\text{TEST ON}}$		–10	µA	V_{IN} = GND, V_{CC} = 5.5V
I_{IL}	Input LOW Current, IB_0 – IB_{15}, parity/IB_{16}, SING ERR, A_0/EXT AD_0, A_1/EXT AD_1		–50	µA	V_{IN} = GND, V_{CC} = 5.5V
I_{IL}	Input LOW Current, $\overline{\text{STRBD}}$, $\overline{\text{TEST ON}}$		–500	µA	V_{IN} = GND, V_{CC} = 5.5V
I_{OZH}	Output Three-State Current		50	µA	V_{OUT} = 2.4V, V_{CC} = 5.5V
I_{OZL}	Output Three-State Current		–50	µA	V_{OUT} = 0.5V, V_{CC} = 5.5V
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels)		10	mA	V_{IN} < 0.2V or > V_{CC} – 0.2V f = 0MHz, Outputs Open, V_{CC} = 5.5V
I_{CCQT}	Quiescent Power Supply Current (TTL Input Levels)		50	mA	V_{IN} = 3.4V, f = 0MHz, All Inputs, Outputs Open, V_{CC} = 5.5V
I_{CCD}	Dynamic Power Supply Current f = 20MHz		40	mA	V_{IN} = 0V to V_{CC},
	f = 30MHz		50	mA	tr = tf = 2.5 ns typ.,
	f = 40MHz		60	mA	Outputs Open, V_{CC} = 5.5V
I_{OS}	Output Short Circuit Current[2]	–25		mA	V_{OUT} = GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance		10	pF	Inputs Only
C_{OUT}	Output/Bi-directional Capacitance		15	pF	Outputs Only (Including I/O Buffers)

Notes:

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. Duration of the short should not exceed one second; only one output may be shorted at a time.

AC ELECTRICAL CHARACTERISTICS[1, 2]

(V_{CC} = 5V ± 10% Over Recommended Operating Conditions)

Symbol	Parameter	20 MHz		30MHz		40 MHz		Unit
		Min	Max	Min	Max	Min	Max	
tEX RDY $(RDYD)_V$	Time from External Ready to Ready Data Valid		16		14		12	ns
tC $(RDYD)_V$	Time from Clock Read to Ready Data Valid		28		22		16	ns
$tSTRBA_H$ $(A)_V$	Time from Strobe Address HIGH to Address Bus Valid		29		21		19	ns
$tIBA_V$ $(A)_V$	Time from Information Bus Address to Address Bus Valid		31		22		20	ns
tFC $(R)_L$	Time from Falling Clock to Read LOW		24		18		12	ns
$t\overline{STRBD}_H$ $(R)_H$	Time from Strobe Data HIGH to Read HIGH		24		18		12	ns
$t\overline{STRBD}_L$ $(W)_L$	Time from Strobe Data LOW to Write LOW		26		20		15	ns
$t\overline{STRBD}_H$ $(W)_H$	Time from Strobe Data HIGH to Write HIGH		26		20		15	ns
$tIBD_{IN}$ $(\overline{ME\ PA\ ER})_L$	Time from Information Bus Data into Memory Parity Error LOW		22		17		12	ns
$tIBA_{IN}$ $(\overline{EX\ AD\ ER})$	Time from Information Bus Address into External Address Error		30		25		20	ns
$t\overline{STRBD}_L$ – $(STRT\ ROM)_V$	Time from Strobe Data LOW to Start-up ROM Valid		26		20		15	ns
tFC $(IB\ OUT)_V$	Time from Falling Clock to Information Bus Valid		30		25		25	ns
tC (TIMER CLK)	Time from Rising Edge of Clock to Timer Clock		30		25		20	ns
tIB IN_V (IB16)	Time from Information Bus Data to Parity Valid		25		20		18	ns
tEXT AD (CLKB3)	Extended Address Setup Time	10		10		10		ns
$t\overline{EX\ RDY}1$ $(RDYD)_V$	Time from External Ready Data to Ready Data Valid		28		24		21	ns
tFC $(\overline{SCR\ EN})$	Time from Falling Clock to SCR Enable; Case Types T and X only		30		24		24	ns
$t\overline{STRBD}_H$ $(\overline{SCR\ EN})$	Time from STRBD HIGH to SCR Enable; Case Types T and X only		30		24		24	ns

Notes:

1. $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_C \le +125°C$. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. All measurements of delay times on active signals are related to the 1.5V levels.

TERMINAL CONNECTIONS

Case Outlines: Dual-In-Line (Case X) and Dual-In-Line with Gull-Wing Leads (Case T)					
Terminal Number	**Terminal Symbol**	**Terminal Number**	**Terminal Symbol**	**Terminal Number**	**Terminal Symbol**
1	GND	23	IB_{13}	45	A_3
2	$\overline{SCR\ EN}$	24	IB_{14}	46	GND
3	$\overline{TEST\ ON}$	25	IB_{15}	47	A_2
4	V_{CC}	26	IB_{16}	48	A_1/EXT AD_1
5	$\overline{RESET}$	27	$\overline{ME\ PA\ ER}$/RAM DIS	49	A_0/EXT AD_0
6	TEST END	28	$\overline{EX\ AD\ ER}$/SING ERR	50	TC
7	TIMER CLK	29	$\overline{INTA}$	51	CPU CLK
8	$\overline{EX\ RDY}_1$	30	STRT ROM	52	STRBA
9	IB_0	31	V_{CC}	53	$\overline{STR\ BD}$
10	IB_1	32	GND	54	$\overline{STR\ B\ EN}$
11	IB_2	33	A_{15}	55	EX RDY
12	IB_3	34	A_{14}	56	RDYD
13	IB_4	35	A_{13}	57	R/$\overline{W}$
14	IB_5	36	A_{12}	58	GND
15	IB_6	37	A_{11}	59	M/$\overline{IO}$
16	IB_7	38	A_{10}	60	$\overline{MEMW}$
17	IB_8	39	A_9	61	$\overline{MEMR}$
18	IB_9	40	A_8	62	$\overline{IOW}$
19	GND	41	A_7	63	$\overline{IOR}$
20	IB_{10}	42	A_6	64	V_{CC}
21	IB_{11}	43	A_5		
22	IB_{12}	44	A_4		

TERMINAL CONNECTIONS

Case Outlines: Leaded Chip Carrier with unformed leads (Case U) and Leaded Chip Carrier with Gull-Wing Leads (Case Y)

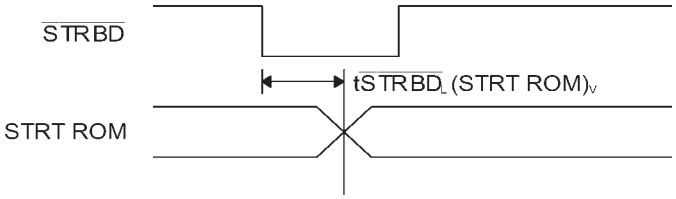
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	24	IB_{12}	47	A_3
2	SC_0	25	IB_{13}	48	GND
3	SC1	26	IB_{14}	49	A_2
4	$\overline{\text{TEST ON}}$	27	IB_{15}	50	A_1/EXT AD_1
5	$\overline{\text{RESET}}$	28	PARITY/IB_{16}	51	A_0/EXT AD_0
6	TEST END	29	$\overline{\text{ME PA ER}}$/RAM DIS	52	SC_4
7	TIMER CLK	30	$\overline{\text{EX AD ER}}$/SING ERR	53	SC_3
8	SC_2	31	$\overline{\text{INTA}}$	54	TC
9	V_{CC}	32	STRT ROM	55	CPU CLK
10	IB_0	33	V_{CC}	56	STRBA
11	IB_1	34	GND	57	$\overline{\text{STRBD}}$
12	IB_2	35	A_{15}	58	$\overline{\text{STRBEN}}$
13	IB_3	36	A_{14}	59	EX RDY
14	IB_4	37	A_{13}	60	RDYD
15	IB_5	38	A_{12}	61	R/$\overline{W}$
16	IB_6	39	A_{11}	62	GND
17	IB_7	40	A_{10}	63	M/$\overline{IO}$
18	$\overline{\text{EX RDY}}_1$	41	A_9	64	$\overline{\text{MEMW}}$
19	IB_8	42	A_8	65	$\overline{\text{MEMR}}$
20	IB_9	43	A_7	66	$\overline{\text{IOW}}$
21	GND	44	A_6	67	$\overline{\text{IOR}}$
22	IB_{10}	45	A_5	68	V_{CC}
23	IB_{11}	46	A_4		

TERMINAL CONNECTIONS

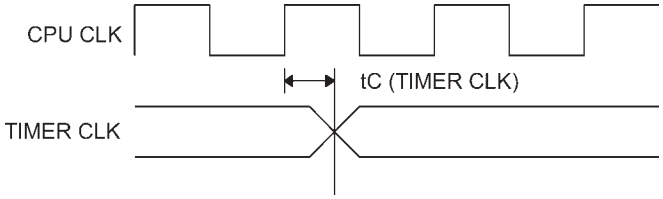
Case Outline: Pin Grid Array (Case Z)

Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
B1	V_{CC}	L5	SC_1	D11	A_3
B2	IB_{14}	K5	SC_0	D10	A_4
C1	IB_{13}	L6	V_{CC}	C11	A_5
C2	IB_{12}	K6	$\overline{IOR}$	C10	A_6
D1	IB_{11}	L7	$\overline{IOW}$	B11	A_7
D2	IB_{10}	K7	$\overline{MEMR}$	A10	GND
E1	IB_9	L8	$\overline{MEMW}$	B10	A_8
E2	IB_8	K8	$M/\overline{IO}$	A9	A_9
F1	$\overline{EX\ RDY}_1$	L9	GND	B9	A_{10}
F2	IB_7	K9	$R/\overline{W}$	A8	A_{11}
G1	IB_6	L10	RDYD	B8	A_{12}
G2	IB_5	K11	EX RDY	A7	A_{13}
H1	IB_4	K10	$\overline{STRB\ EN}$	B7	A_{14}
H2	IB_3	J11	$\overline{STRBD}$	A6	A_{15}
J1	IB_2	J10	STRBA	B6	GND
J2	IB_1	H11	CPU CLK	A5	V_{CC}
K1	IB_0	H10	TC	B5	STRT ROM
L2	GND	G11	SC_3	A4	$\overline{INTA}$
K2	SC_2	G10	SC_4	B4	$\overline{EX\ AD\ ER}$
L3	TIMER CLK	F11	A_0/EXT AD_0	A3	$\overline{ME\ PA\ ER}$
K3	TEST END	F10	A_1/EXT AD_1	B3	PARITY/IB_{16}
L4	$\overline{RESET}$	E11	A_2	A2	IB_{15}
K4	$\overline{TEST\ ON}$	E10	GND		

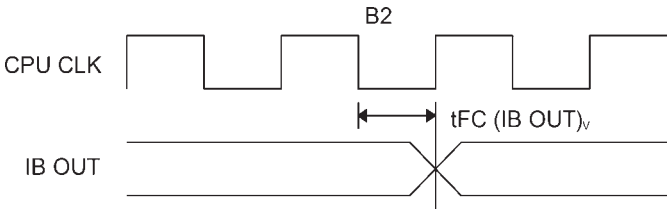
STRT ROM



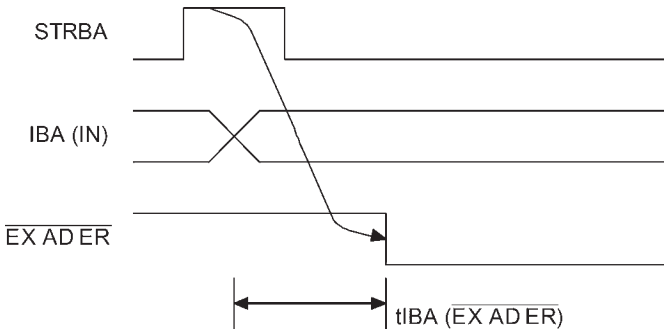
Timer Clk



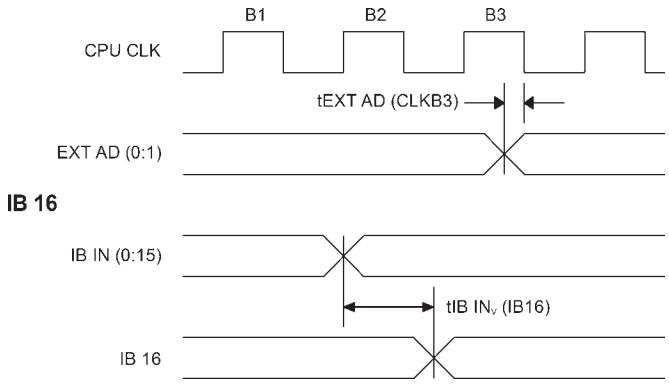
IB Bus Output (0:15)



EX AD ER

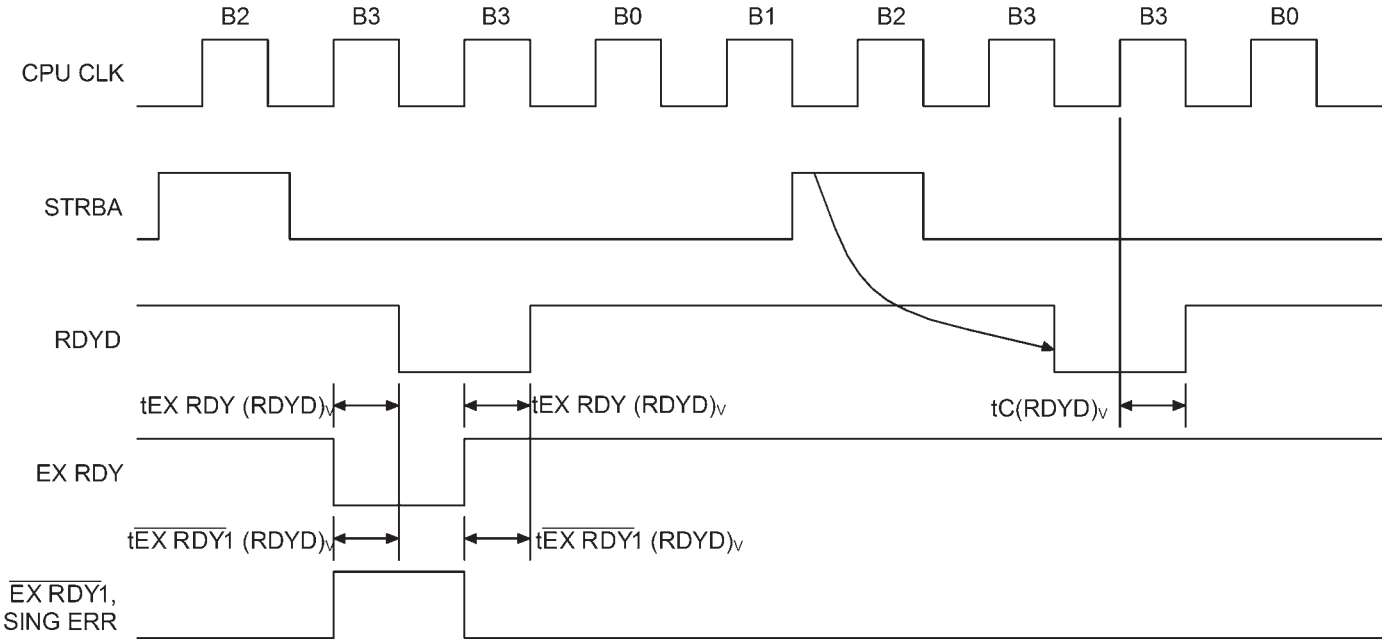


Extended Addresses (0:1)

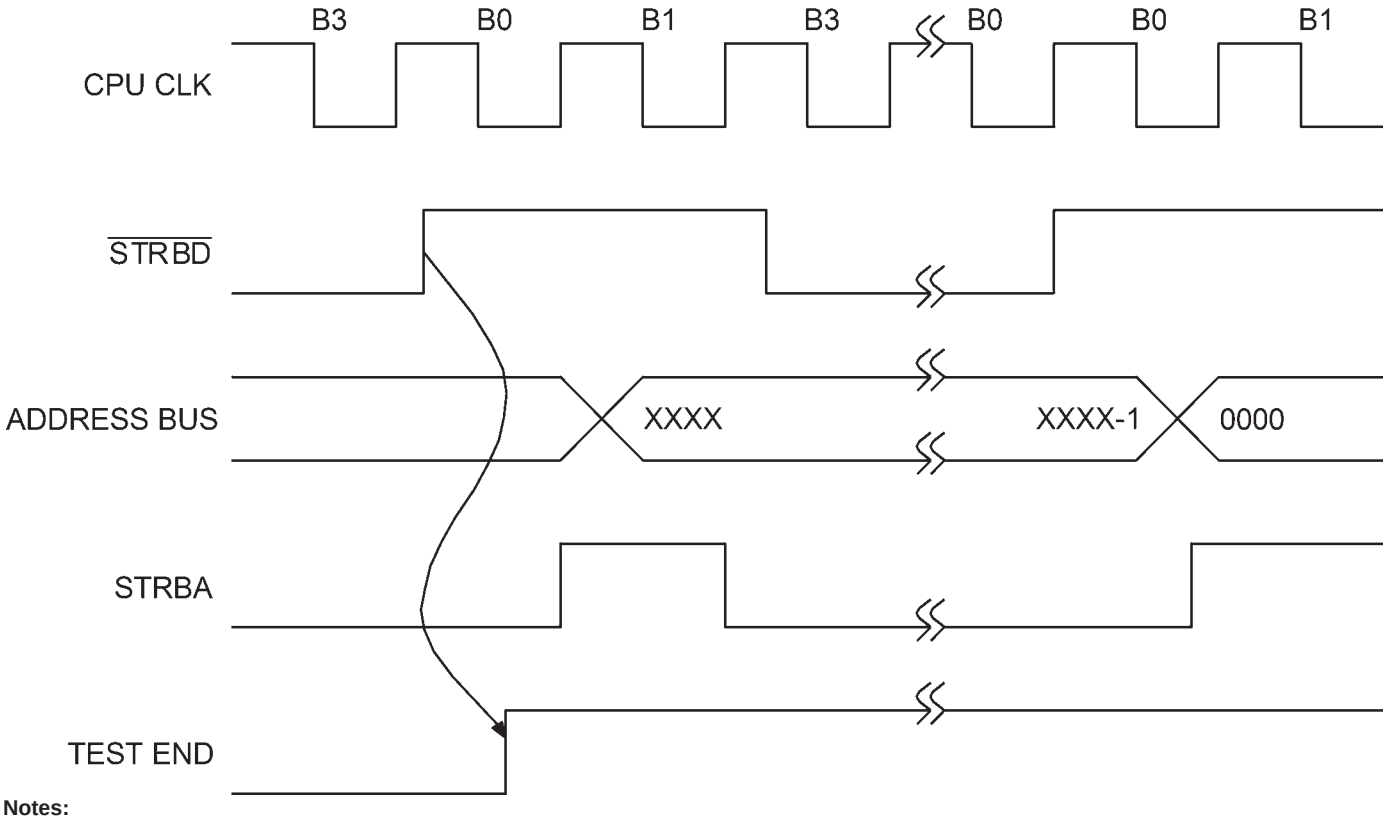


Note: All time measurements on active signals relate to 1.5V levels.

RDYD Timing



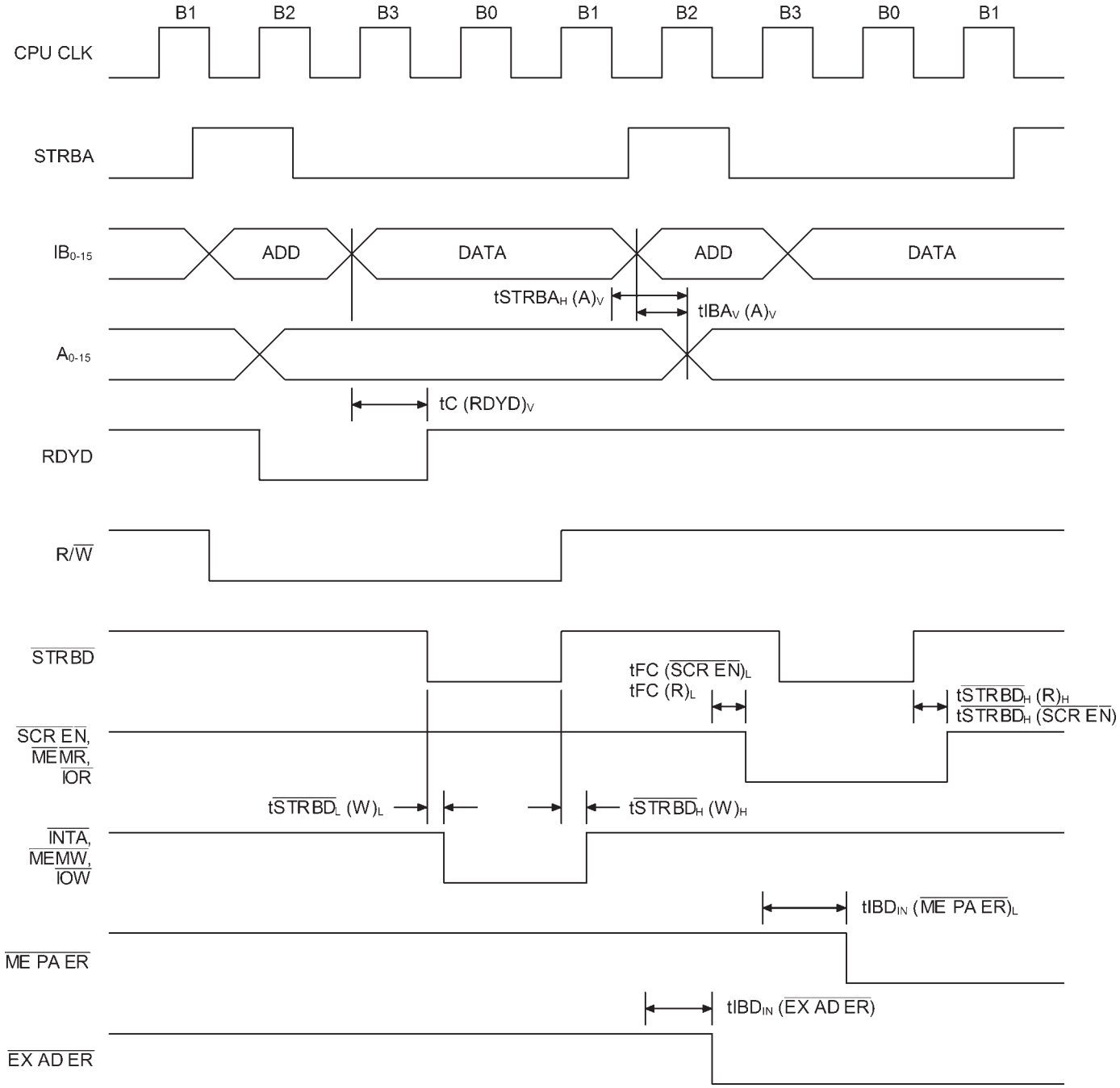
TEST END Timing[1]



Notes:

1. The last two instructions executed during system test are: XIO RA, 1F44, 0 and JC 7, 0000 hex, 0. After execution of the IOW bus cycle, the XIO proceeds by filling the instruction pipe with two memory read bus cycles where the opcode 7070 hex and 0000 hex are entered to the processor. As from the end of STRBD in the second cycle, TEST END is asserted. At this point, the execution of IC starts by first issuing two fetch cycles from the "old PC" (from addresses XXXX & XXXX+1). The data will be taken from system memory (because TEST END is asserted) but both the address and data are irrelevent. Following that, IC will start filling the pipe from address 0000 hex and 0001 hex, now from the system memory to start user's program execution.
2. All time measurements on active signals relate to 1.5V levels.

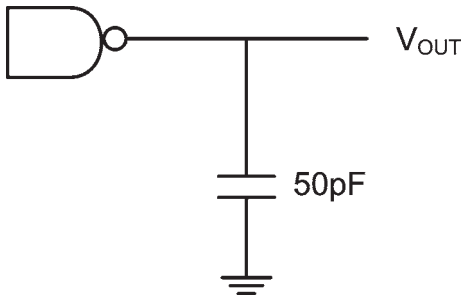
Address Bus and Strobes



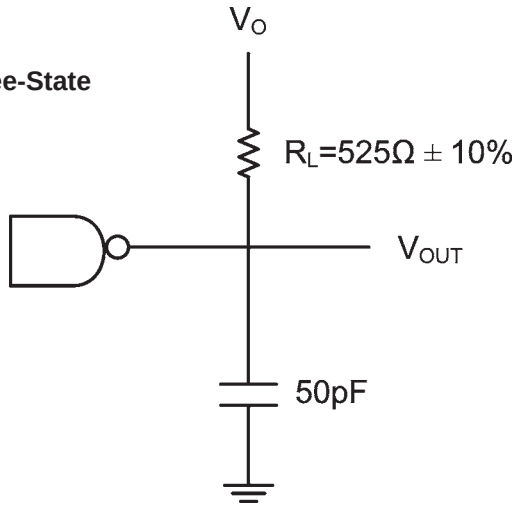
Note: All time measurements on active signals relate to 1.5V levels.

TEST CIRCUITS

Standard Output (Non Three-State)



Three-State



Note: All time measurements on active signals relate to 1.5V levels.

Parameter	V_O	V_{MEA}
TPLZ	≥ 3V	0.5V
TPHZ	0V	V_{CC} – 0.5V
TPXL	V_{CC}/2	1.5V
TPXH	V_{CC}/2	1.5V

PIN FUNCTIONS

Symbol	Name	Description
CPU CLK	CPU Clock	A single-phase input clock signal (0-40MHz, 40% to 60% duty cycle.)
STRBA	Strobe Address	An active HIGH input which latches the contents of IB(0:15) into the address latches.
$\overline{\text{STRBD}}$	Strobe Data	An active LOW input which is used for writing or reading data to or from the device and also to produce the external memory and I/O strobes.
TIMER CLK	Timer Clock	A 100KHz output (fixed frequency) based on the programmed operating frequency of the CPU clock.
$\overline{\text{MEMW}}$	Memory Write Strobe	An active LOW output produced in memory write cycles.
$\overline{\text{MEMR}}$	Memory Read Strobe	An active LOW output produced in memory read cycles.
$\overline{\text{IOW}}$	I/O Write Strobe	An active LOW output produced in output write cycles.
$\overline{\text{IOR}}$	I/O Read Strobe	An active LOW output produced in input read cycles.
$\overline{\text{INTA}}$	Interrupt Acknowledge Strobe	An active LOW output produced after any interrupt, corresponding to an output write to address 1000 (hex).
$\overline{\text{SCR EN}}$	System Configuration	An active LOW output (in 64 pin only) produced any time an input read from address 8410 (hex), read system configuration is executed.
$\overline{\text{STRB EN}}$	Strobe Enable	An active LOW input, enabling the active state of the address outputs and the $\overline{\text{MEMR}}$, $\overline{\text{MEMQ}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$ outputs. When at a logic "1" (if enabled by bits EST, EAD of the control register) it will correspondingly enable the three-state state of the above signals.
IB_0 - IB_{15}	Information Bus (0:15)	A bi-directional time multiplexed bus. It is an input during the address phase of any bus cycle and also during the data phase when writing. It is an output during the data phase when reading from the device.
IB_{16}	Information Bus (16)	A bi-directional line. It is an output during write cycles and an input during read cycles. It is used to implement the parity function at the system level.
A(0:1)/ EX AD(0:1), A(2:15)	Address Bus (0:15)	An active HIGH output bus. Contains the address of the current bus cycle as latched by the end of STRBA. In system configurations including the MMU function, the only active lines during memory are A(4:15). In this case, A(2:3) are high impedance (don't care) and A(0:1) turn into inputs called Extended Addresses, EXT ADR (0:1). In this case, these two lines supplied by the MMU, will be used to operate the programmable ready generation during bus cycles.
M/$\overline{\text{IO}}$	Memory I/O	An input qualifier indicating the nature of the current bus cycle.

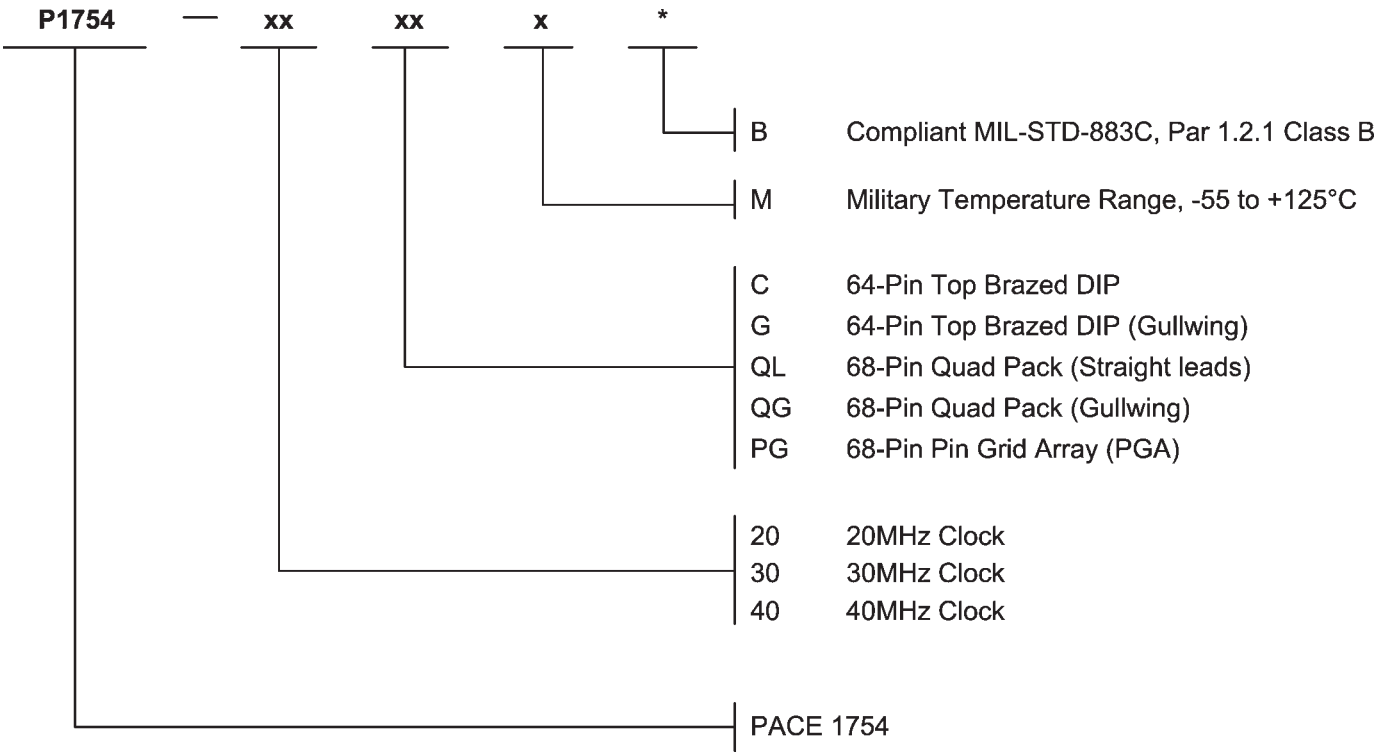
PIN FUNCTIONS (Continued)

Symbol	Name	Description
R/$\overline{W}$	Read or Write	An input qualifier indicating the nature of the current bus cycle, either Read (1) or Write (0).
$\overline{RESET}$	External Reset	An active LOW input used to initialize the device's hardware.
$\overline{TEST\ ON}$	System Test Enable	An active LOW input used to enable the execution of the System Test built into the device, immediately after completion of the P1754 initialization and before fetching any instruction from the user program.
TEST END	System Test End	An active HIGH output indicating whether the system test in the device has been completed. Whenever the system test is disabled by the $\overline{TEST\ ON}$ signal, the TEST END output will be at a logical "1" immediately after RESET is removed.
STRT ROM	Start Up ROM	An output following the execution of the ESUR and DSUR, I/O commands as defined in MIL-STD-1750A. It will be at the logical "1" level after executing ESUR and at the logical "0" level after executing DSUR. Initially, it defaults to a logical "1".
RDYD	Ready Data	An active HIGH output to be connected to the P1750A/AE CPU input to control the bus cycle termination.
EX RDY	External Ready Data	An active HIGH input which at logical "0" overrides the internal RDYD generation and forces it to a logical "0".
$\overline{EX\ RDY}$1	External Ready Data	An active LOW input which at logical "1" overrides the internal RDYD generation and forces it to a logical "0".
$\overline{ME\ PA\ ER}$/ RAM DIS	Memory Parity Error	An active LOW output indicating a parity error when reading from memory. It becomes an active HIGH output called RAM DISABLE for handshaking with the P1753 MMU when the device is programmed to support EDAC.
$\overline{EX\ AD\ ER}$/ SING ERR	Illegal Address Error	An active LOW output indicating an illegal address error when referencing memory or I/O. It becomes an active HIGH output called SINGLE ERROR for handshaking with the P1753 MMU when the device is programmed to support EDAC.
TC	Terminal Count	An active HIGH output indicating a Bus time out or a watchdog trigger.
SC_0–SC_4	System Configuration	Inputs (for case outlines U, Y, and Z only) which are buffered onto IB_0–IB_4 when executing an I/O read from I/O address 8410 (hex), system configuration.
GND	Ground	0 volts system ground.
V_{CC}	Power Supply	5 volts ± 10% power supply.

Case U: Leaded Chip Carrier with Unformed Leads
Case Y: Leaded Chip Carrier with Gull-Wing Leads
Case Z: Pin Grid Array

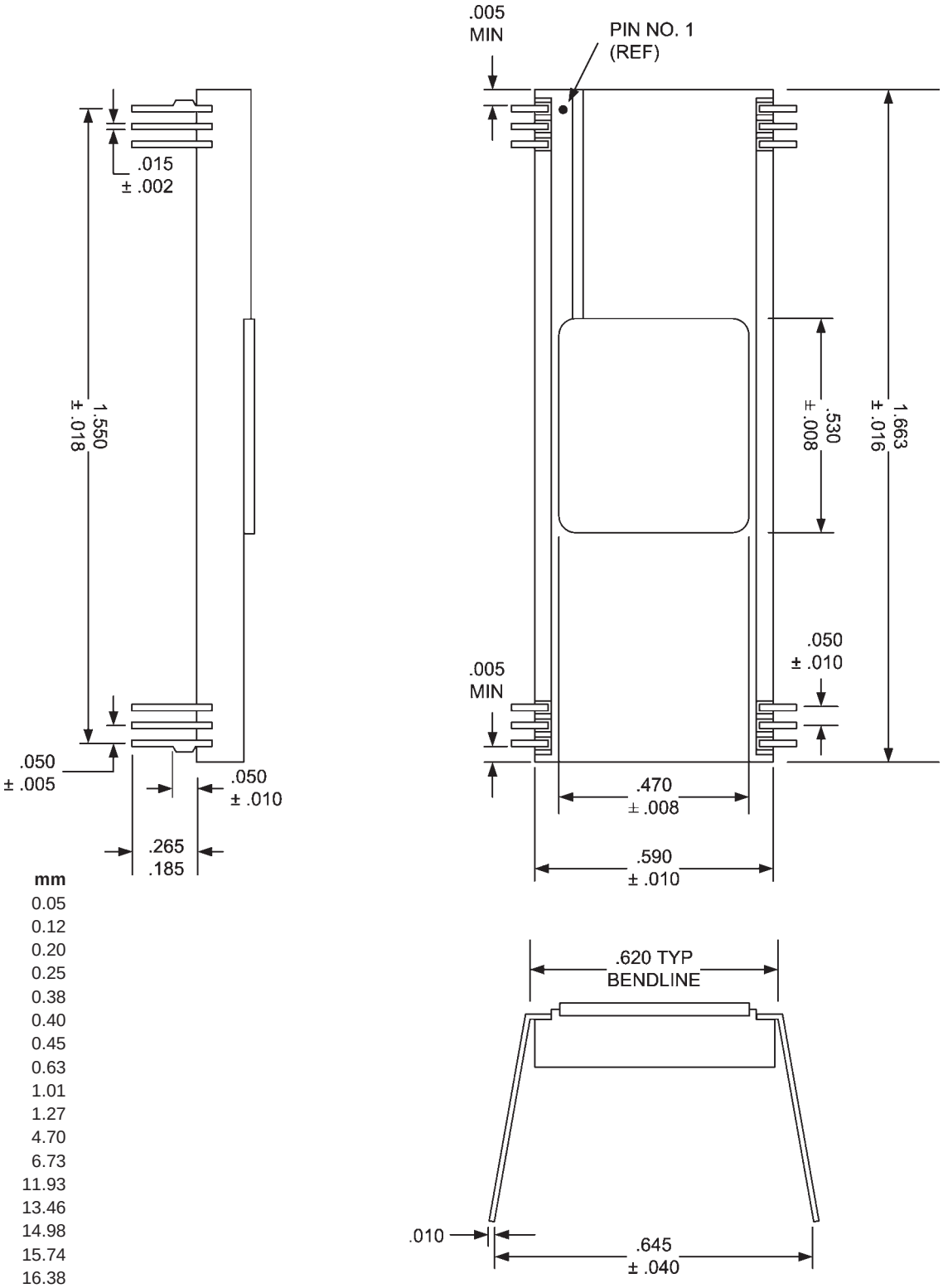
Standardized Military Drawing PIN	Vendor CAGE Number	Vendor similar PIN
5962-8864201UX	3DTT2	P1754-20QLMB
5962-8864201YX	3DTT2	P1754-20QGMB
5962-8864201ZX	3DTT2	P1754-20PGMB
5962-8864202UX	3DTT2	P1754-30QLMB
5962-8864202YX	3DTT2	P1754-30QGMB
5962-8864202ZX	3DTT2	P1754-30PGMB
5962-8864203UX	3DTT2	P1754-40QLMB
5962-8864203YX	3DTT2	P1754-40QGMB
5962-8864203ZX	3DTT2	P1754-40PGMB
5962-8864204TX	3DTT2	P1754-20GMB
5962-8864204XX	3DTT2	P1754-20CMB
5962-8864205TX	3DTT2	P1754-30GMB
5962-8864205XX	3DTT2	P1754-30CMB
5962-8864206TX	3DTT2	P1754-40GMB
5962-8864206XX	3DTT2	P1754-40CMB

ORDERING INFORMATION



CASE OUTLINE X:

64 Lead Top Brazed DIP Package, Straight Lead Version (Ordering Code C)



Inches	mm
.002	0.05
.005	0.12
.008	0.20
.010	0.25
.015	0.38
.016	0.40
.018	0.45
.025	0.63
.040	1.01
.050	1.27
.185	4.70
.265	6.73
.470	11.93
.530	13.46
.590	14.98
.620	15.74
.645	16.38
1.550	39.37
1.563	39.70

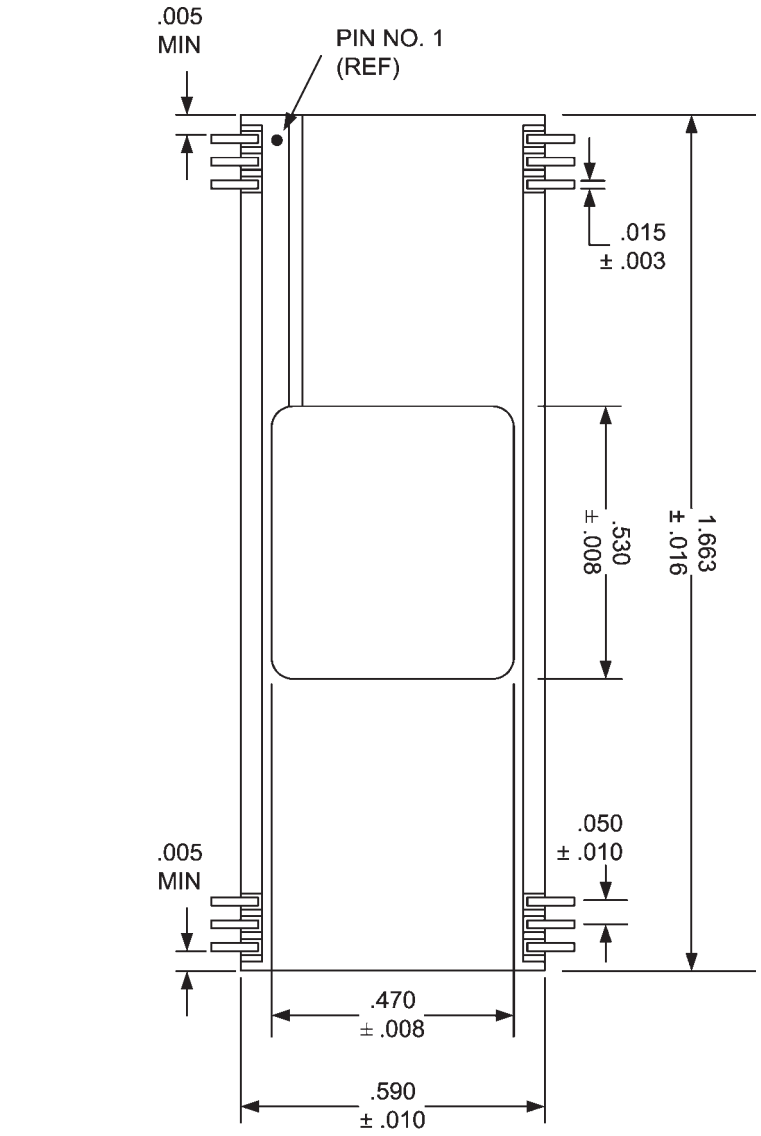
NOTES:

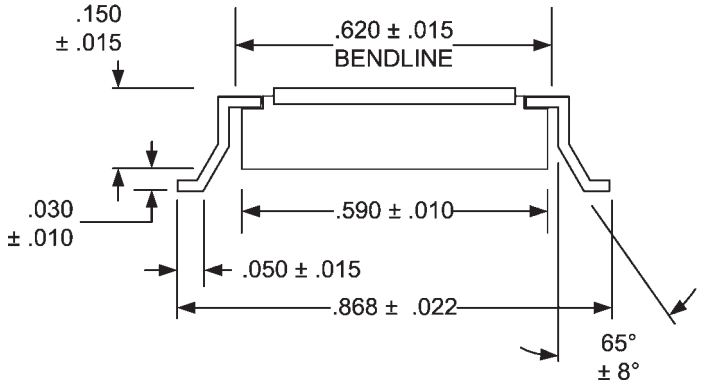
1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.

CASE OUTLINE T:

64 Lead Top Brazed DIP Package, Gullwing Lead Version (Ordering Code G)

Inches	mm
.001	0.03
.003	0.08
.005	0.12
.008	0.20
.010	0.25
.015	0.38
.016	0.41
.022	0.55
.030	0.76
.040	1.01
.050	1.27
.150	3.81
.470	11.93
.530	13.46
.590	14.98
.620	15.74
.868	22.04
1.663	42.24



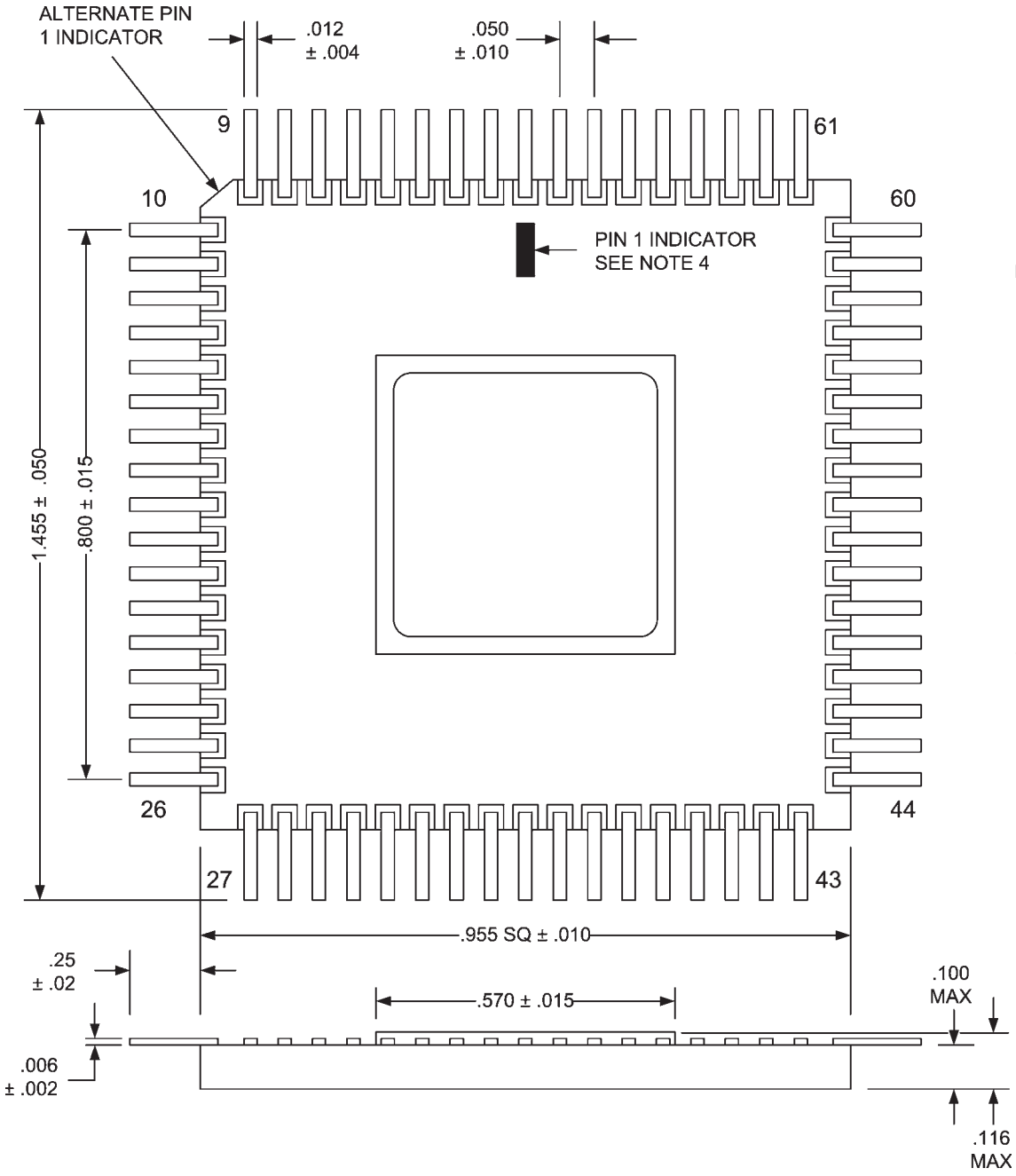


NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Case T is derived from Case X by forming the leads to the shown gullwing configuration.

CASE OUTLINE U:

68 Lead Quad Pack with Straight Leads (Ordering Code QL)



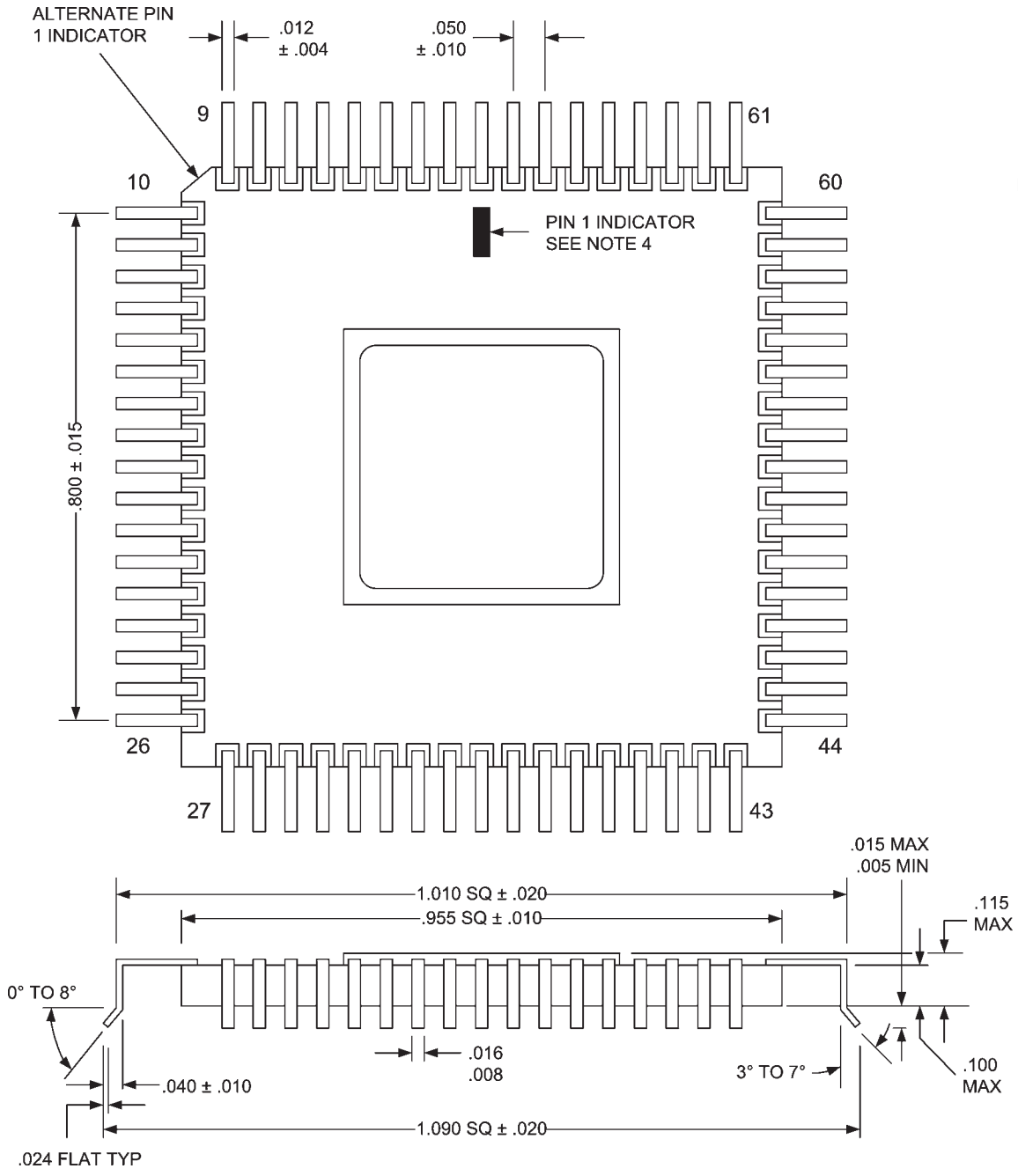
Inches	mm
.002	0.05
.004	0.10
.006	0.15
.010	0.25
.012	0.30
.020	0.51
.050	1.27
.100	2.54
.116	2.95
.250	6.40
.560	14.22
.570	14.48
.800	20.32
.955	24.25
1.090	27.69

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Pin 1 indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5) Corners indicated as notched may be either notched or square.

CASE OUTLINE Y:

68 Lead Quad Pack with Gullwing Leads (Ordering Code QG)



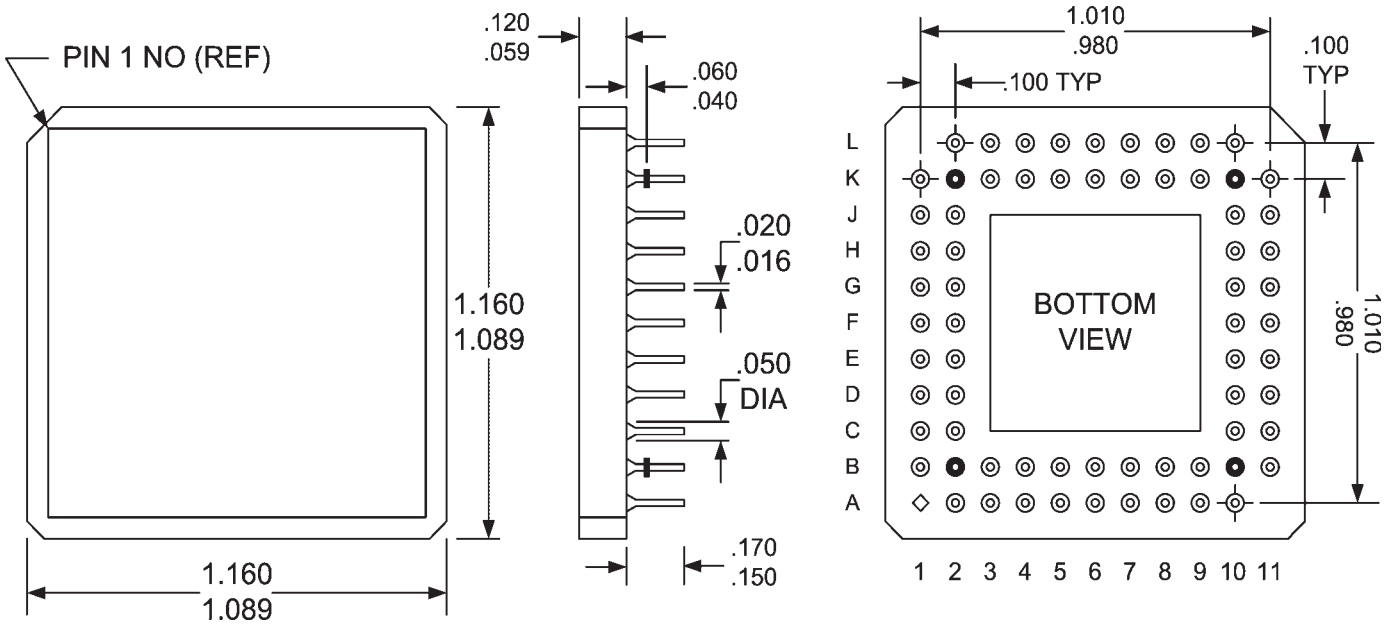
Inches	mm
.004	0.10
.005	0.12
.008	0.20
.010	0.25
.012	0.30
.015	0.38
.016	0.41
.020	0.50
.024	0.60
.040	1.02
.050	1.27
.100	2.54
.115	2.92
.570	14.48
.800	20.32
.955	24.25
1.010	25.65
1.090	27.68

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Pin 1 indicator can either be rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5) Corners indicated as notched my be either notched or square (with radius).
6) Case Y is derived from Case U by forming the leads to the shown gullwing configuration.

CASE OUTLINE Z:

68-Pin Pin Grid Array (PGA) (Ordering Code PG)



Inches	mm
.016	0.41
.020	0.50
.040	1.01
.050	1.27
.059	1.49
.060	1.52
.098	2.49
.100	2.54
.120	3.04
.150	3.81
.170	4.32
1.010	25.65
1.089	27.66
1.160	29.46

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Corners except pin number 1 (ref.) can be either rounded or square.
5) All pins must be on the .100" grid.

REVISIONS

DOCUMENT NUMBER: MICRO-5 **DOCUMENT TITLE**: PACE1754 PIC BULK CMOS			
REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
ORIG	May-89	RKK	New Data Sheet
A	Jul-04	JDB	Added Pyramid logo
B	Aug-05	JDB	Re-created electronic version
C	11/15/05	JDB	Removed Commercial Temperature Range