IZD1520U

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER & DRIVER

FEATURES

- CMOS LSI chips
- Connection with CPU
  Can be directly coupled with 80-port or 68-port system
- Available in chip form or in 100-pin plastic QFP
- Pin-to-Pin Replacement for SED1520 Series
- Many command set
- Total 80 (segment+common) drive sets
- Low power consumption - 30μW maximum at 2kHz external clock
- Power supply V_{DD} - V_{SS} : 2.4 to -7.0V
  V_{DD} - V_5 : 3.5 to -13.0V

DESCRIPTION

The IZD1520 family of dot matrix LCD (Liquid Crystal Display) drivers are designed for the display of characters and graphics.

The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.

The IZD1520 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.

These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

The IZD1520 which is able to drive two lines of twelve characters each.

The IZD1521 which is able to drive 80 segments for extention.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage (1)	V_{SS}	- 8.0 ~ 0.3	V
Supply Voltage (2)	V_5	- 16.5 ~ 0.3	V
Supply Voltage (3)	V_1, V_2, V_3, V_4	V_5 ~ 0.3	V
Input Voltage	V_I	V_{SS} - 0.3 ~ 0.3	V
Output Voltage	V_O	V_{SS} - 0.3 ~ 0.3	V
Power Dissipation	P_D	250	mW
Operating Temperature	T_a	- 10 ~ + 75	°C
Storage Temperature	T_{stg}	- 65 ~ + 150	°C
Soldering temperature time (10 sec max)	T_{sol}	260	°C

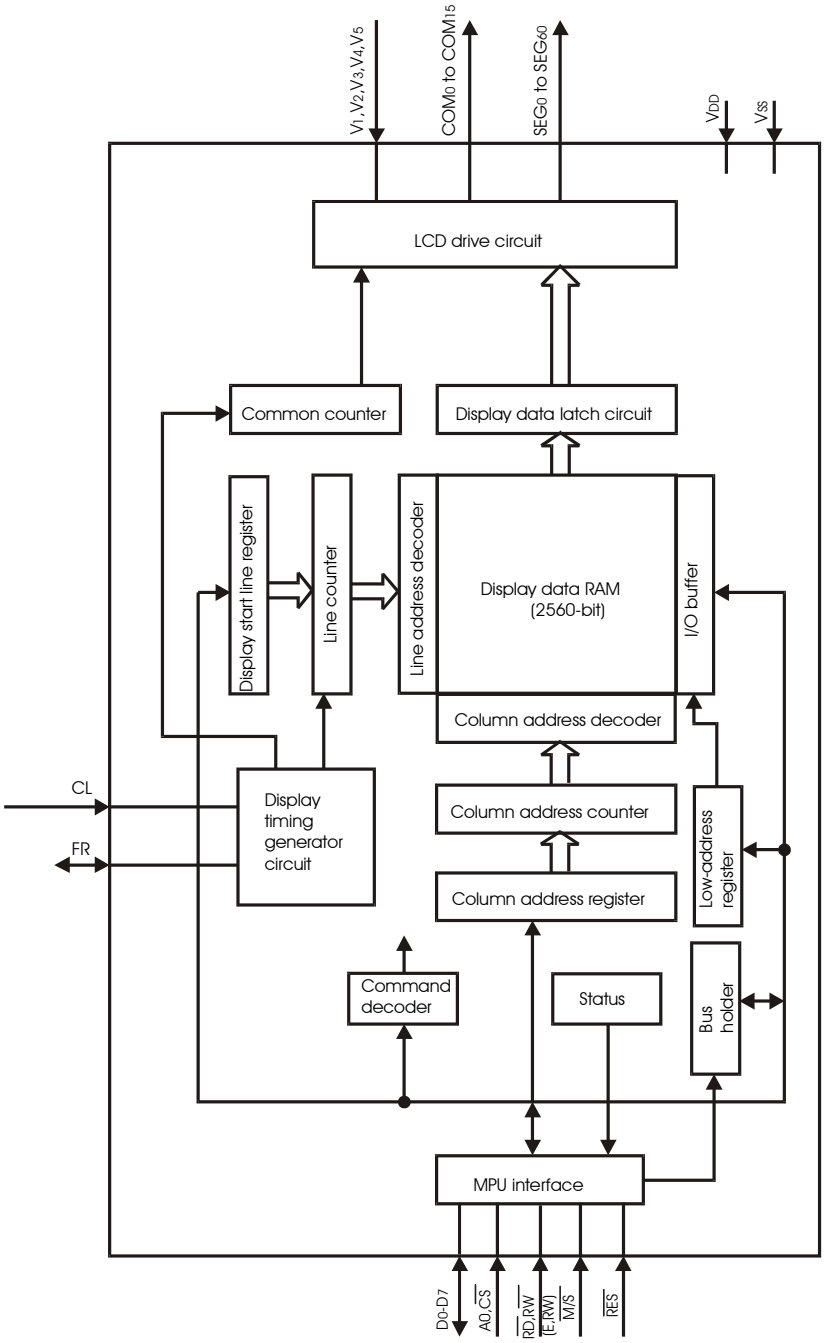
Notes:

1. All voltages are specified relative to V_{DD} = 0V.
2. The following relation must be always hold
   $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operating under these conditions is not implied.

LINE-UP

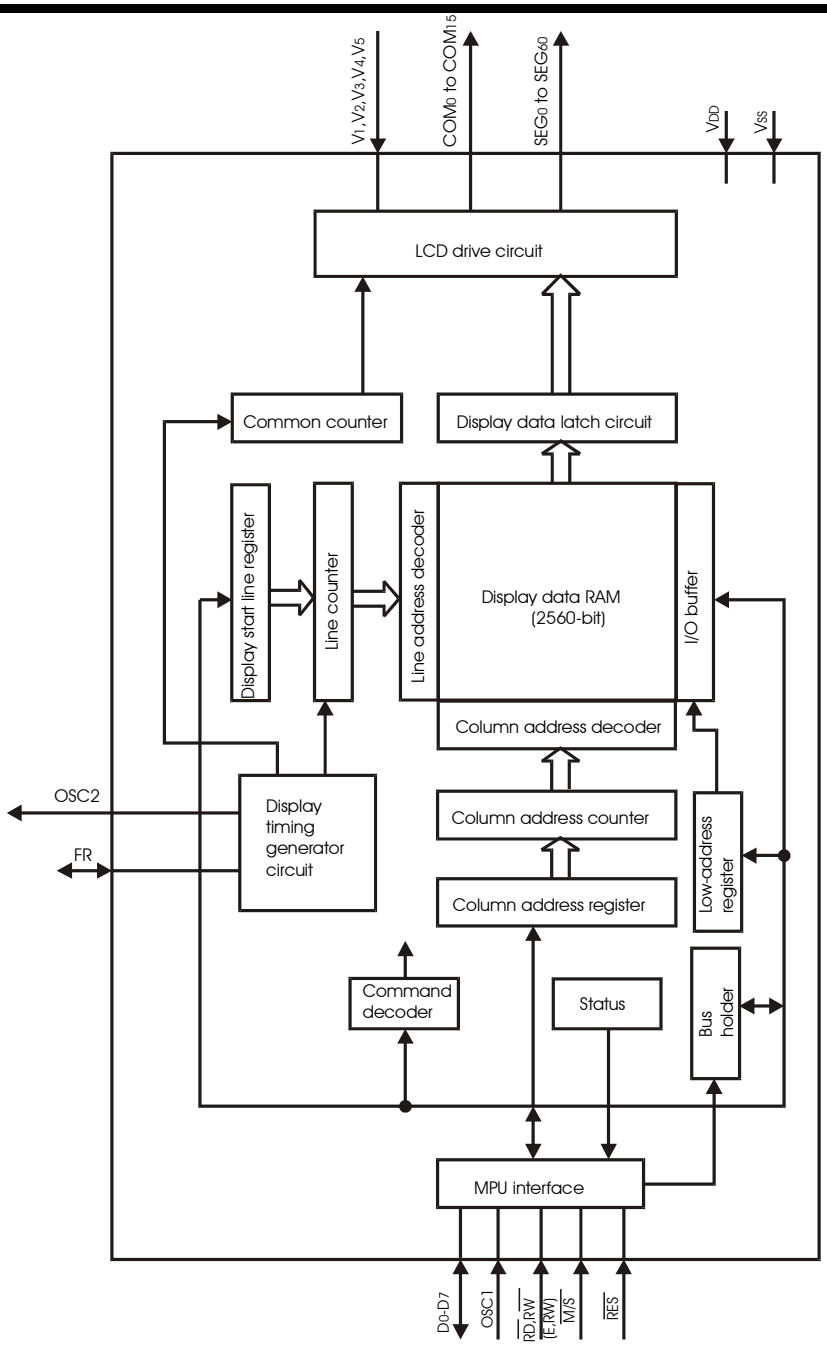
Product Name	Clock Frequency		Applicable Driver	Number of SEGMENT Drivers	Number of COMMON Drivers	Duty
	On-chip	External				
$IZD1520_{OA}$	18kHz	18kHz	$IZ1520_{OA}$, $IZ1521_{OA}$	61	16	1/16, 1/32
$IZD1521_{OA}$	-	18kHz	$IZ1520_{OA}$	80	0	1/8 ~ 1/32
$IZD1520_{AA}$	-	2kHz	$IZ1520_{AA}$, $IZ1521_{AA}$	61	16	1/16, 1/32
$IZD1521_{AA}$	-	2kHz	$IZ1520_{AA}$	80	0	1/8 ~ 1/32

BLOCK DIAGRAM IZ1520AA



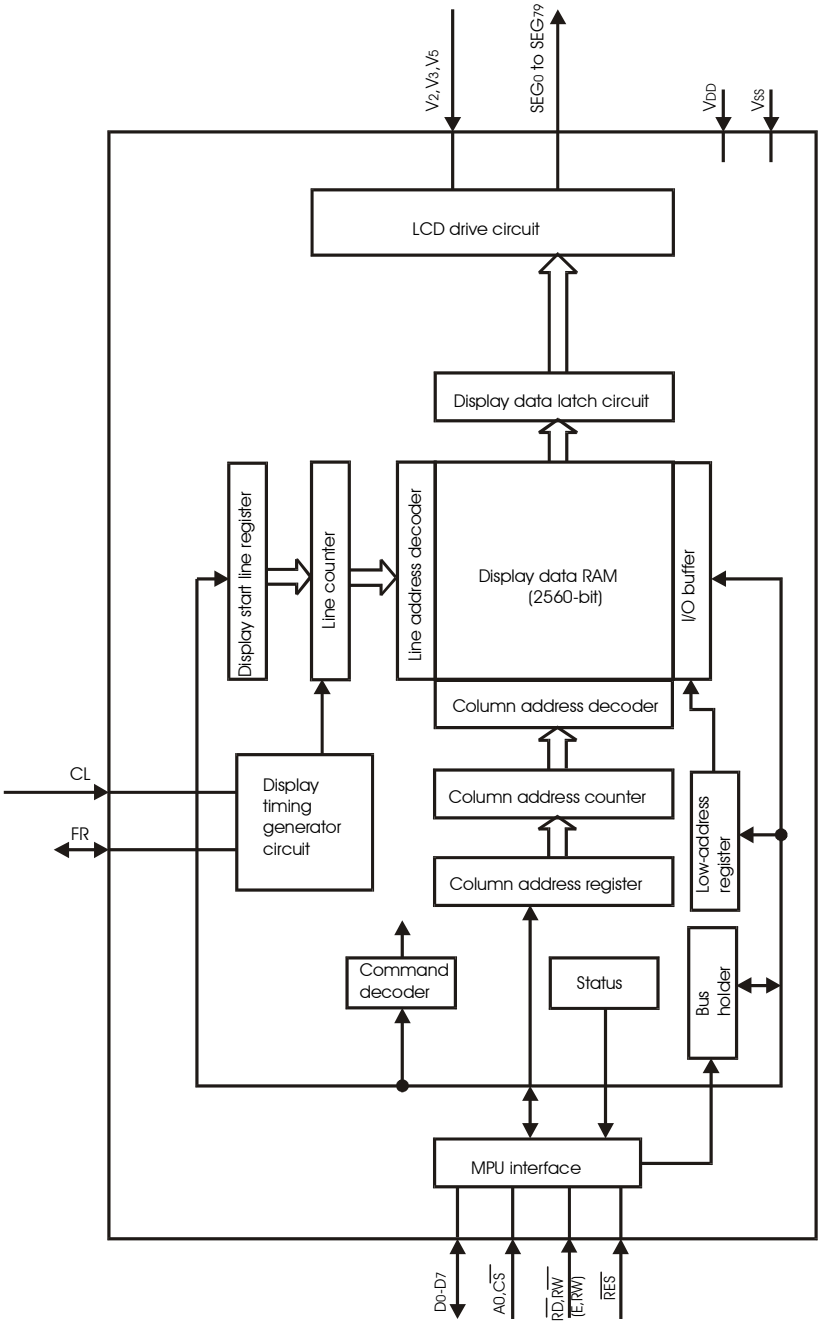
BLOCK DIAGRAM IZD1520OA

INTEGRAL


V1,V2,V3,V4,V5
COM0 to COM15
SEG0 to SEG60
VDD
VSS
LCD drive circuit
Common counter
Display data latch circuit
Display start line register
Line counter
Line address decoder
Display data RAM (2560-bit)
I/O buffer
Column address decoder
OSC2
FR
Display timing generator circuit
Column address counter
Low-address register
Column address register
Command decoder
Status
Bus holder
MPU interface
D0-D7
OSC1
RD,RW
E,RW
M/S
RES

INTEGRAL

BLOCK DIAGRAM IZD1521AA, IZD1521OA



ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{DD} = 0V, V_{SS} = -5.0V unless otherwise specified)

Characteristic		Symbol	Test Condition	Applicable Terminals	Min	Typ	Max	Unit
Operating Voltage(1) Note 1	Recommended	V_{SS}		V_{SS}	-5.5	-5.0	-4.5	V
					-7.0		-2.4	
Operating Voltage(2)	Recommended	V_5		V_5	-13.0		-3.5	V
					-13.0			
	Permitted	V_1, V_2		V_1, V_2	0.6 x V_5		V_{DD}	
	Permitted	V_3, V_4		V_3, V_4	V_5		0.4xV_5	
HIGH Input Voltage		V_{IH}		A0,Di, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}+2.0		V_{DD}	V
				CL, FR, M/$\overline{S}$, $\overline{RES}$	0.2 x V_{SS}		V_{DD}	
LOW Input Voltage		V_{IL}		A0, Di, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}		V_{SS}+0.8	V
				CL, FR, M/$\overline{S}$, $\overline{RES}$	V_{SS}		0.8+V_{SS}	
HIGH Output Voltage		V_{OH}	I_{OH} = -3.0 mA	D0 ÷ D7	V_{SS}+2.4			V
			I_{OH} = -2.0 mA	FR	V_{SS}+2.4			
			I_{OH} = -120 µA	OSC2	0.2 x V_{SS}			
LOW Output Voltage		V_{OL}	I_{OL} = 3.0 mA	D0 ÷ D7			V_{SS}+0.4	V
			I_{OL} = 2.0 mA	FR			V_{SS}+0.4	
			I_{OL} = 120µA	OSC2			0.8xV_{SS}	
Input Leakage Current		I_{LI}		A0, E, R/$\overline{W}$, $\overline{CS}$, CL, M/S, RES	-1.0		1.0	µA
Output Leakage Current		I_{LO}	Outputs are high impedance	D0 ÷ D7, FR	-3.0		3.0	µA
LCD Driver ON Resistance Note 2		R_{ON}	V_5=-5.0V	SEG0 ~ SEG79 COM0 ~ COM15		5.0	7.5	KΩ
Supply Current, Static		I_{DDQ}	$\overline{CS}$ = CL = V_{DD}	V_{DD}		0.05	1.0	µA
Supply Current, Dynamic		I_{DD}	During display V_5=-5.0V, f_{CL}=2kHz Note 3	V_{DD}		2.0	5.0	µA
			During display V_5=-5.0V, R_f =1MΩ Note 4			9.5	15.0	
			During display V_5=-5.0V, f_{CL}=18KHz Note 5			5.0	10.0	
			During access f_{cyc}=200KHz			300	500	µA
Input Terminal Capacity		C_{IN}	f = 1 MHz	All inputs		5.0	8.0	pF
Oscillator Frequency		f_{OSC}	R_f =1MΩ±2%		15	18	21	KHz
Reset Time		t_R		RES	1.0		1000	µs

Notes: 1. Operating over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. For a voltage differential of 0.1V between input (V_1, …, V_4) and output (COM, SEC) pins. All voltages within specified operating voltage range.
3. $IZ1520_{AA}$ and $IZ1521_{AA}$ only. Does not include transient currents due to stray and panel capacitances.
4. $IZ1521_{OA}$ only. Does not include transient currents due to stray and panel capacitances.
5. $IZ1520_{OA}$ only. Does not include transient currents due to stray and panel capacitances.

• Read/Write timing for the 80-port MPU

Characteristic	Symbol	Signal	Condition	Min	Typ	Max	Unit
Address hold time	t_{AH8}	A0, $\overline{CS}$	CL = 100pF	10			ns
Address setup time	t_{AW8}			20			ns
System cycle time	t_{CYC8}	$\overline{WR}$, $\overline{RD}$		1000			ns
Control pulse width	t_{CC8}			200			ns
Data setup time	t_{DS8}	D0 ÷ D7		80			ns
Data hold time	t_{DH8}			10			ns
V_{DD} access time	t_{ACC8}					90	ns
Output Disable time	t_{OH8}			10		60	ns
Low-level pulsewidth	t_{WLCL}	CL		35			µs
High-level pulsewidth	t_{WHCL}			35			µs
Rise time	t_r				30	150	ns
Fall time	t_f				30	150	ns
FR delay time Note 1	t_{FDR}	FR (Input)		-2.0	0.2	2.0	µs
FR delay time Note 2	t_{FDR}	FR (Input)			0.2	2.0	µs

• Read/Write timing for the 68-port MPU

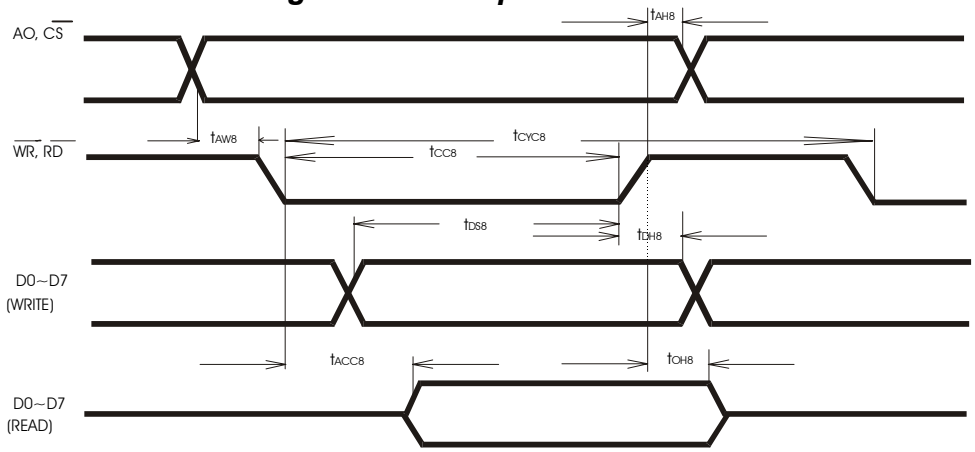
Characteristic		Symbol	Signal	Condition	Min	Typ	Max	Unit
System cycle time		t_{CYC6}	A0	CL = 100pF	1000			ns
Address setup time		t_{AW6}	R/W		20			ns
Address hold time		t_{AH6}			10			ns
Data setup time		t_{DS6}	D0 ÷ D7		80			ns
Data hold time		t_{DH6}			10			ns
Output disable time		t_{OH6}			10		60	ns
Access time		t_{ACC6}					90	ns
Enable pulse width	READ	t_{EW}	E		100			ns
	WRITE				80			ns
Low-level pulsewidth		t_{WLCL}	CL		35			µs
High-level pulsewidth		t_{WHCL}			35			µs
Rise time		t_r				30	150	ns
Fall time		t_f				30	150	ns
FR delay time Note 1		t_{FDR}	FR (Input)		-2.0	0.2	2.0	µs
FR delay time Note 2		t_{FDR}	FR (Input)			0.2	2.0	µs

* The rating when V_{SS} = -3.0V are approximately 100% higher that when V_{SS} = -5.0V

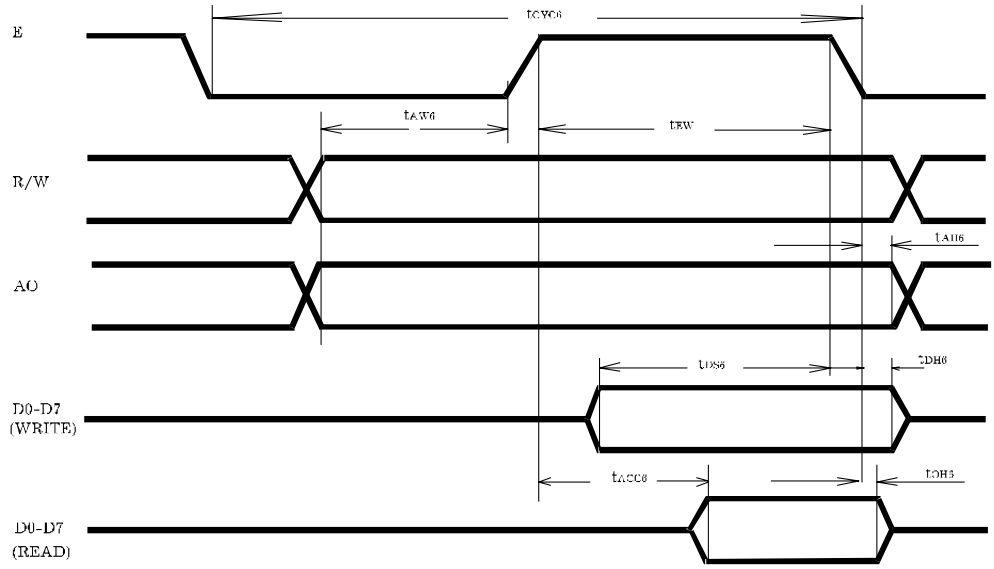
Notes: 1. The listed input t_{FDR} applies to IZ1520 and IZ1521 in slave mode.
2. The listed input t_{FDR} applies to IZ1520 and IZ1521 in master mode.

• TIMING CHART

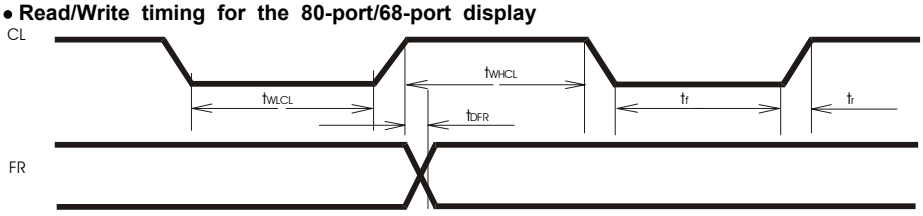
• Read/Write timing for the 80-port MPU



• Read/Write timing for the 68-port MPU



• Read/Write timing for the 80-port/68-port display



INTEGRAL

TERMINAL DESCRIPTION

Terminal Name	Function
D0 ÷ D7	Data I/O
A0	Select display data or functions. HIGH: Display data LOW : Instructions
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU HIGH: 68-port MPU interface LOW : 80-port MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only.
OSC1	Chip Select input LOW : Active level sensing
E (RD)	Read/Write Enable signal when a 68-port MPU is connected. (Active LOW Read Enable signal when an 80-port MPU is connected)
R/W $\overline{(WR)}$	Read/Write Select signal when a 68-port MPU is connected. HIGH: Read Select LOW : Write Select (Active LOW Write Enable input when an 80-port MPU is connected Rising edge sensing)
$\overline{CL}$	Input. Effective for an external clock operation model only.
OSC2	External clock input (only effective with external clock types)
FR	LCD Frame (AC- conversion) signal input/output
SEGn	Segment output for driving the LCD
COMn	Common output for driving the LCD
M/S	Master/Slave Select signal
V_{DD}	5V power supply
V_{SS}	0V power supply (GND level)
V_1, V_2, V_3, V_4, V_5	Power supplies for driving the LCD. $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

DISPLAY COMMANDS

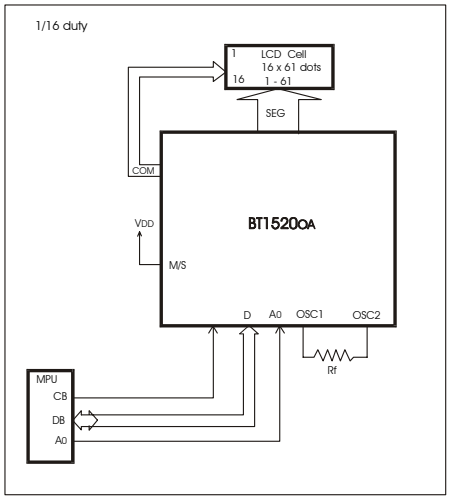
(Based on the 80-port MPU; the RD and WR commands differ for the 68-port MPU)

	Command	RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Function
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	Switches the entire display ON or OFF regardless of the Display RAM's data or the internal status. *Note
2	Display START Line	1	0	0	1	1	0	Display START address (0 ÷ 31)					Determines the line of RAM data to be displayed at the display's top line (COM0)
3	Page Address Set	1	0	0	1	0	1	1	1	0	Page		Sets the page of the Display RAM in the page address register
4	Column (Segment) Address Set	1	0	0	0	Column address (0 ÷ 79)							Sets the column address of the Display RAM in the column address register
5	Status Read	0	1	0	BUSY	ACC	ON/OFF	RESET	0	0	0	0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6	Write Display Data	1	0	1	Write Data								Writes the data on the data bus to RAM These commands access a previously specified address
7	Read Display Data	0	1	1	Read Data								Reads data from the Display RAM onto the data bus of the Display RAM, after which the column address is incremented one
8	ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse)
9	Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects normal display operation or static all-fit drive display operation 1: Static drive (Power Save) 0: Normal display
10	Duty Select	1	0	0	1	0	1	0	1	0	0	0/1	Selects the duty factor for driving LCD cells 1: 1/32 duty 0: 1/16 duty
11	Read Modify Write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counter by one only when display data is written but not when it is read
12	End	1	0	0	1	1	1	0	1	1	1	0	Cancels the Ready Modify Write mode
13	Reset	1	0	0	1	1	1	0	0	0	1	0	Resets the Display START line to the 1-st line in the register. Resets the column address counter and page address register to 0.

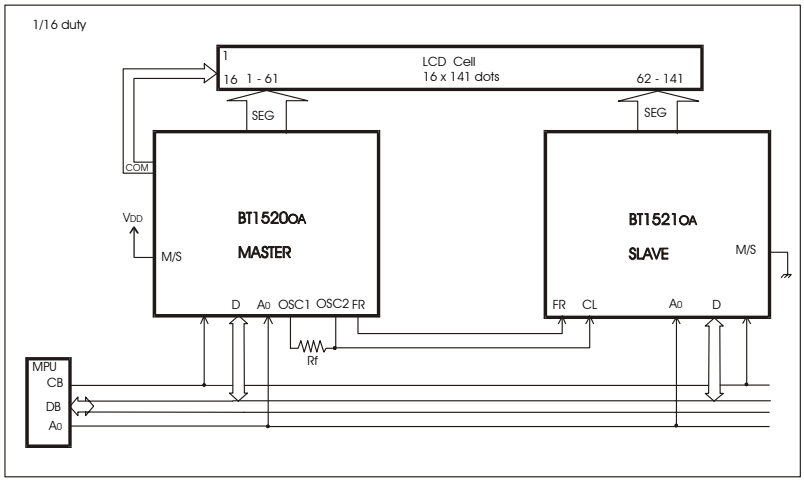
Note: Power Save mode is entered by selecting static drive in the Display OFF status.

REFERENCE CIRCUITRY EXAMPLES

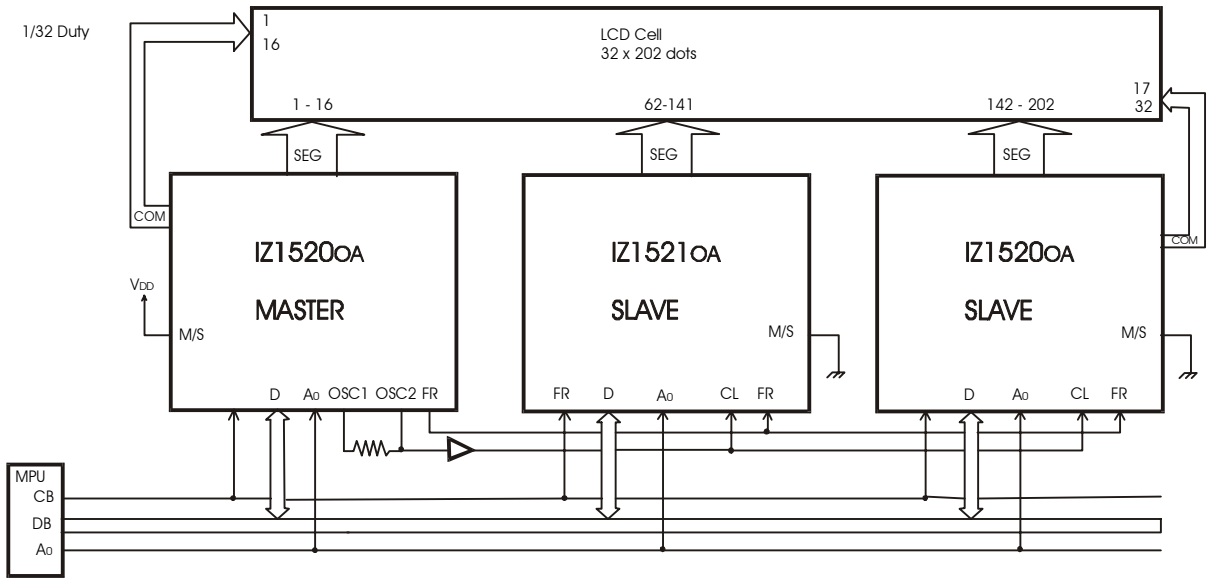
- **16 x 61 dots**



- **16 x 141 dots**

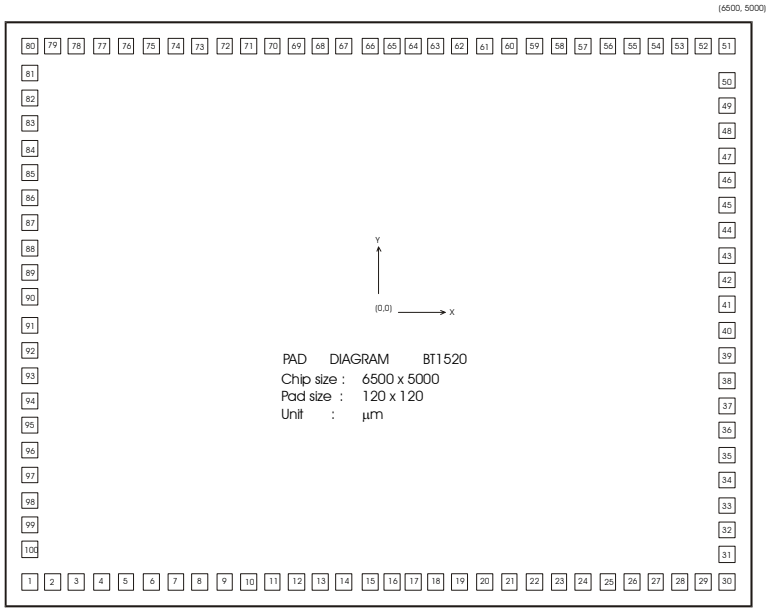


- **32 x 202 dots**



Note: If a system has two or more slave drivers a CMOS buffer will be required for clock signal.

PAD LAYOUT

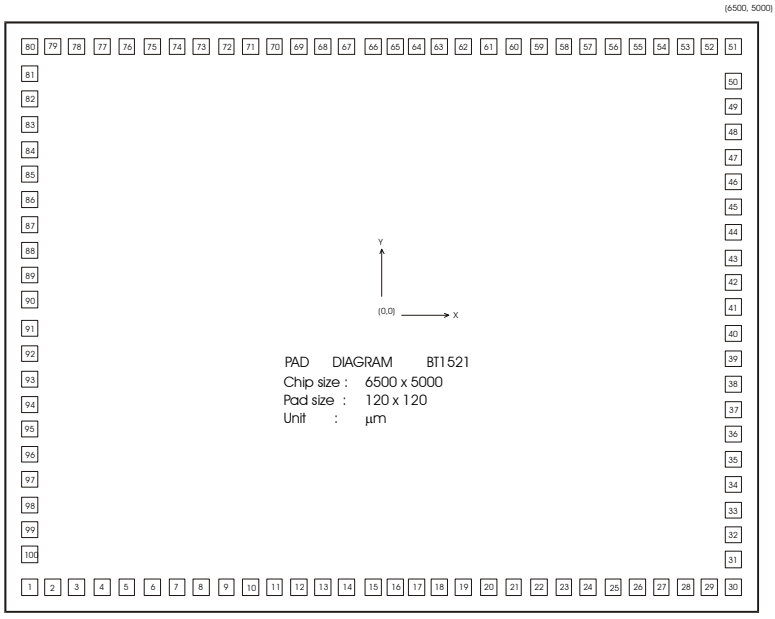


PAD LOCATION (Unit: μm)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM5	-2994	-2243	35	SEG37	3010	-1100	69	SEG3	-650	2242
2	COM6	-2717	-2244	36	SEG36	3010	-892	70	SEG2	-798	2242
3	COM7	-2510	-2244	37	SEG35	3010	-722	71	SEG1	-968	2242
4	COM8	-2302	-2244	38	SEG34	3010	-515	72	SEG0	-1177	2242
5	COM9	-2132	-2244	39	SEG33	3010	-344	73	A0	-1368	2242
6	COM10	-1924	-2244	40	SEG32	3010	-136	74	OSC1 [CS]	-1569	2242
7	COM11	-1754	-2244	41	SEG31	3010	33	75	OSC2 [CL]	-1761	2242
8	COM12	-1547	-2244	42	SEG30	3010	241	76	E [RD]	-1953	2242
9	COM13	-1377	-2244	43	SEG29	3010	412	77	R/W (WR)	-2142	2242
10	COM14	-1167	-2244	44	SEG28	3010	620	78	GND	-2348	2242
11	COM15	-998	-2244	45	SEG27	3010	790	79	DB0	-2646	2242
12	SEG60	-790	-2244	46	SEG26	3010	998	80	DB1	-3009	2242
13	SEG59	-620	-2244	47	SEG25	3010	1170	81	DB2	-3009	1895
14	SEG58	-413	-2244	48	SEG24	3010	1376	82	DB3	-3009	1695
15	SEG57	-242	-2244	49	SEG23	3010	1544	83	DB4	-3009	1497
16	SEG56	-35	-2244	50	SEG22	3010	1754	84	DB5	-3009	1297
17	SEG55	135	-2244	51	SEG21	3010	2242	85	DB6	-3009	1097
18	SEG54	344	-2244	52	SEG20	1494	2242	86	DB7	-3009	916
19	SEG53	514	-2244	53	SEG19	2434	2242	87	V_{CC}	-3009	737
20	SEG52	722	-2244	54	SEG18	2226	2242	88	RES	-3009	542
21	SEG51	892	-2244	55	SEG17	2056	2242	89	FR	-3009	342
22	SEG50	1100	-2244	56	SEG16	1848	2242	90	V5	-3009	162
23	SEG49	1270	-2244	57	SEG15	1678	2242	91	V3	-3009	-18
24	SEG48	1478	-2244	58	SEG14	1470	2242	92	V2	-3009	-198
25	SEG47	1607	-2244	59	SEG13	1300	2242	93	M/S	-3009	-398
26	SEG46	1856	-2244	60	SEG12	1012	2242	94	V4	-3009	-603
27	SEG45	2026	-2244	61	SEG11	922	2242	95	V1	-3009	-806
28	SEG44	2234	-2244	62	SEG10	714	2242	96	COM0	-2994	-996
29	SEG43	2477	-2244	63	SEG9	544	2242	97	COM1	-2994	-1166
30	SEG42	3020	-2244	64	SEG8	336	2242	98	COM2	-2994	-1375
31	SEG41	3010	-1857	65	SEG7	166	2242	99	COM3	-2994	-1544
32	SEG40	3010	-1648	66	SEG6	-42	2242	100	COM4	-2994	-1753
33	SEG39	3010	-1474	67	SEG5	-213	2242				
34	SEG38	3010	-1270	68	SEG4	-420	2242				

Note: Pads 74,75 are OSC1, OSC2 for $BT5150_{OA}$ and CS, CL for $IZ1520_{AA}$ respectively. All other pad names are identical.

PAD LAYOUT



PAD LOCATION (Unit: μm)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG71	-2994	-2243	35	SEG37	3010	-1100	69	SEG3	-650	2242
2	SEG70	-2717	-2244	36	SEG36	3010	-892	70	SEG2	-798	2242
3	SEG69	-2510	-2244	37	SEG35	3010	-722	71	SEG1	-968	2242
4	SEG68	-2302	-2244	38	SEG34	3010	-515	72	SEG0	-1177	2242
5	SEG67	-2132	-2244	39	SEG33	3010	-344	73	A0	-1368	2242
6	SEG66	-1924	-2244	40	SEG32	3010	-136	74	$\overline{CS}$	-1569	2242
7	SEG65	-1754	-2244	41	SEG31	3010	33	75	CL	-1761	2242
8	SEG64	-1547	-2244	42	SEG30	3010	241	76	E RD	-1953	2242
9	SEG63	-1377	-2244	43	SEG29	3010	412	77	R/W (WR)	-2142	2242
10	SEG62	-1167	-2244	44	SEG28	3010	620	78	GND	-2348	2242
11	SEG61	-998	-2244	45	SEG27	3010	790	79	DB0	-2646	2242
12	SEG60	-790	-2244	46	SEG26	3010	998	80	DB1	-3009	2242
13	SEG59	-620	-2244	47	SEG25	3010	1170	81	DB2	-3009	1895
14	SEG58	-413	-2244	48	SEG24	3010	1376	82	DB3	-3009	1695
15	SEG57	-242	-2244	49	SEG23	3010	1544	83	DB4	-3009	1497
16	SEG56	-35	-2244	50	SEG22	3010	1754	84	DB5	-3009	1297
17	SEG55	135	-2244	51	SEG21	3010	2242	85	DB6	-3009	1097
18	SEG54	344	-2244	52	SEG20	1494	2242	86	DB7	-3009	916
19	SEG53	514	-2244	53	SEG19	2434	2242	87	V_{CC}	-3009	737
20	SEG52	722	-2244	54	SEG18	2226	2242	88	RES	-3009	542
21	SEG51	892	-2244	55	SEG17	2056	2242	89	FR	-3009	342
22	SEG50	1100	-2244	56	SEG16	1848	2242	90	V5	-3009	162
23	SEG49	1270	-2244	57	SEG15	1678	2242	91	V3	-3009	-18
24	SEG48	1478	-2244	58	SEG14	1470	2242	92	V2	-3009	-198
25	SEG47	1607	-2244	59	SEG13	1300	2242	93	SEG79	-3009	-398
26	SEG46	1856	-2244	60	SEG12	1012	2242	94	SEG78	-3009	-603
27	SEG45	2026	-2244	61	SEG11	922	2242	95	SEG77	-3009	-806
28	SEG44	2234	-2244	62	SEG10	714	2242	96	SEG76	-2994	-996
29	SEG43	2477	-2244	63	SEG9	544	2242	97	SEG75	-2994	-1166
30	SEG42	3020	-2244	64	SEG8	336	2242	98	SEG74	-2994	-1375
31	SEG41	3010	-1857	65	SEG7	166	2242	99	SEG73	-2994	-1544
32	SEG40	3010	-1648	66	SEG6	-42	2242	100	SEG72	-2994	-1753
33	SEG39	3010	-1474	67	SEG5	-213	2242				
34	SEG38	3010	-1270	68	SEG4	-420	2242				