

Low Voltage SPDT Analog Switch 2:1 Mux/Demux Bus Switch

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 8Ω at 3.0V
- Wide VCC Range: 1.65V to 5.5V
- Rail-to-Rail Signal Range
- Control Input Overvoltage Tolerance: 5.5V
- Fast Transition Speed: 2ns at 5.0V
- High Off Isolation: -63dB @ 10MHz
- Break-Before-Make Switching
- High Bandwidth: 350MHz
- Extended Industrial Temperature Range: -40°C to 85°C
- PI5A3157B Is Improved Direct Replacement for NC7SB3157
- Packaging (Pb-free & Green):
 - 6-pin UDFN 1mm×1mm
 - 6-pin SC70

Description

The PI5A3157B is a high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, 1.65V to 5.5V, the PI5A3157B has a maximum ON resistance of 12-ohms at 1.65V, 9-ohms at 2.3V & 6-ohms at 4.5V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

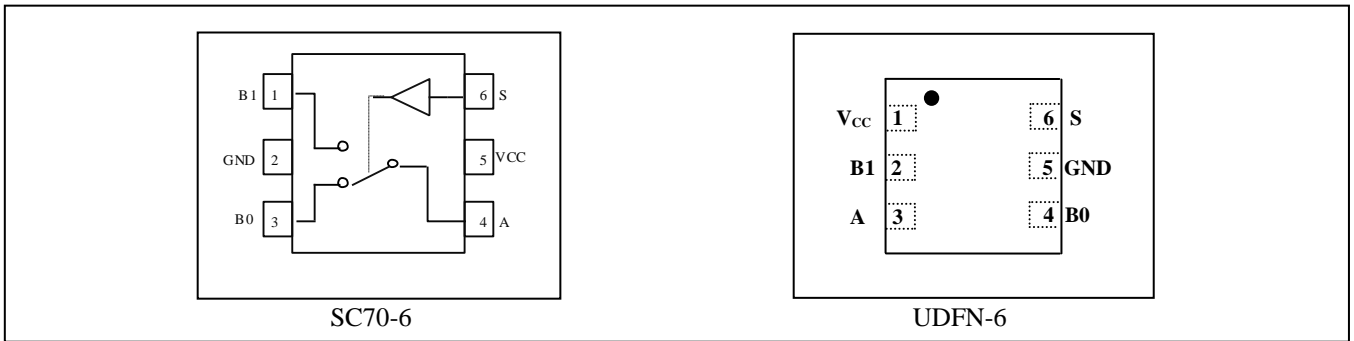
The control input, S, is independent of supply voltage.

PI5A3157B is an improved direct replacement for the NC7SB3157.

Application

- Cell Phones
- PDAs
- MP3 Players
- Portable Instrumentation
- Battery powered Communications
- Computer Peripherals

Pin Assignment



Pin Description

Pin No		Pin Name	Description
SC70-6	UDFN-6		
1	2	B1	Data Port
2	5	GND	Ground
3	4	B0	Data Port (Normally connected)
4	3	A	Common Output/Data Port
5	1	V _{CC}	Positive Power Supply
6	6	S	Logic control

Logic Function Table

Logic Inputs(S)	Function
0	B ₀ connect to A
1	B ₁ connect to A

Maximum Ratings

Storage Temperature.....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage V_{CC}	-0.5V to +7.0V
DC Control Input Voltage V_S	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to $V_{CC} + 0.5V$
DC Output Current V_{OUT}	128mA
DC V_{CC} or Ground Current I_{CC} / I_{GND}	$\pm 100mA$
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (TL) (Soldering, 10 seconds)	260°C
Power Dissipation (Pd) @ +85°C	180mW
ESD(HBM).....	2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	1.65	-	5.5	V
V_S	Control Input Voltage	-	0	-	5.5	V
V_{IN}	Switch Input Voltage	-	0	-	V_{CC}	V
V_{OUT}	Output Voltage	-	0	-	V_{CC}	V
T_A	Operating Temperature	-	-40	25	85	°C
T_s						
tr, tf	Input Rise and Fall Time	Control Input $V_{CC} = 2.3V$ to $3.6V$	0	-	10	ns/V
		Control Input $V_{CC} = 4.5V$ to $5.5V$	0	-	5	ns/V

Note: Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics ($T_A = -40^\circ\text{C}$ to 85°C , unless otherwise noted.)

Parameter	Description	Test Conditions	Temperature (T_A : $^\circ\text{C}$)	Min.	Typ.	Max.	Units
V_{IAR}	Analog Input Signal Range	V_{CC}	-40°C to 85°C	0	-	V_{CC}	V
R_{ON}	ON Resistance ⁽¹⁾	$V_{CC}=4.5\text{V}, I_O = 30\text{mA}, V_{IN} = 0\text{V}$	25°C	-	4	6	Ω
		$V_{CC}=4.5\text{V}, I_O = -30\text{mA}, V_{IN} = 2.4\text{V}$		-	5	8	
		$V_{CC}=4.5\text{V}, I_O = -30\text{mA}, V_{IN} = 4.5\text{V}$		-	7	11	
		$V_{CC}=4.5\text{V}, I_O = 30\text{mA}, V_{IN} = 0\text{V}$	-40°C to 85°C	-	-	6	
		$V_{CC}=4.5\text{V}, I_O = -30\text{mA}, V_{IN} = 2.4\text{V}$		-	-	8	
		$V_{CC}=4.5\text{V}, I_O = -30\text{mA}, V_{IN} = 4.5\text{V}$		-	-	11	
		$V_{CC}=3.0\text{V}, I_O = 24\text{mA}, V_{IN} = 0\text{V}$	25°C	-	5	8	
		$V_{CC}=3.0\text{V}, I_O = -24\text{mA}, V_{IN} = 3.0\text{V}$		-	10	15	
		$V_{CC}=3.0\text{V}, I_O = 24\text{mA}, V_{IN} = 0\text{V}$		-	-	8	
		$V_{CC}=3.0\text{V}, I_O = -24\text{mA}, V_{IN} = 3.0\text{V}$	-40°C to 85°C	-	-	15	
		$V_{CC}=2.3\text{V}, I_O = 8\text{mA}, V_{IN} = 0\text{V}$		-	6	9	
		$V_{CC}=2.3\text{V}, I_O = -8\text{mA}, V_{IN} = 2.3\text{V}$		-	13	20	
		$V_{CC}=2.3\text{V}, I_O = 8\text{mA}, V_{IN} = 0\text{V}$	-40°C to 85°C	-	-	9	
		$V_{CC}=2.3\text{V}, I_O = -8\text{mA}, V_{IN} = 2.3\text{V}$		-	-	20	
		$V_{CC}=1.65\text{V}, I_O = 4\text{mA}, V_{IN} = 0\text{V}$		-	8	12	
		$V_{CC}=1.65\text{V}, I_O = -4\text{mA}, V_{IN} = 1.65\text{V}$	25°C	-	20	30	
$V_{CC}=1.65\text{V}, I_O = 4\text{mA}, V_{IN} = 0\text{V}$	-	-		12			
$V_{CC}=1.65\text{V}, I_O = -4\text{mA}, V_{IN} = 1.65\text{V}$	-	-		25			
ΔR_{ON}	ON Resistance Match Between Channels ^(1,2,3)	$V_{CC}=4.5\text{V}, I_A = -30\text{mA}, V_{IN} = 3.15\text{V}$	25°C	-	0.15	-	Ω
		$V_{CC}=3.0\text{V}, I_A = -24\text{mA}, V_{IN} = 2.1\text{V}$		-	0.2	-	
		$V_{CC}=2.3\text{V}, I_A = -8\text{mA}, V_{IN} = 1.6\text{V}$		-	0.3	-	
		$V_{CC}=1.65\text{V}, I_A = -4\text{mA}, V_{IN} = 0\text{V}$		-	0.5	-	
R_{ONF}	ON Resistance Flatness ^(1,2,4)	$V_{CC}=5.0\text{V}, I_A = -30\text{mA}, 0 \leq V_{IN} \leq V_{CC}$	25°C	-	6	-	Ω
		$V_{CC}=3.3\text{V}, I_A = -24\text{mA}, 0 \leq V_{IN} \leq V_{CC}$		-	12	-	
		$V_{CC}=2.5\text{V}, I_A = -8\text{mA}, 0 \leq V_{IN} \leq V_{CC}$		-	22	-	
		$V_{CC}=1.8\text{V}, I_A = -4\text{mA}, 0 \leq V_{IN} \leq V_{CC}$		-	90	-	
V_{IH}	Input High Voltage (Logic High Level)	$V_{CC}=1.65\text{V}$	-40°C to 85°C	1	-	-	V
		$V_{CC} = 2.3\text{V}$		1.2	-	-	
		$V_{CC} = 3\text{V}$		1.3	-	-	
		$V_{CC} = 4.2\text{V}$		1.5	-	-	
		$V_{CC} = 5.5\text{V}$		1.8	-	-	
V_{IL}	Input Low Voltage (Logic Low Level)	$V_{CC}=1.65\text{V}$	-40°C to 85°C	-	-	0.4	V
		$V_{CC} = 2.3\text{V}$		-	-	0.6	
		$V_{CC} = 3\text{V}$		-	-	0.8	
		$V_{CC} = 4.2\text{V}$		-	-	1	
		$V_{CC} = 5.5\text{V}$		-	-	1.2	
I_{LKC}	Input Leakage Current	$0 \leq V_{IN} \leq 5.5\text{V}, V_{CC} = 0\text{V}$ to 5.5V	25°C	-	-	± 0.1	μA
			-40°C to 85°C	-	-	± 1.0	
I_{OFF}	OFF State Leakage Current	$0 \leq V_{IN} \leq 5.5\text{V}, V_{CC} = 1.65\text{V}$ to 5.5V	25°C	-	-	± 0.1	μA
			-40°C to 85°C	-	-	± 10	
I_{CC}	Quiescent Supply Current	All channels ON or OFF, $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0, V_{CC} = 5.5\text{V}$	25°C	-	-	1	μA
			-40°C to 85°C	-	-	5	

Notes:

- Measured by voltage drop between A and B pins at the indicated current through the device. ON resistance is determined by the lower of the voltages on two ports (A or B).
- Parameter is characterized but not tested in production.
- $\Delta R_{ON} = R_{ON} \text{ max} - R_{ON} \text{ min}$, measured at identical V_{CC} , temperature and voltage levels.
- Flatness is defined as difference between maximum and minimum value of ON resistance over the specified range of conditions. Guaranteed by design.

Capacitance⁽¹⁾ ($T_A = 25^\circ\text{C}$, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Control Input	$V_{CC} = 5.0\text{V}$, $f = 1\text{ MHz}$ ⁽¹⁾	-	2.5	-	pF
C_{IO-B}	For B Port, Switch OFF		-	5.0	-	
C_{IOA-ON}	For A Port, Switch ON		-	15.0	-	

Notes:

1. Capacitance is characterized but not tested in production

Switch and AC Characteristics⁽¹⁾

Parameter	Description	Test Conditions	Supply Voltage	Temperature ($T_A: ^\circ\text{C}$)	Min	Typ	Max	Units
t_{PLH} t_{PHL}	Propagation Delay: A to Bn	See test circuit diagrams 1 and 2. V_I Open ⁽²⁾	$V_{CC} = 1.65\text{V to } 1.95\text{V}$ $V_{CC} = 2.3\text{V to } 2.7\text{V}$ $V_{CC} = 3.0\text{V to } 3.6\text{V}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$	-40 to 85 $^\circ\text{C}$	-	-	3.5	ns
					-	-	1.1	
					-	-	0.9	
					-	-	0.6	
t_{PZL} t_{PZH}	Output Enable Turn ON Time: A to Bn	See test circuit diagrams 1 & 2. $V_I = 2V_{CC}$ for t_{PZL} , $V_I = 0\text{V}$ for t_{PZH}	$V_{CC} = 1.65\text{V to } 1.95\text{V}$ $V_{CC} = 2.3\text{V to } 2.7\text{V}$ $V_{CC} = 3.0\text{V to } 3.6\text{V}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$	-40 to 85 $^\circ\text{C}$	6	-	13	
					3.5	-	8.0	
					2.5	-	6.9	
					1.7	-	5.2	
t_{PLZ} t_{PHZ}	Output Disable Turn OFF Time: A to Bn	See test circuit diagrams 1 and 2. $V_I = 2V_{CC}$ for t_{PLZ} , $V_I = 0\text{V}$ for t_{PHZ}	$V_{CC} = 1.65\text{V to } 1.95\text{V}$ $V_{CC} = 2.3\text{V to } 2.7\text{V}$ $V_{CC} = 3.0\text{V to } 3.6\text{V}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$	-40 to 85 $^\circ\text{C}$	3	-	13	
					2	-	9	
					1.5	-	7.0	
					0.8	-	4.5	
t_{BM}	Break Before Make Time	See test circuit diagram 3.	$V_{CC} = 1.65\text{V to } 1.95\text{V}$ $V_{CC} = 2.3\text{V to } 2.7\text{V}$ $V_{CC} = 3.0\text{V to } 3.6\text{V}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$	-40 to 85 $^\circ\text{C}$	-	3.7	-	
					-	2.5	-	
					-	2.5	-	
					-	1.6	-	
Q	Charge Injection	$C_L = 0.1\text{nF}$, $V_{GEN} = 0\text{V}$, $R_{GEN} = 0\Omega$. See test circuit 4	$V_{CC} = 5.0\text{V}$ $V_{CC} = 3.3\text{V}$	25 $^\circ\text{C}$	-	5	-	pC
OIRR	Off Isolation	$R_L = 50\Omega$, $V_{GEN} = 0\text{V}$, $R_{GEN} = 0\Omega$, $f = 10\text{MHz}$. ⁽³⁾ See test circuit 5	$V_{CC} = 1.65\text{V to } 5.5\text{V}$	25 $^\circ\text{C}$	-	-63	-	dB
X_{TALK}	Crosstalk Isolation	See test circuit 6 ⁽⁴⁾	$V_{CC} = 1.65\text{V to } 5.5\text{V}$	25 $^\circ\text{C}$	-	-64	-	
f _{3dB}	-3dB Bandwidth	See test circuit 9	$V_{CC} = 1.65\text{V to } 5.5\text{V}$	25 $^\circ\text{C}$	-	350	-	MHz
T_{HD}	Total Harmonic Distortion	$R_L = 600\Omega$, $V_{IN} = 0.5\text{Vpp}$, $f = 20\text{Hz to } 20\text{kHz}$	$V_{CC} = 1.65\text{V to } 5.5\text{V}$	25 $^\circ\text{C}$	-	0.012	-	%

Notes:

- Guaranteed by design.
- The device contributes no other propagation delay other than the RC delay of the switch ON resistance and the 50pF load capacitance, when driven by an ideal voltage source with zero output impedance.
- Off Isolation = $20 \text{ Log}_{10} [V_{Bn}/V_A]$ and is measured in dB.
- Crosstalk Isolation = $20 \text{ Log}_{10} [V_{B1}/V_{B0}]$ and is measured in dB.

Test Circuits and Timing Diagrams

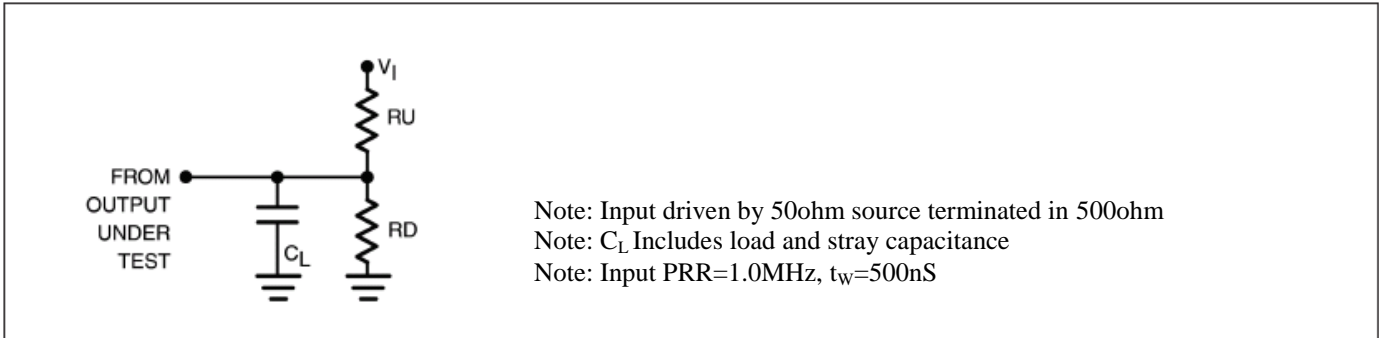


Figure 1. AC Test Circuit

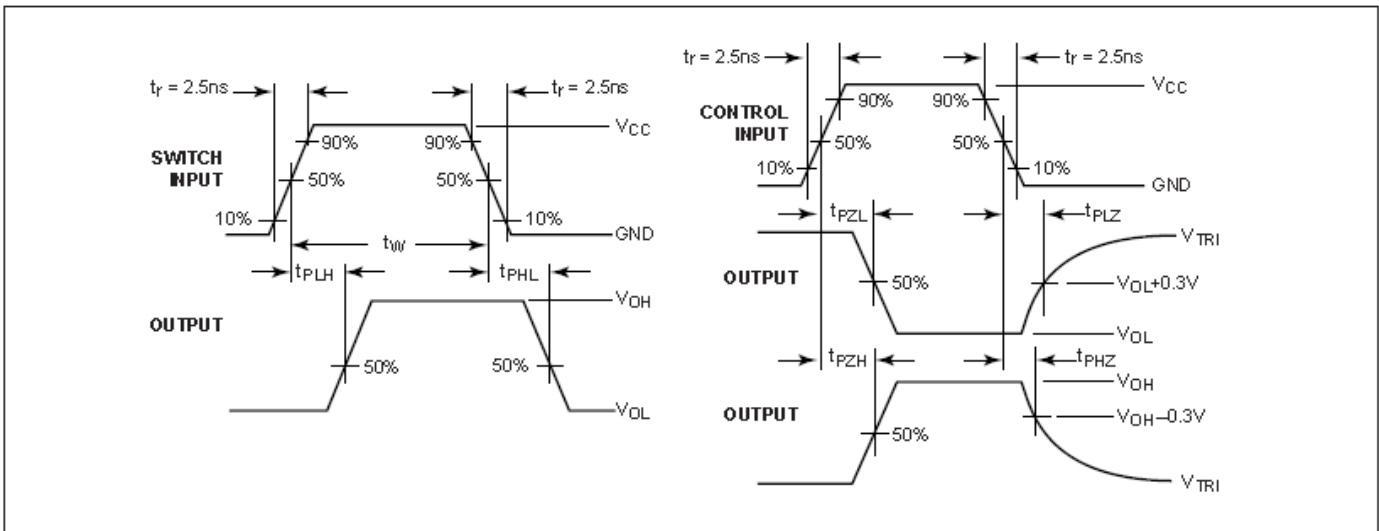


Figure 2. AC Waveforms

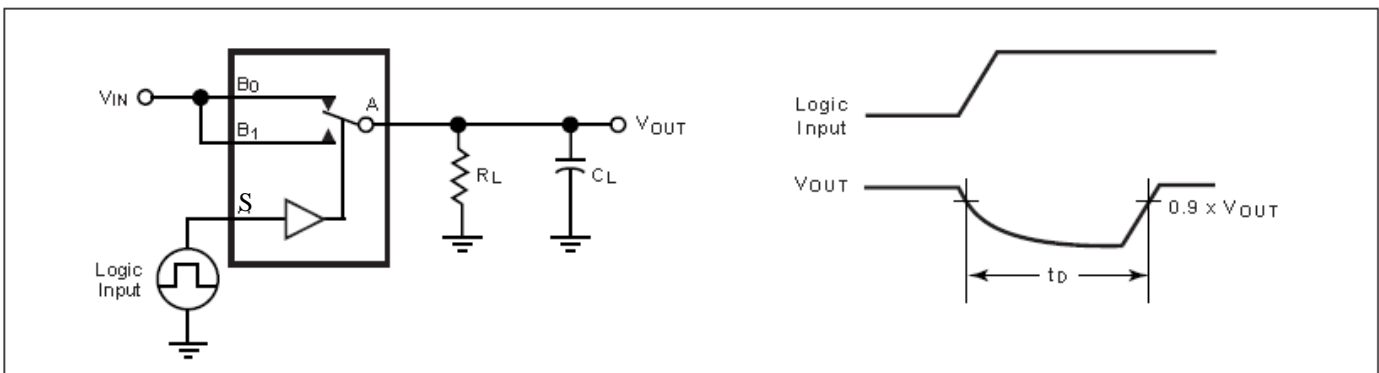


Figure 3. Break Before Make Interval Timing

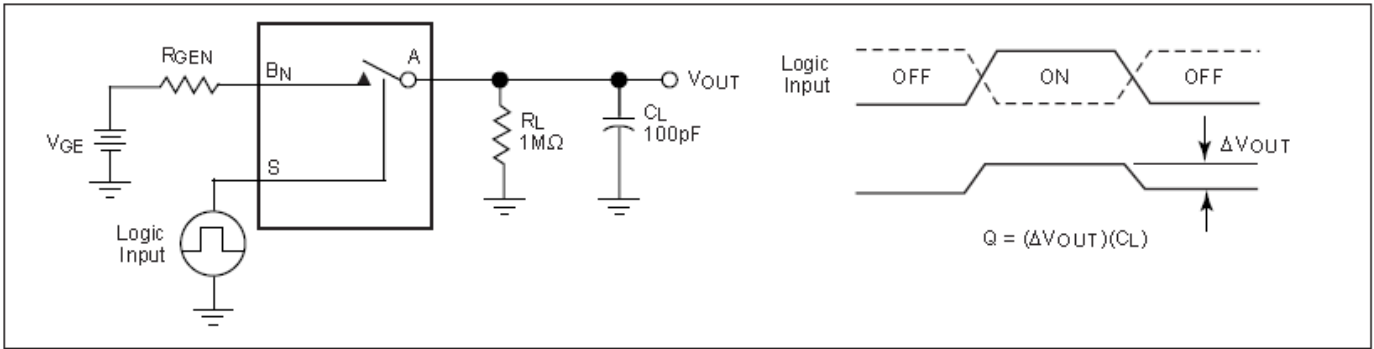


Figure 4. Charge Injection Test

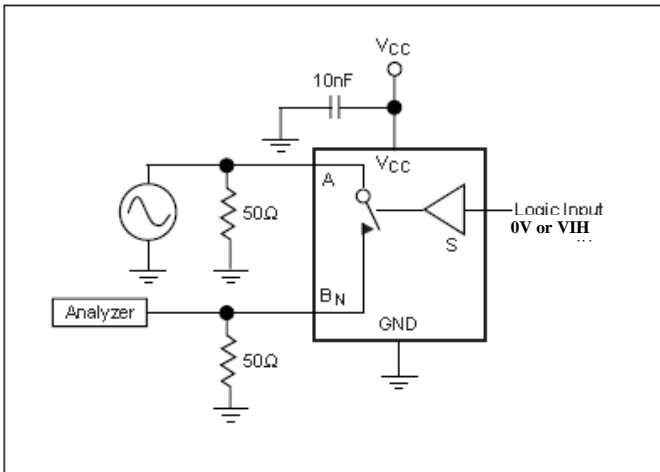


Figure 5. Off Isolation

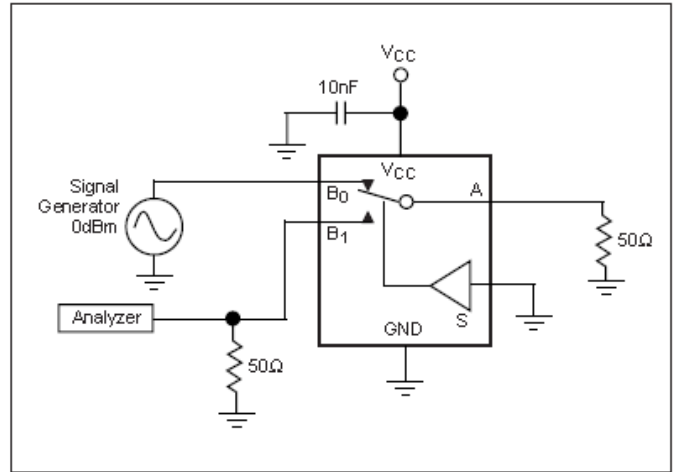


Figure 6. Crosstalk

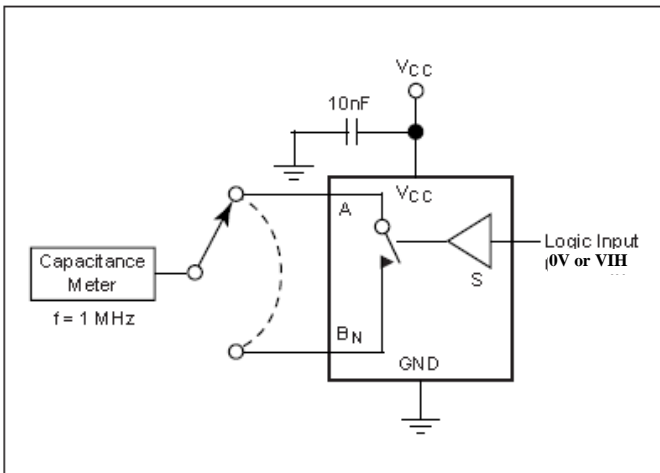


Figure 7. Channel Off Capacitance

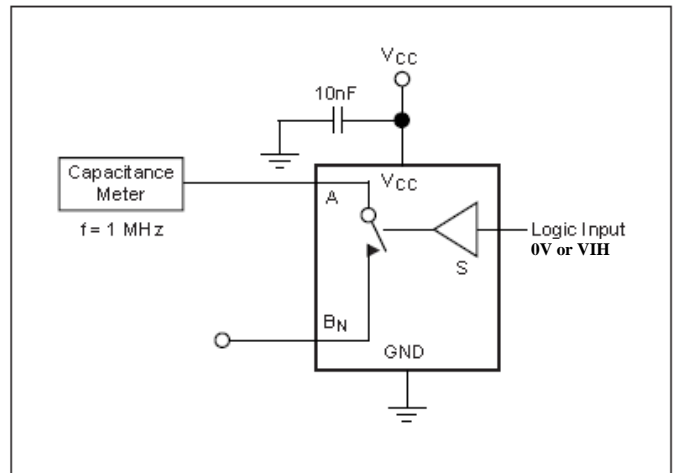


Figure 8. Channel On Capacitance

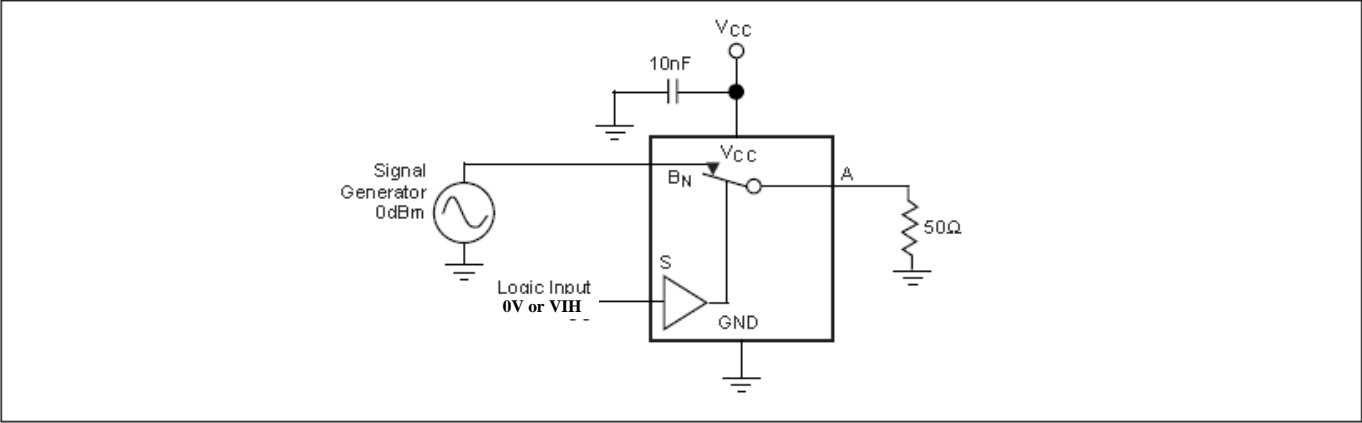


Figure 9. Bandwidth

**Mechanical Information:
6-UDFN (ZU)**

TOP VIEW

BOTTOM VIEW

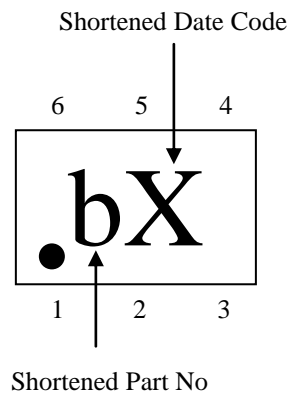
SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.50	0.60
A1	0.00	0.05
A3	0.15 REF	
D	0.95	1.05
E	0.95	1.05
b	0.10	0.20
L	0.30	0.50
e	0.35 BSC	

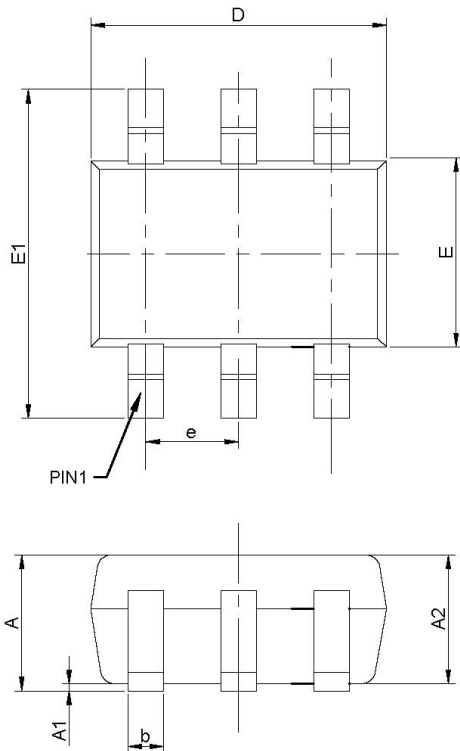
Note:
1. Ref: JEDEC MO-287A

PERICOM Enabling Serial Connectivity		DATE: 06/18/13
DESCRIPTION: 6-Pin, UDFN, 1X1		
PACKAGE CODE: ZU (ZU6)		
DOCUMENT CONTROL #: PD-2152	REVISION: --	

Marking Description



6-SC70 (C6)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.15	0.40
c	0.08	0.22
D	1.80	2.20
E	1.10	1.40
E1	1.80	2.40
e	0.65 BSC	
L	0.26	0.46
θ	0°	8°

Notes:

1. Comply with MO-203C/AB, except b Max, D Min and D Max.
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR



DATE: 03/29/16

DESCRIPTION: 6-Pin, SOT363 (SC70)

PACKAGE CODE: C (C6)

DOCUMENT CONTROL#: PD-1902

REVISION: B

16-0078

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Part Number	Package Code	Package	Top Marking
PI5A3157BZUEX	ZU	6-Pin, 1x1 (UDFN)	b
PI5A3157BC6EX	C6	6-Pin, SOT363 (SC70)	kD

Notes:

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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