MUAA Routing CoProcessor (RCP) Family

APPLICATION BENEFITS

- High performance MAC Address processor for multiport switches and routers (Up to 48 10/100 or 4 Gigabit Ethernet at wire speed)
- Layer 4 flow recognition for Quality of Service up to 16.7 million packets per second
- ARP Cache manager/IP address caching at 12.5 million packets per second
- Synchronous interfaces and programmable priority between ports for simplicity of design
- Learn, age, and auto-age functions with “virtual queues,” keeping track of aged and learned entries
- Transparent cascade of up to four 2K devices without external logic, software setup, or performance hit

DISTINCTIVE CHARACTERISTICS

- 2K and 8K x 80-bit partitionable CAM/RAM data field in address database
- 32-bit synchronous port with separate inputs and outputs; optional 16-bit configuration
- 32-bit bi-directional processor port; optional 16-bit configuration
- Pipelined operation
- Operations performed from the synchronous port or processor port; all flags independently available to both ports
- 9-bit internal time stamp
- 50 MHz clock
- 388-pin PBGA (8K) and 160-pin PQFP (2K) packages.
- 3.3 Volt core with 3.3 Volt/5 Volt tolerant IO buffers.
- IEEE 1149.1 (JTAG) compliant

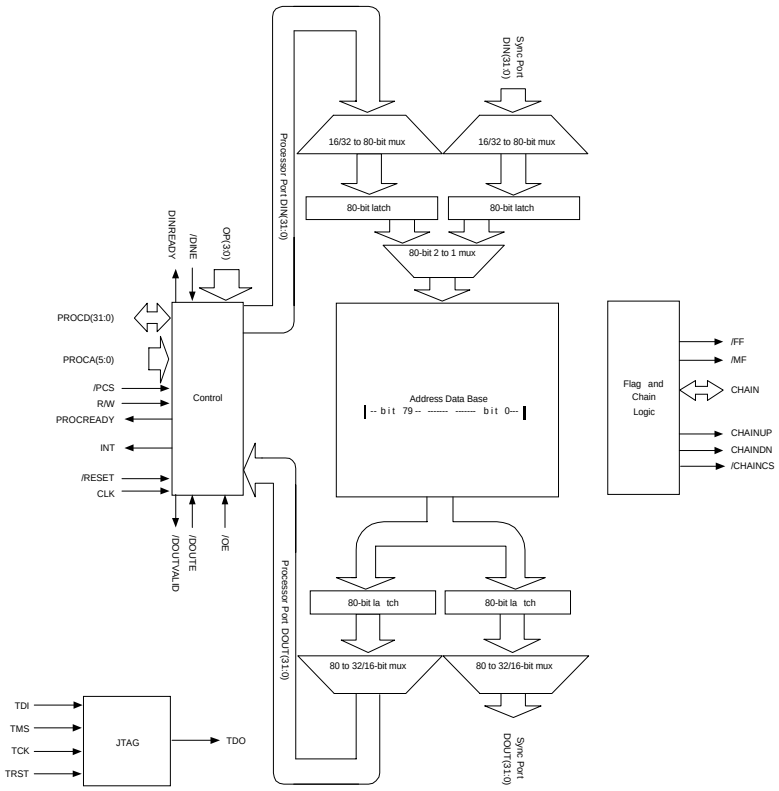


Figure 1: Block Diagram

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GENERAL DESCRIPTION

The MUSIC MUAA Routing CoProcessor (RCP) family consists of 80-bit wide content-addressable memories (CAMs), available in depths of 2K and 8K words. The CAM/RAM associated data partition is programmable from 32 bits of CAM and 48 bits of associated data, to 80 bits of CAM and 0 bits of RAM. The MUAA RCP can perform normal routing functions such as search, insert, and delete on single entries and can age multiple entries simultaneously. In addition, there is a learn instruction, particularly useful in networking applications. For maximum flexibility all the operations may be performed either through the processor port or through the synchronous port. Operations may occur on both ports simultaneously; the port with the highest priority will gain access first if both ports require a read or write into the CAM array simultaneously.

The synchronous interface consists of 32-bit wide input and output ports, both of which may be configured as 16 bits. The data is multiplexed into and out of the CAM and RAM associated data field. Where input or output data is wider than the port, it is loaded or unloaded in multiple cycles starting with the least significant word. Internally the device is pipelined; once an operation is started on the synchronous port the next operation may be loaded and the results of the previous operation unloaded, thus maximizing device throughput.

Multiple 2K MUAA RCPs may be chained transparently to provide deeper memory. No software configuration is necessary. Each MUAA RCP detects where it is in the chain from the chaining pins on the previous device. A register is provided to inform the host of the total available CAM memory and the number of CAMs chained. All operations to the chained CAM are totally transparent. No individual device selection or addressing is required.

The MUSIC MUAA RCP has aging, auto-aging, and learning functions. All entries have a 9-bit time stamp and may be marked as static to prevent the aging function from deleting them. When auto aging is enabled it may be configured to have higher or lower priority access than the ports.

Two internal virtual queues of learned and aged entries are available. As entries are learned or aged out they are tagged as such and may be read from the device through either of the ports. This feature enables simple host management of aged out and learned entries.

IEEE Standard. 1149.1 (JTAG) testability is implemented providing BYPASS, SAMPLE/PRELOAD, EXTEST, CLAMP, and HIGH-Z functions.

PIN DESCRIPTIONS

Note: *Signal names that start with a slash ("/") are active LOW. All signals are 3.3 Volt CMOS level. All input and bi-directional pins are 5-Volt tolerant, except for CLK. Never leave inputs floating except where indicated. The CAM architecture draws large currents during search operations, mandating the use of good layout and bypassing techniques. Refer to the Electrical Characteristics section for more information.*

See Table 1 for the 388-pin balls and the Packages section for the chip illustrations.

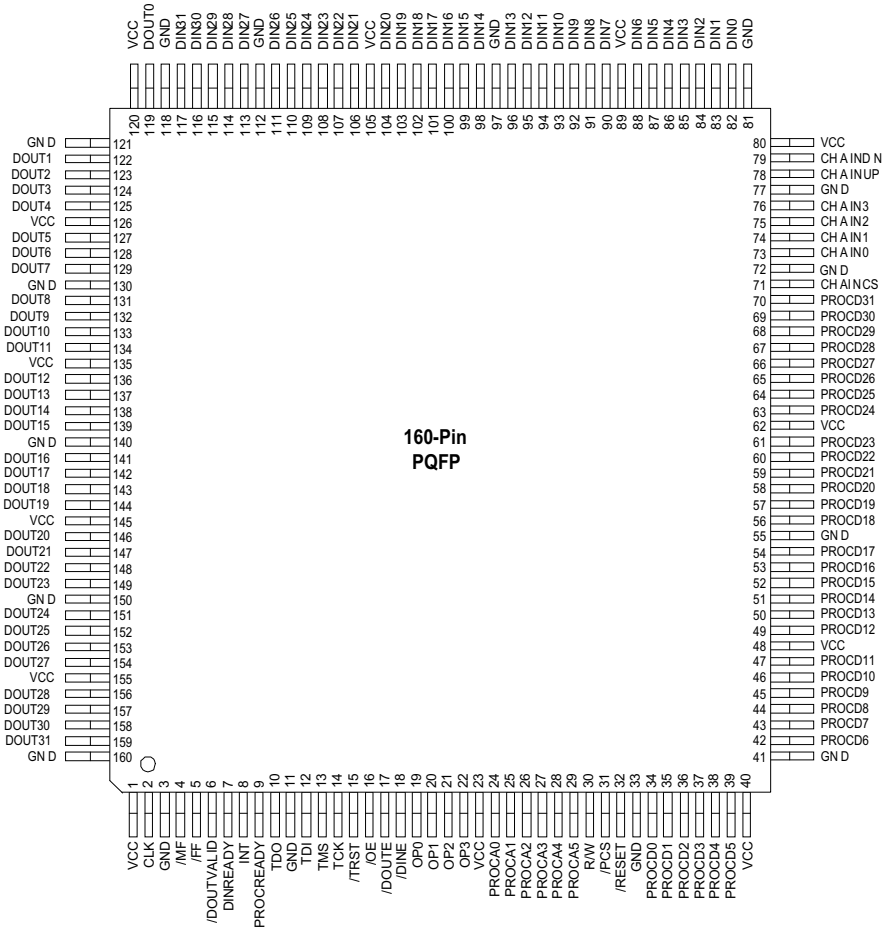


Figure 2: 160-Pin PQFP (Top View)

DIN[31:0] (Input)

DIN[31:0] are synchronous port data input pins. Data is loaded into the MUAA RCP right aligned, least significant word first.

/DINE (Input)

DIN is sampled by the rising edge of CLK when /DINE is asserted. Refer to Table 1 for slave connections.

OP[3:0] (Input)

OP[3:0] is a synchronous port operation to be performed on the data applied to the DIN pins. OP is sampled by the rising edge of CLK when /DINE is asserted. When loading the CAM/RAM words to DIN, OP is set to LOAD except for the last word. OP for the last word is set to the desired operation.

DINREADY (Output)

When DINREADY is HIGH, the synchronous port accepted the current operation. This is affected by the priority set for the DIN port and the processor port. Note, DINREADY may be LOW for up to 800 CLK periods after /RESET is taken HIGH. The JTAG interface is able to set DINREADY to HIGH-Z. Active HIGH.

DOUT[31:0] (3-State Output)

DOUT[31:0] is the synchronous port data output. Data is read out right aligned, least significant word first. The address index (bits 25–0), SWEX flag (bit 26), PWEX flag (bit 27), LQUEUE flag (bit 28), AQUEUE flag (bit 29), Sync Port Match flag (bit 30), and Full flag (bit 31) may also be read from this port before or after operation data depending on configuration.

/DOUTVALID (Output)

/DOUTVALID indicates when new data is available at the synchronous output port. /DOUTVALID is active LOW for one CLK cycle. /DOUTVALID may be configured to become active on the same clock as new DOUT becomes valid or the CLK before. The JTAG interface is able to set /DOUTVALID to HIGH-Z.

/OE (Input)

/OE is the DOUT High Impedance control.

/DOUTE (Input)

/DOUTE is the DOUT enable control. When the DOUT data word is configured to be wider than the output port then this strobe enables the next word(s) of the DOUT data onto the DOUT pins.

PROCD[31:0] (Bi-directional)

The bi-directional Processor data port provides the processor interface to the device. On write cycles all devices respond in parallel. On read cycles the appropriate device responds without additional intervention from the processor.

PROCA[5:0] (Input)

Processor port address bus. Selects which device register is accessed. Bit 0 is only used when the port is set to 16-bit mode, otherwise it should be held at a valid logic level.

R/W (Input)

R/W is the processor port read/write control pin. This pin is HIGH for reads, LOW for writes.

/PCS (Input)

/PCS is the processor port chip select pin. When LOW this pin indicates a cycle to the processor port. On write cycles data must be set up to the rising edge of /PCS. On read cycles /PCS controls the output enable of the PROCD bus. Note that /PCS may be asynchronous to CLK. Refer to Table 1 for slave connections.

PROCREADY (Output)

When PROCREADY is HIGH, indicates the processor read data is available or the processor write data is accepted. Priority may be set between the DIN port and the processor port. Note PROCREADY may be LOW for up to 800 CLK periods after /RESET is taken HIGH. The JTAG interface is able to set PROCREADY to HIGH-Z.

INT (Output)

INT interrupt. Indicates the aged or learned queue has at least one entry or a write exception occurred. The service routine should either check the AQUEUE, LQUEUE, and WEX registers, or bits 26–29 of the Address Index register, to determine the cause. The interrupt is cleared after the appropriate flag register has been read and will not be reasserted until either the queue(s) are emptied and then get at least one entry again, or another write exception occurs. The JTAG interface is able to set INT to HIGH-Z.

/RESET (Input)

The /RESET input is used to reset the MUAA RCP. /RESET must be asserted for at least 3 CLK periods.

CLK (Input)

The rising edge of CLK input is the device clock.

/FF (Full Flag, Output)

/FF is active when the device (or chain of devices) is full. /FF becomes inactive when any one device has two open entries. The JTAG interface is able to set /FF to HIGH-Z.

CHAIN[3:0 (Input)

When two or more devices are chained they communicate among themselves using the CHAIN[3:0] signals. See Chaining section. Internally Pulled-up. Refer to Table 1 for slave connections.

CHAINUP (Output)

When two or more devices are chained they communicate among themselves using the CHAINUP signals. See Chaining section. The JTAG interface is able to set CHAINUP to HIGH-Z. Refer to Table 1 for slave connections.

CHAINDN (Output)

When two or more devices are chained they communicate among themselves using the CHAINDN signals. See Chaining section. The JTAG interface is able to set CHAINDOWN to HIGH-Z. Refer to Table 1 for slave connections.

CHAINCS (Bi-directional)

When two or more devices are chained they communicate among themselves using the CHAINCS signals. See Chaining section. Internally pulled up. Refer to Table 1 for slave connections.

/MF (Match Flag, Output)

The /MF output indicates whether a match was found. The JTAG interface is able to set /MF to HIGH-Z.

/TRST (JTAG Reset, Input)

The /TRST is the Test Reset pin. Internally pulled up with 25K minimum. Must be tied to /RESET or tied LOW when not in use.

/TCLK (JTAG Test Clock, Input)

The /TCLK input is the Test Clock input. Must be tied at a valid logic level when not in use.

TMS (JTAG Test Mode Select, Input)

The TMS input is the Test Mode Select input. Internally pulled up with 25K minimum.

TDI (JTAG Test Data Input, Input)

The TDI input is the Test Data input. Internally pulled up with 25K minimum. Refer to Table 1 for slave connections.

TDO (JTAG Test Data Output, Output)

The TDO output is the Test Data output. Refer to Table 1 for slave connections.

VCC, GND

These pins are the power supply connection to the MUAA RCP. VCC must meet the voltage supply requirements in the Operating Conditions section relative to the GND pins, which are at 0 Volts (system reference potential), for correct operation of the device. All the ground and power pins must be connected to their respective planes with adequate bulk and high frequency bypassing capacitors in close proximity to the device.

Ball Descriptions

Table 1: Ball Descriptions

Functional Group	Ball Name(s)	Function	Type	PBGA Ball(s)
Synchronous Input Port	DIN[31:0]	Synchronous port data input.	Input 5V tol	b0:AA26, b1:AA25, b2:Y26, b3:Y25, b4:W26, b5:W25, b6:V26, b7:V25, b8:U26, b9:U25, b10:T26, b11:T25, b12:R26, b13:R25, b14:P26, b15:P25, b16:N26, b17:N25, b18:M26, b19:M25, b20:L26, b21:L25, b22:K26, b23:K25, b24:J26, b25:J25, b26:H26, b27:H25, b28:G26, b29:G25, b30:F26, b31:F25
	/DINE	When asserted, DIN is sampled by the rising edge of CLK. Connect to T2, R2, and P2.	Input 5V tol	T1
	/DINE-S1	Slave 1. Connect to T1, /DINE.	Input 5V tol	T2
	/DINE-S2	Slave 2. Connect to T1, /DINE.	Input 5V tol	R2
	/DINE-S3	Slave 3. Connect to T1, /DINE.	Input 5V tol	P2
	OP[3:0]	Synchronous port operation performed on data applied to DIN pins.	Input 5V tol	b0:U1, b1:U2, b2:U3, b3:T3
	DINREADY	When HIGH, indicates the synchronous port accepted the current operation.	Output	H1
	CLK	Rising edge is the device clock.	Input 3.3V only	D1
Synchronous Output Port	DOUT[31:0]	Synchronous port data output.	Output	b0:A21, b1:B21, b2:A20, b3:B20, b4:A19, b5:B19, b6:A18, b7:B18, b8:A17, b9:B17, b10:A16, b11:B16, b12:A15, b13:B15, b14:A14, b15:B14, b16:A13, b17:B13, b18:A12, b19:B12, b20:A11, b21:B11, b22:A10, b23:B10, b24:A9, b25:B9, b26:A8, b27:B8, b28:A7, b29:B7, b30:A6, b31:B6
	/DOUTVALID	Indicates when new data is available at the synchronous output port.	Output	G1
	/OE	DOUT high impedance control.	Input 5V tol	P1
	/DOUTE	DOUT enable control.	Input 5V tol	R1
	/MF	Match flag. Indicates if a match was found.	Output	E1

Table 1: Ball Descriptions (continued)

Functional Group	Ball Name(s)	Function	Type	PBGA Ball(s)
Processor Port	PROCD[31:0]	Processor port data.	Bidir 5V tol	b0:AB1, b1:AB2, b2:AC1, b3:AC2, b4:AF3, b5:AE3, b6:AF4, b7:AE4, b8:AF5, b9:AE5, b10:AF6, b11:AE6, b12:AF7, b13:AE7, b14:AF8, b15:AE8, b16:AF9, b17:AE9, b18:AF10, b19:AE10, b20:AF11, b21:AE11, b22:AF12, b23:AE12, b24:AF13, b25:AE13, b26:AF14, b27:AE14, b28:AF15, b29:AE15, b30:AF16, b31:AE16
	PROCA[5:0]	Processor port address bus.	Input 5V tol	b0:W1, b1:W2, b2:W3, b3:Y1, b4:Y2, b5:Y3
	R/W	Processor port read/write control	Input 5V tol	V2
	/PCS	Processor port chip select. Connect to AA2, AA3, and AB3.	Input 5V tol	AA1
	/PCS-S1	Slave 1. Connect to AA1, /PCS.	Input 5V tol	AA2
	/PCS-S2	Slave 2. Connect to AA1, /PCS.	Input 5V tol	AA3
	/PCS-S3	Slave 3. Connect to AA1, /PCS.	Input 5V tol	AB3
	PROCREADY	When HIGH, indicates the processor read data is available or the processor write data is accepted.	Output	K1
	INT	INT interrupt. Indicates the aged or learned queue has at least one entry or a write exception occurred.	Output	J1
	/RESET	Resets the MUAA RCP.	Input 5V tol	V1
	/FF	Full flag. Active when the device (or chain of devices) is full	Output	F1

Table 1: Ball Descriptions (continued)

Functional Group	Ball Name(s)	Function	Type	PBGA Ball(s)
Cascade	CHAIN0	NC. For MUSIC production test only.	Input	AF18
	CHAIN1	Internal chaining. Connect to AE19, CHAINUP-S1.	Input	AF19
	CHAIN2	Internal chaining. Connect to AE20, CHAINUP-S2.	Input	AF20
	CHAIN3	Internal chaining. Connect to AE21, CHAINUP-S3.	Input	AF21
	CHAIN0D	Internal chaining. Connect to AF23, CHAINDN.	Input	AE22
	CHAIN1D	Internal chaining. Connect to AE23, CHAINDN-S1.	Input	AD22
	CHAIN2D	Internal chaining. Connect to AD23, CHAINDN-S2.	Input	AC22
	CHAINUP	NC. For MUSIC production test only.	Output	AF22
	CHAINUP-S1	Internal chaining. Connect to AF19, CHAIN1.	Output	AE19
	CHAINUP-S2	Internal chaining. Connect to AF20, CHAIN2.	Output	AE20
	CHAINUP-S3	Internal chaining. Connect to AF21, CHAIN3.	Output	AE21
	CHAINDN	Internal chaining. Connect to AE22, CHAIN0D.	Output	AF23
	CHAINDN-S1	Internal chaining. Connect to AD22, CHAIN1D.	Output	AE23
	CHAINDN-S2	Internal chaining. Connect to AC22, CHAIN2D.	Output	AD23
	CHAIND-S3	NC. For MUSIC production test only.	Output	AC23
	CHAINCS	Internal chaining. Connect to AE17, AD17, and AC17.	Bidir	AF17
	CHAINCS-S1	Internal chaining. Connect to AF17.	Bidir	AE17
	CHAINCS-S2	Internal chaining. Connect to AF17.	Bidir	AD17
	CHAINCS-S3	Internal chaining. Connect to AF17.	Bidir	AC17
	CHAIN1X	NC. For MUSIC production test only.	Input	AE18
	CHAIN2X	NC. For MUSIC production test only.	Input	AD18
	CHAIN3X	NC. For MUSIC production test only.	Input	AC18
JTAG	/TRST	Test reset.	Input	N3
	TCLK	Test clock input.	Input	N2
	TMS	Test mode select.	Input	N1
	TDI	Test data input.	Input	M1
	TDI-A	Internal JTAG chain. Connect to L2, TDO-A.	Input	M2
	TDI-B	Internal JTAG chain. Connect to L3, TDO-B.	Input	M3
	TDI-C	Internal JTAG chain. Connect to L3, TDO-C.	Input	M4
	TDO	Test data output.	Output	L1
	TDO-A	Internal JTAG chain. Connect to M2, TDI-A.	Output	L2
	TDO-B	Internal JTAG chain. Connect to M3, TDI-A.	Output	L3
	TDO-C	Internal JTAG chain. Connect to M4, TDI-A.	Output	L4
Power	3.3V	Device power, 3.3 volts.	N/A	AD7, AD8, AD13, AD14, AD19, AD20, AC7, AC8, AC13, AC14, AC19, AC20, Y4, Y23, Y24, W4, W23, W24, R3, R4, R12, R13, R14, R15, P3, P4 P12, P15, P23, P24, N12, N15, N23, N24, M12, M13, M14, M15, H23, H24, G23, G24, D6, D7, D10, D11, D15, D16, D20, D21, C6, C7, C10, C11, C15, C16, C20, C21

Table 1: Ball Descriptions (continued)

Functional Group	Ball Name(s)	Function	Type	PBGA Ball(s)
Ground	GND	Device ground.	N/A	AF1, AF2, AF24, AF25, AF26 AE1, AE2, AE24, AE25, AE26 AD1–AD6, AD9– AD12, AD15, AD16, AD21, AD24, AD25, AD26, AC3–AC6, AC9–AC12 AC15, AC16, AC21, AC24–AC26, AB4, AB23–AB26, AA4, AA23, AA24, V3, V4, V23, V24, U4, U23, U24, T4, T11–T16, T23, T24, R11, R16, R23, R24, P11, P13, P14, P16, N4, N11, N13, N14, N16, M11, M16, M23, M24, L11–L16, L23, L24, K23, K24 J23, J24, F23, F24, E23–E26, D2–D5, D8, D9, D12–D14, D17–D19, D22–D26, C1–C5, C8, C9, C12–C14, C17–C19, C22– C26, B1–B5, B22–B26, A1–A5, A22–A26

OPERATIONAL CHARACTERISTICS

Loading and Unloading

In order to keep data alignment simple, the number of words to be loaded and unloaded for each operation is kept consistent for each CAM/RAM partition configuration and the width of the port.

Tables 2 and 3 show the cycle sequence and CAM/RAM bit mappings for 32- and 16-bit bus modes. The bus may be selected for each port independently. Table 4 shows whether CAM, RAM or both types of segments are used on input or output cycles for each operation.

Loads always start right aligned from the least significant word, CAM partition first, followed by RAM if necessary. Most instructions do not require the entire 80 bits to be loaded.

CAM data is required as an input for all operations except READ LQUEUE and READ AQUEUE. The use of RAM data is optional (i.e., it is not necessary to perform all RAM cycles when inputting data). However, the user must be aware that INSERT and LEARN operations will over-write RAM data. Therefore, the application should remain consistent in the number of RAM bits used for these operations.

All CAM and RAM segment writes except the last use the LOAD instruction. The last segment of data uses the instruction for the desired operation.

Depending on the operation, unloads either start from the right aligned, least significant word of CAM followed by the right aligned, least significant word of RAM or just from the right aligned, least significant word of RAM. For instance, a QUEUE read returns CAM then RAM, whereas a search just returns RAM. Where the CAM/RAM partition does not lie on a port width boundary the last word of the read may contain undefined data in the most significant bits. The number of unload cycles actually completed is optional.

The DOUT register stores the results of operations from the asynchronous processor port. Search results are obtained by repeated reads of DOUT until all RAM data is read. When performed from the processor port, READ LQUEUE and READ AQUEUE return the first segment of CAM data on the cycle that requests the operation; additional CAM and RAM segments are obtained by repeated reads of the DOUT register.

Loading is flow controlled on the synchronous DIN port with the DINREADY signal, which is HIGH when data is accepted by the DIN port. On the Processor port the PROCREADY signal is HIGH when the current write cycle may complete.

Operations

On the synchronous port, operations are started on the CLK cycle in which the requested Op-Code is written. On the processor port operations are started when the chosen operation register is written. The user should use the flow control mechanisms to determine when results are available. On the synchronous port the /DOUTVALID signal is asserted for one CLK cycle when new data is written to the DOUT port. The processor port will assert its PROCREADY signal on the CLK edge that data is available. Note that there is no internal flow control from the sync DOUT port back to the sync DIN port. The DOUT data is overwritten if it is not unloaded.

Table 2: 32-Bit Bus Mode CAM/RAM Cycles by Partition Configuration

Cycle	No RAM 79:0 CAM	79:64 RAM 63:0 CAM	79:48 RAM 47:0 CAM	79:32 RAM 31:0 CAM
1	CAM[31:0]	CAM[31:0]	CAM[31:0]	CAM[31:0]
2	CAM[63:32]	CAM[63:32]	CAM[47:32]*	RAM[63:32]
3	CAM[79:64]*	RAM[79:64]*	RAM[79:48]	RAM[79:64]*

Note: **Bus bits [15:0] contain data. Bus bits [31:16] are undefined.*

Table 3: 16-Bit Bus Mode CAM/RAM Cycles by Partition Configuration

Cycle	No RAM 79:0 CAM	79:64 RAM 63:0 CAM	79:48 RAM 47:0 CAM	79:32 RAM 31:0 CAM
1	CAM[15:0]	CAM[15:0]	CAM[15:0]	CAM[15:0]
2	CAM[31:16]	CAM[31:16]	CAM[31:16]	CAM[31:16]
3	CAM[47:32]	CAM[47:32]	CAM[47:32]	RAM[47:32]
4	CAM[63:48]	CAM[63:48]	RAM[63:48]	RAM[63:48]
5	CAM[79:64]	RAM[79:64]	RAM[79:64]	RAM[79:64]

Table 4: Input and Output CAM/RAM Cycles by Operation

Operation	DIN, PROCD (Write)	DOUT, PROCD (Read)
INSERT	CAM & RAM	N/A
SEARCH	CAM only	RAM only
SEARCHA	CAM only	RAM only
LEARN	CAM & RAM	N/A
DELETE	CAM only	N/A
READ LQUEUE	N/A	CAM & RAM
READ AQUEUE	N/A	CAM & RAM

Device Chaining

Up to four MUAA 2K RCPs may be chained with no external logic. Figure 3 shows the interconnection. Unused CHAIN[3:0] pins should be left unconnected.

The /MF, /FF, INT, DOUTVALID, DINREADY, and PROCREADY signals should only be used on the master device and left disconnected on the slave devices. The master device is the one with no connection to the CHAINUP pin.

Where device pins are paralleled, attention should be paid to signal integrity, in particular to signals used for clocking, i.e., CLK, /PCS. PCB layout techniques such as daisy chaining and driver to track impedance matching should be observed.

The scheme in Figure 3 allows devices to be designed in but not fitted. The fit order would be MASTER, SLAVE1, SLAVE2, SLAVE3.

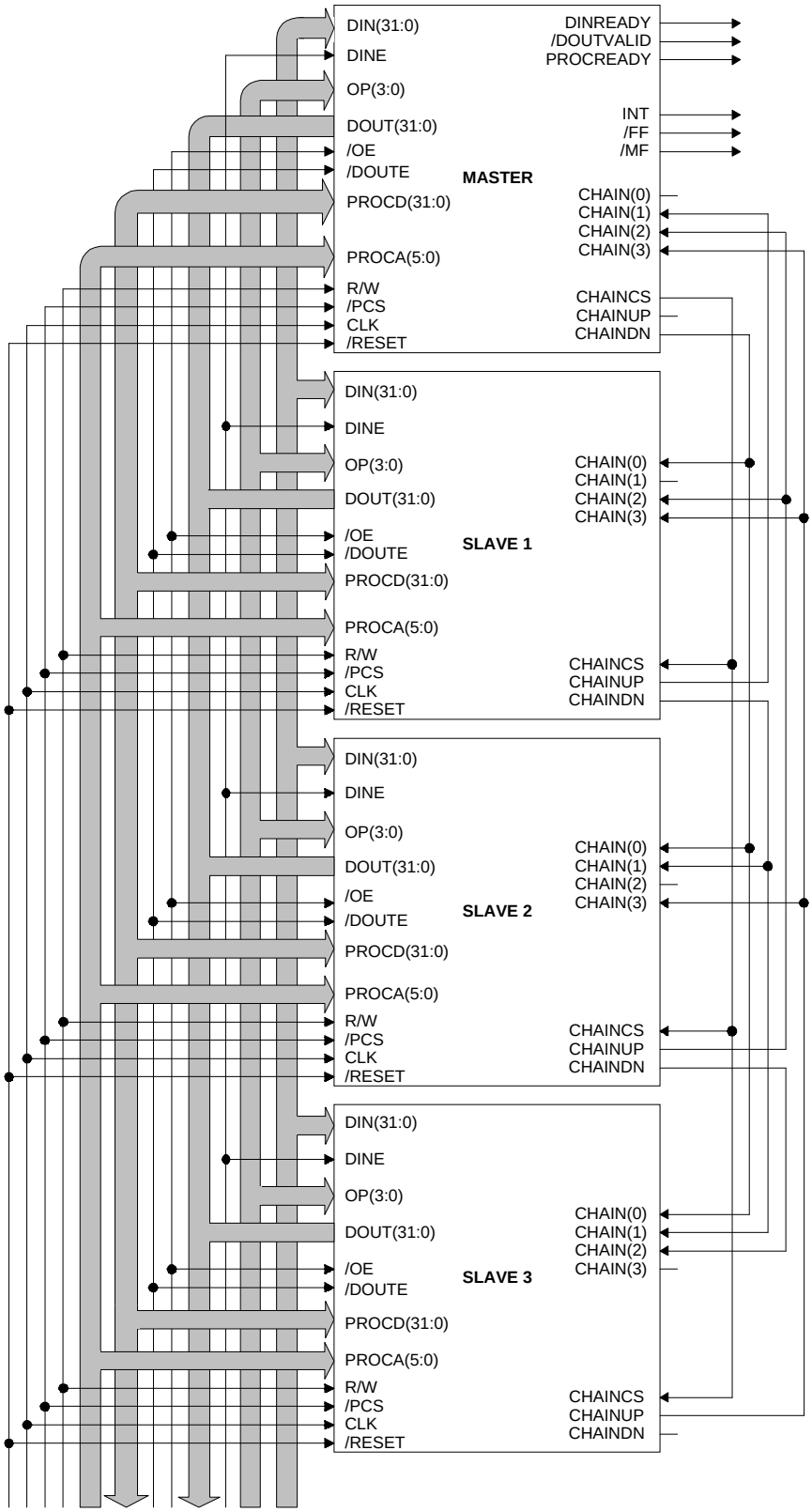


Figure 3: Device Chaining (2K only)

Interrupts

There are four sources of interrupts that will cause the INT pin to be asserted: AQUEUE, LQUEUE, SWEX, and PWEX. The appropriate enables must be set in the Configuration register to enable the interrupts.

The interrupt service routine should read the appropriate flag registers to determine the interrupt cause. The flags are available individually or from the Address Index register. The appropriate individual flag register must be read in order to acknowledge the interrupt.

LQUEUE and AQUEUE

AQUEUE and LQUEUE interrupts are set by an entry being written into one or another of the queues. When the flag register is read the interrupt is acknowledged. The processor may read the LQUEUE and AQUEUE flags to determine when all the entries are read from the appropriate queue. The interrupt will not be reasserted until a queue has been emptied and then gets another entry. Note that it is possible for learned entries to be aged and aged entries to be learned. If this occurs the AQUEUE and LQUEUE flags may be set for an entry that has changed status. The user may qualify reads from AQUEUE and LQUEUE with the appropriate ports match flag that will be asserted if the data is valid.

SWEX and PWEX

SWEX and PWEX interrupts are set when a write exception condition occurs. This occurs when two Write cycles are pending in the device and there is only one space left.

The SWEX and PWEX flags indicate which port caused the exception and which are available individually to the processor. Both processor write exceptions are available in the processor Address index port and the DOUT port Address index word.

JTAG

Please refer to IEEE Standard 1149.1 for information on using the JTAG functions. See Table 5 for JTAG functions. A BSDL file is available; check the MUSIC Semiconductors website or contact MUSIC Technical Support.

Table 5: JTAG Functions

ID								
Binary	0011	1010	1010	0000	0010	0001	0011	0011
HEX	3	A	A	0	2	1	3	3
Description	Version	MUAA		2K		MANUF ID		

JTAG Codes	
EXT TEST	0000
BYPASS	1111
SAMPLE	0001
ID CODE	0010
CLAMP	0100
HIGH-Z	0011

Typical Example

This typical example shows the cycles that the MUAA RCP would perform in a multiport switch. The CAM/RAM partition is set to 48 bits CAM, 32 bits RAM. Both the processor port and the synchronous port are 32 bits wide. The index and flags are programmed to be the last word out of the DOUT port. The synchronous port has priority. The LQUEUE and AQUEUE are enabled. The CAM partition is used to store 48-bit MAC addresses and the RAM partition used to store associated data to the MAC address such as switch port and VLAN numbers.

Sync Port Cycle 1 is a search to lookup the port associated with a frame DA (Destination address). At CLK1 the first word (32 bits) of CAM search word is loaded. At CLK2 the last 16 bits of CAM search word is loaded and the instruction “search” given. The most significant 16 bits of the second word are discarded as the CAM partition is 48 bits wide. The results from the DA search will not be available until CLK6 because the operation takes three CLK periods to complete. Due to the internal design of the MUAA RCP, pipelining is possible; therefore, further operations can be performed while the DA search is being done internally.

Sync Port cycle2 is a learn on a frame SA (Source address). At CLK3 the first word of CAM is loaded, at CLK4 the second word is loaded (most significant 16 bits discarded). At CLK5 the learn instruction is given along with the word of RAM data that would contain the port ID and other data associated with the SA.

At CLK6 the results of the search instruction issued in cycle1 are available at the DOUT bus of the synchronous port, as indicated by /DOUTVALID going active for a CLK. The result of this cycle was a no-match condition as /MF was not asserted LOW. Because the cycle was a DA search and there was a no-match result, there will be no data available on the DOUT bus. Typically in this situation a switch would forward the frame to all ports or all ports on the same VLAN.

Sync Port cycle3 starts at CLK8, which is the DA search of the next frame.

AT CLK 10 the results of the cycle2 learn operation are available. /MF was not asserted LOW; therefore the 48-bit CAM partition data was not found during the compare. The MUAA RCP automatically writes the 80-bit CAM/RAM word into the next free location of the memory array along with the most up to date time stamp or entry life. The address index is available from the DOUT bus to indicate where in the memory array the data was placed. This can be used to implement further associated data in software or hardware. Furthermore, the INT output is asserted to indicate that the "learned" word was entered into the LQUEUE.

Sync Port cycle4, which is the SA learn of the same frame as Sync Port cycle3, is initiated at CLK10.

The processor can also be used to access the MUAA RCP for general housekeeping duties. The LQUEUE contains the contents of the virtual learned queue. A processor cycle is started around CLK12 to read the LQUEUE register. This cycle is unable to be completed because the CAM core is busy servicing the synchronous port. PROCREADY remains inactive to inform the processor of the delay. The cycle is therefore extended and will complete when the MUAA RCP asserts PROCREADY HIGH.

/MF is asserted LOW to indicate a match result on the CAM partition compare. At this point DOUT will be used to transfer the associated data and the address index of the matching condition. The associated data is available first (RAM partition) and would normally contain the port ID in a typical switch. The RAM partition is configured as 32 bits wide and can therefore be transferred in one CLK period. /DOUTE is asserted by the user to transfer the next word of data on the next clock period. As the RAM takes only one cycle, the address index is available after the associated data.

The result of cycle4, which was a SA learn, is available at CLK17. The learn instruction produced a match result. There was no need to overwrite the CAM/RAM partitions, but the MUAA RCP automatically updated the time stamp or entry life of the matching entry. The address index of the entry becomes available at the DOUT port.

The processor cycle data requested earlier, can now become available at CLK21. PROCREADY is asserted HIGH by the device to indicate that the cycle may be completed. The first 32-bit word is available on the PROCD bus and can be read by the processor. The two remaining 32-bit words that complete the LQUEUE entry are read by the subsequent processor cycles. These cycles do not require access to the CAM core, hence the PROCREADY signal is asserted immediately once the cycle is initiated. The processor may use the LQUEUE data to maintain a management database of MAC addresses and associated port IDs.

Back to back DA searches are shown from CLK25 onward. This is to demonstrate how the synchronous port handshaking works using the /DINREADY output. Sync port cycle5 and cycle6 are completed normally but at CLK29 /DINREADY goes LOW to indicate that the MUAA RCP cannot accept the load operation of sync cycle7. Therefore the host must hold the DIN, OP, and DINE signals active until /DINREADY goes HIGH. At this point the MUAA RCP will return /DINREADY to HIGH to indicate that it has accepted the DIN and OP information.

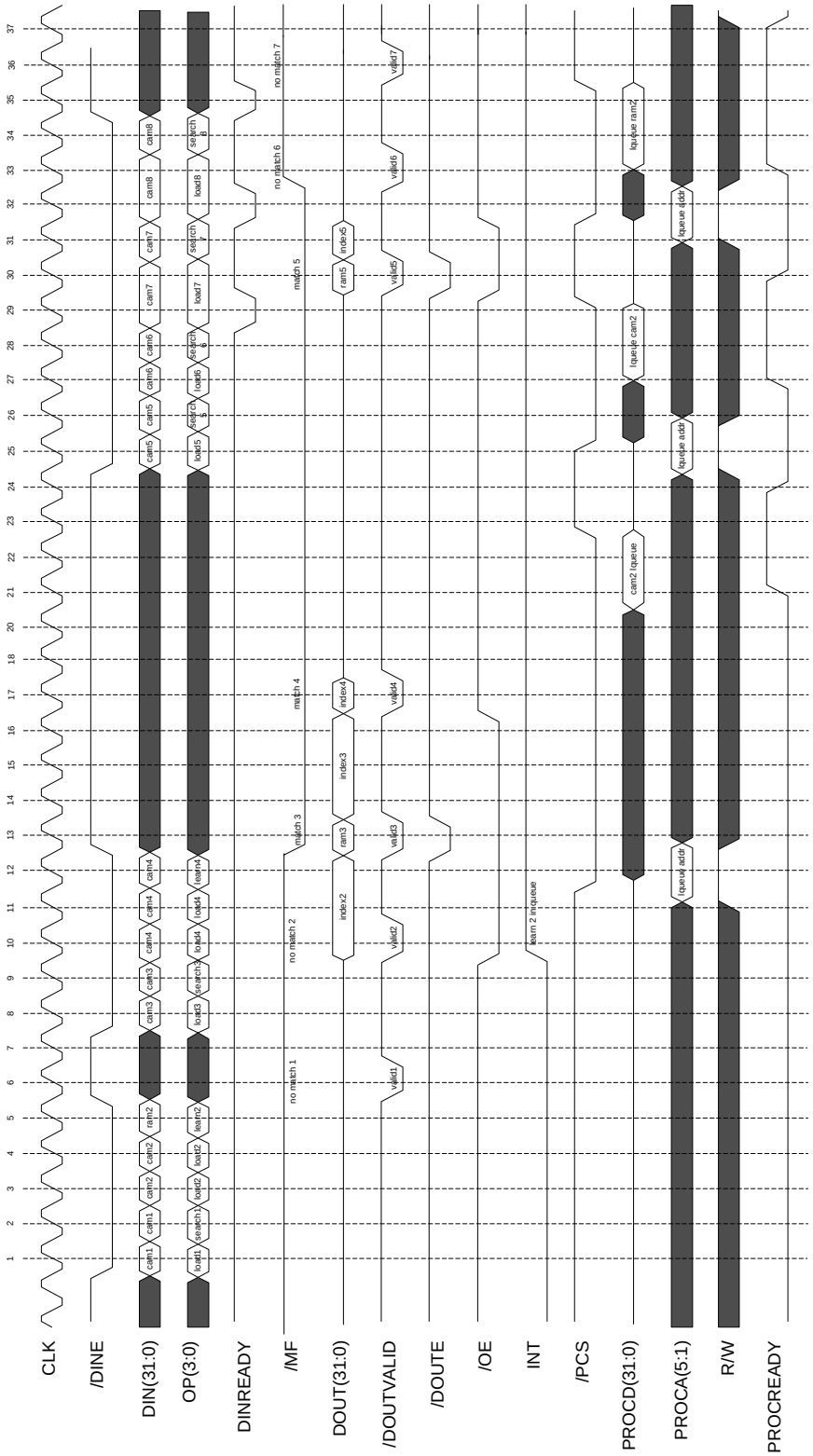


Figure 4: Example Sequence

INSTRUCTION SET DESCRIPTIONS

Mnemonic: NOOP
Binary Op-Code: 0 CLKS: 3
Function: No operation.

Mnemonic: load<DIN>
Binary Op-Code: 1 CLKS: 1
Function: Load a word of the DIN data, starting with the least significant word. This instruction is applied to all words loaded into the DIN port except the last word. The last word is loaded with the Op-Code of the operation to be performed. Refer to the Loading and Unloading section.

Mnemonic: insert<DIN>
Binary Op-Code: 2 CLKS: 4
Function: Write DIN into the CAM/RAM. If data exists in the CAM partition already, the RAM partition will be overwritten with the new RAM partition data. The entry will be marked as permanent. The address index may be read from the output ports. See Note 1 regarding write exception.

Mnemonic: search<DIN>
Binary Op-Code: 3 CLKS: 3
Function: Search for data in the CAM partition of DIN. If data is found the match flag is asserted and RAM data will appear at DOUT. The address index and flags may also be read.

Mnemonic: searcha<DIN>
Binary Op-Code: 4 CLKS: 4
Function: Search for data in the CAM partition of DIN. If data is found the match flag is asserted and RAM data will appear at DOUT and the age of the entry is updated. The address index and flags may also be read.

Mnemonic: learn<DIN>
Binary Op-Code: 5 CLKS: 4
Function: Search for data in the CAM partition of DIN. If data is found, the match flag is asserted and the RAM partition written. The address index may be read. Update the age. If data is not found, write the CAM and RAM partitions to the next free address. The address index may be read. See Note 1 regarding write exception.

Mnemonic: delete<DIN>
Binary Op-Code: 6 CLKS: 3
Function: Search for data on the CAM partition of DIN. If data is found delete the data. The address index may be read.

Mnemonic: age
Binary Op-Code: 7 CLKS: 3
Function: If the aged virtual queue is disabled: This instruction will remove all entries whose life has expired and are not marked as permanent. Removed entries will not participate in future searches. If the aged virtual queue is enabled: This instruction will move all entries whose life has expired to the aged virtual queue. If a learn instruction matches the CAM partition of an entry in the aged virtual queue, the entry is moved to the learned virtual queue and the new RAM data written.

Mnemonic: clear
Binary Op-Code: 8 CLKS: 3
Function: Reset array to empty.

Mnemonic: clear LQUEUE
Binary Op-Code: 9 CLKS: 3
Function: Delete the contents of the learned virtual queue. The entry will not generate a match on a SEARCH or SEARCHA operation.

Mnemonic: clear AQUEUE
Binary Op-Code: 10 CLKS: 3
Function: Delete the contents of the aged virtual queue, if enabled.

Mnemonic: read LQUEUE
Binary Op-Code: 11 CLKS: 3
Function: Read the next learned queue entry. Entries are returned in internal priority order, lowest address first, not in the order they were written. The address index may be read. Note that entries do not have to be read from the LQUEUE if deemed unnecessary. The device treats learned entries as if they are valid entries.

Mnemonic: read AQUEUE
Binary Op-Code: 12 CLKS: 4
Function: This instruction is available only if the AQUEUE is enabled. Read the next aged queue entry. Entries are returned in internal priority order, lowest address first, not in the order they were written. The address index may be read.

Notes:

1. *Due to the pipelined nature of the device, it is possible for a write cycle to be pending (learn or insert) when the device is full. A write exception interrupt will indicate when this occurs if enabled. See Interrupt section.*
2. *There is one CLK of latency to start the pipe on the synchronous port. The number of CLKs per instruction assumes the pipe is kept full and indicates throughput.*

Processor Port Registers

Table 6: Processor Port Registers

Register/Instruction	PROCA[5:0]	Bit(s)	Function
NOOP	0x00	31:0 W	NOOP operation
load<DIN>	0x02	31:0 W	Perform load operation.
insert<DIN>	0x04	31:0 W	Perform insert operation.
search<DIN>	0x06	31:0 W	Perform search operation.
searcha<DIN>	0x08	31:0 W	Perform searcha operation.
learn<DIN>	0x0A	31:0 W	Perform learn operation.
delete<DIN>	0x0C	31:0 W	Perform delete operation.
age	0x0E	N/A W	Age MUAA RCP contents.
clear	0x10	N/A W	Perform clear operation.
clear LQUEUE	0x12	N/A W	Perform clear LQUEUE operation.
clear AQUEUE	0x14	N/A W	Perform clear AQUEUE operation.
read LQUEUE	0x16	31:0 R	Read LQUEUE data.
read AQUEUE	0x18	31:0 R	Read AQUEUE data.
DOUT	0x1A	31:0 R	After an operation has been performed on the processor port the output data may be read and unloaded from this port. Data is read right aligned least significant word first.
CONFIGURATION	0x20	0 R/W	Processor port width. If set to 16-bit mode the most significant 16 bits of each register are addressed by bit 0 of the address pins. After reset, the Configuration register must be written before any other, 0 = 32-bit, 1 = 16-bit. Resets to 0.
		1 R/W	Sync port input width. 0 = 32-bit; 1 = 16-bit. Resets to 0.
		2 R/W	Sync port output width. 0 = 32-bit; 1 = 16-bit. Resets to 0.
		4:3 R/W	CAM/associated data partition point 0 = 79:0 CAM 1 = 79:64 RAM 63:0 CAM 2 = 79:48 RAM 47:0 CAM 3 = 79:32 RAM 31:0 CAM Resets to 0
		5 R/W	DOUTVALID Timing. 0 = Same CLK as Data; 1 = 1 CLK before Data. Resets to 0.
		6:7 R/W	Reserved. Write 0.
		8 R/W	INT active HIGH or active LOW. 0 = LOW; 1 = HIGH. Resets to 1.
		9 R/W	Enable LQUEUE interrupt. 0 = Disable; 1 = Enable. Resets to 0.
		10 R/W	Enable AQUEUE interrupt. 0 = Disable; 1 = Enable. Resets to 0.
		11 R/W	Enable PWEX interrupt. 0 = Disable; 1 = Enable. Resets to 0.
		12 R/W	Enable SWEX interrupt. 0 = Disable; 1 = Enable. Resets to 0.
		13 R/W	Enable auto-aging function. 0 = Disable; 1 = Enable. Resets to 0.
		14 R/W	Enable AQUEUE queue. 0 = Disable; 1 = Enable; Resets to 0. Note that LQUEUE is always enabled.
		15 R/W	Set port priority. 0 = Sync port; 1 = Processor port. Resets to 0.
		16 R/W	Reserved. Write 0.
		17 R/W	Set Sync DOUT port address index first read or last read. 0 = Last, 1 = First. Resets to 0.
		18 R/W	1 = Auto age highest-priority; 0 = lowest-priority. Resets to 0. Only if auto-aging is on.
		31:19 R/W	Reserved. Write 0.
MF	0x22	0 R	Indicates the Processor port got a match on the last operation. 1 = Match, 0 = No Match.
FF	0x24	0 R	Full flag. Indicates when the device has one or zero free entries left. 1 = Full, 0 = Not Full.

Table 6: Processor Port Registers (continued)

Register/Instruction	PROCA[5:0]	Bit(s)	Function
Address Index	0x26	25:0 R	Once an operation has been performed on the Processor port the address index is available here. Useful as an index for associated tables in software.
		26 R	SWEX flag
		27 R	PWEX flag
		28 R	LQUEUE flag
		29 R	AQUEUE flag
		30 R	Processor Port Match flag; 1 = Match
		31 R	Full flag; 1 = Full
LQUEUE Flag	0x28	0 R	Indicates the LQUEUE has at least one entry. Note this bit is available even if the INT pin is disabled. A read clears the interrupt.
AQUEUE Flag	0x2A	0 R	Indicates the AQUEUE has at least one entry. Note this bit is available even if the INT pin is disabled. A read clears the interrupt.
PWEX Flag	0x2C	0 R	Indicates a write exception condition has occurred on the processor port. A read clears the interrupt.
SWEX Flag	0x2E	0 R	Indicates a write exception condition has occurred on the syncport. A read clears the interrupt.
Auto-Age Interval	0x30	31:0 R/W	When auto-aging is enabled the CLK is divided by the value in this register to provide the auto-age interval. Resets to 02FAF080h = 1 second with 50 MHz CLK.
Learned Entry Life	0x32	8:0 R/W	This register sets the life of a learned entry in units of the auto-age Interval register. Resets to 012Ch = 300.
Info	0x34	1:0 R	Number of cascaded devices
		2 R	Read 0
		31:3 R	Device ID. 1 = MUAA RCP.
Size	0x36	31:0 R	Chain size. Multiples of 0.25K
Revision	0x38	3:0 R	Master Device Rev.
		7:4 R	Slave 1 Rev.
		11:8 R	Slave 2 Rev.
		15:12 R	Slave 3 Rev.
		31:16 R	Read 0

ELECTRICAL

Absolute Maximum Ratings

Supply Voltage	-0.5 to 4.6 Volts
Voltage on All Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature	-40°C to 85°C
Storage Temperature	-55°C to 125°C
DC Output Current	20 mA (per output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages referenced to GND.

Operating Conditions

Symbol	Parameter	Min.	Typical	Max.	Units	Notes
V_{CC}	Operating supply voltage	3.0	3.3	3.6	Volts	
V_{IH}	Input voltage logic 1	2.0		5.5	Volts	All other pins
		2.4		V_{DD} + 0.3	Volts	CLK
V_{IL}	Input voltage logic 0	-0.3		0.8	Volts	
T_A	Ambient operating temperature	0		70	°C	Still air

Electrical Characteristics

Symbol	Parameter		Min.	Typical	Max.	Units	Notes
I_{CC}	Average power supply current			310	400	mA	MUAA2K
				1.25	1.6	A	MUAA8K
$I_{CC(SB)}$	Stand-by power supply current			2	7	mA	
V_{OH}	Output voltage logic 1		2.4			Volts	I_{OH} = -8.0 mA
V_{OL}	Output voltage logic 0				0.4	Volts	I_{OL} = 8.0 mA
I_{IZ}	Input leakage current		-2		2	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OZ}	Output leakage current		-10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$
I_{RP}	Input pull-up resistors	MUAA2K	25			KΩ	/TRST, TMS, TDI
		MUAA8K	6.25			KΩ	

Capacitance

Symbol	Parameter		Max.	Units	Notes
C_{IN}	Input capacitance	MUAA2K	6	pF	f = 1 MHz, V_{IN} = 0V
		MUAA8K	45	pF	
C_{OUT}	Output capacitance	MUAA2K	7	pF	f = 1 MHz, V_{OUT} = 0V
		MUAA8K	45	pF	

TIMING DIAGRAMS

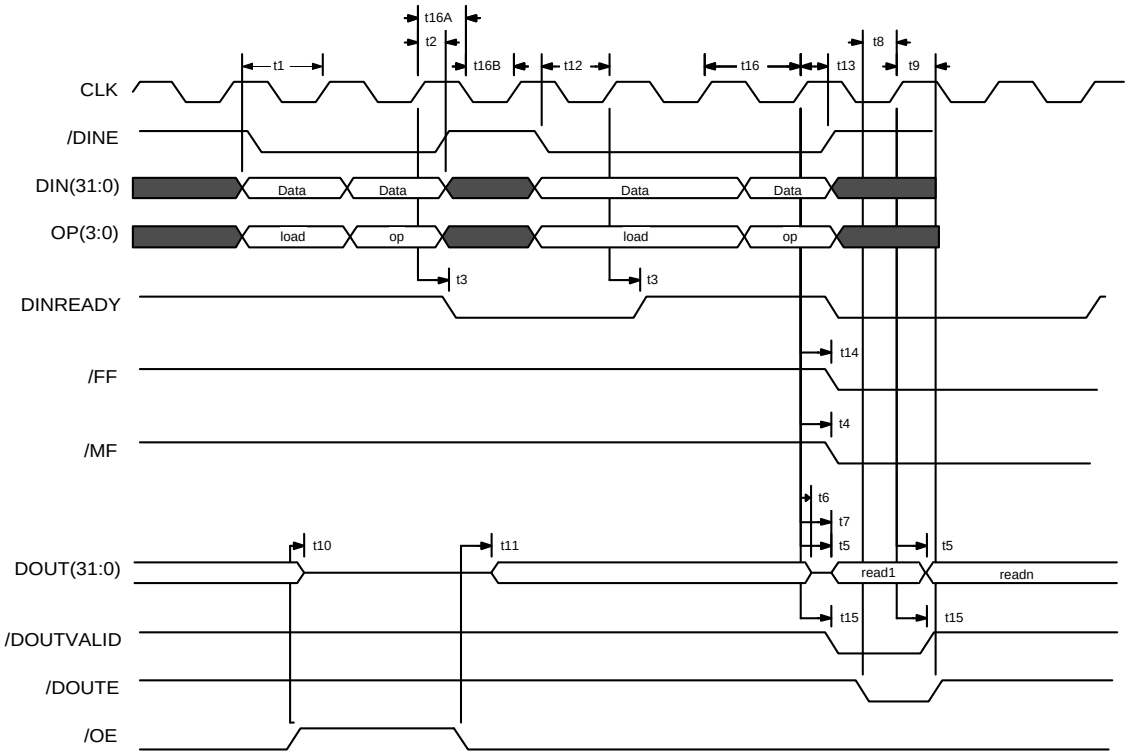


Figure 5: Sync Port Cycle

Table 7: Sync Port Cycle

		- 20		- 30		
No.	**Name**	**Min.**	**Max.**	**Min.**	**Max.**	**Comment**
t1	tDVCH	5		7		DIN(31:0), OP(3:0) setup to CLK HIGH
t2	tCHDX	3		4		CLK HIGH to DIN(31:0), OP(3:0) hold
t3	tCHDRV		16		18	CLK HIGH to DINREADY valid
t4	tCHMV		10		12	CLK HIGH to /MF valid
t5	tCHQV		15		18	CLK HIGH to DO valid
t6	tCHQZ	0.5	2.5	0.5	4	CLK HIGH to DO Hi-Z
t7	tCHQX	3		4		CLK HIGH to DO active
t8	tQEVCH	5		7		/DOUTE setup to CLK HIGH
t9	tCHQEX	3		4		CLK HIGH to /DOUTE hold
t10	tGHQZ	0.5	3	0.5	4	/OE to DO Hi-Z
t11	tGLQX	3		4		/OE to DO active
t12	tDEVCH	5		7		/DINE setup to CLK HIGH
t13	tCHDEX	3		4		CLK HIGH to DINE hold
t14	tCHFV		10		12	CLK HIGH to /FF valid
t15	tCHQVV		10		12	CLK HIGH to /DOUTVALID
t16	tCHCH	20		30		CLK period
t16A	tCHCL	8		12		CLK HIGH time
t16B	tCLCH	8		12		CLK LOW time

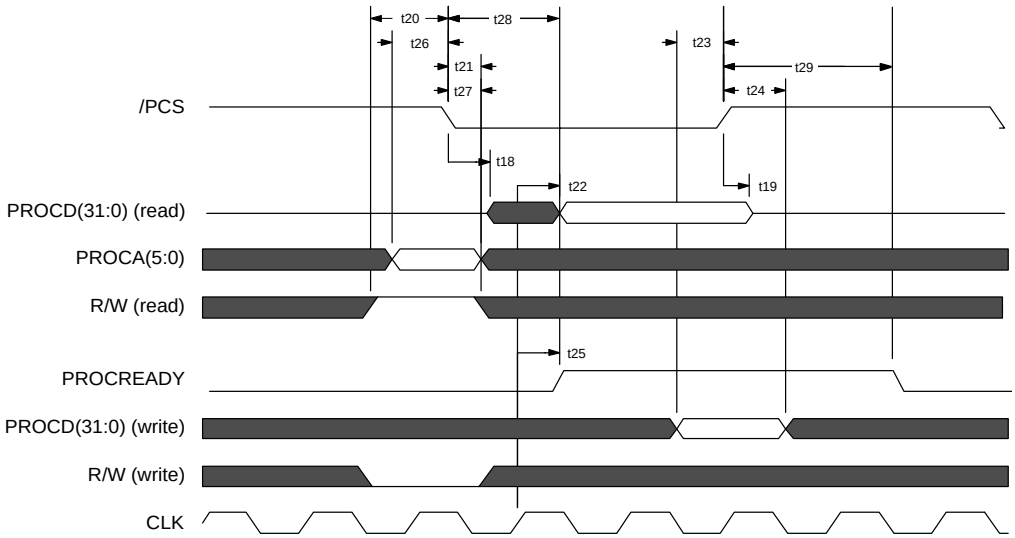


Figure 6: Processor Port Cycle

Table 8: Processor Port Cycle

		- 20		- 30		
No.	**Name**	**Min.**	**Max.**	**Min.**	**Max.**	**Comment**
t18	tSLDQX	t16		t16		/PCS LOW to PROCD active
t19	tSHDQZ		8		12	/PCS HIGH to PROCD HI-Z
t20	tRWVSL	3		4		R/W setup to /PCS LOW
t21	tSLRWX	3		4		/PCS LOW to R/W hold
t22	tCHDQV		15		18	CLK to PROCD valid (read)
t23	tDQVSH	5		8		PROCD setup to /PCS HIGH (write)
t24	tSHDQX	3		5		/PCS HIGH to PROCD hold (write)
t25	tCHPRH		10		12	CLK HIGH to PROCREADY valid
t26	tAVSL	5		7		PROCA setup to /PCS LOW
t27	tSLAX	3		4		/PCS LOW to PROCA hold
t28	tSLPRH		Nxt16*		Nxt16*	/PCS LOW to PROCREADY HIGH
t29	tSHPRL		4xt16*		4xt16*	/PCS HIGH to PROCREADY LOW
t30	tCHIV		10		12	CLK HIGH to INT valid

***Notes:** **

N = 3 for all write operations

N = 6 for all register read operations

N = 10 for read LQUEUE operations

N = 11 for read AQUEUE operations

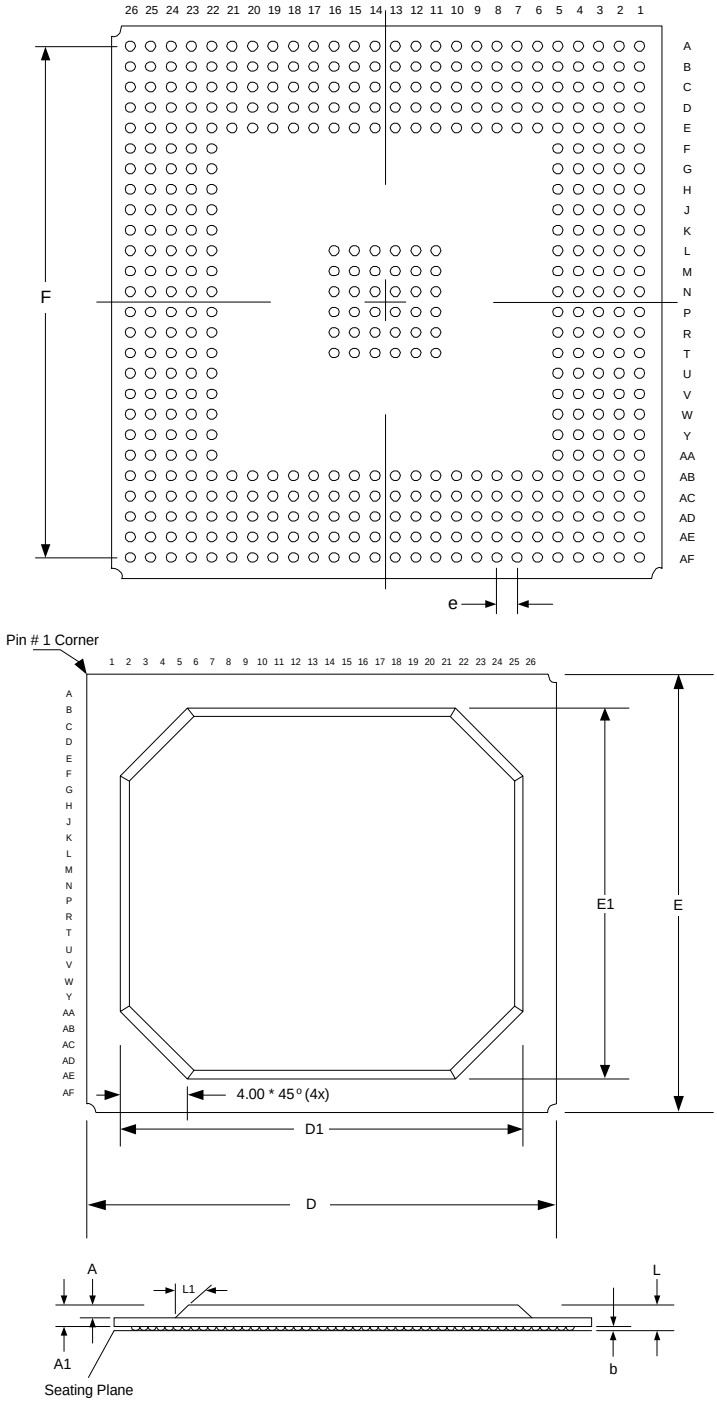
Assumes no Sync port activity to core on previous processor port core operation pending completion. Depending on Sync port activity (auto-age events and processor port priority setting), processor port operations may be extended.

NOTES

NOTES

PACKAGES

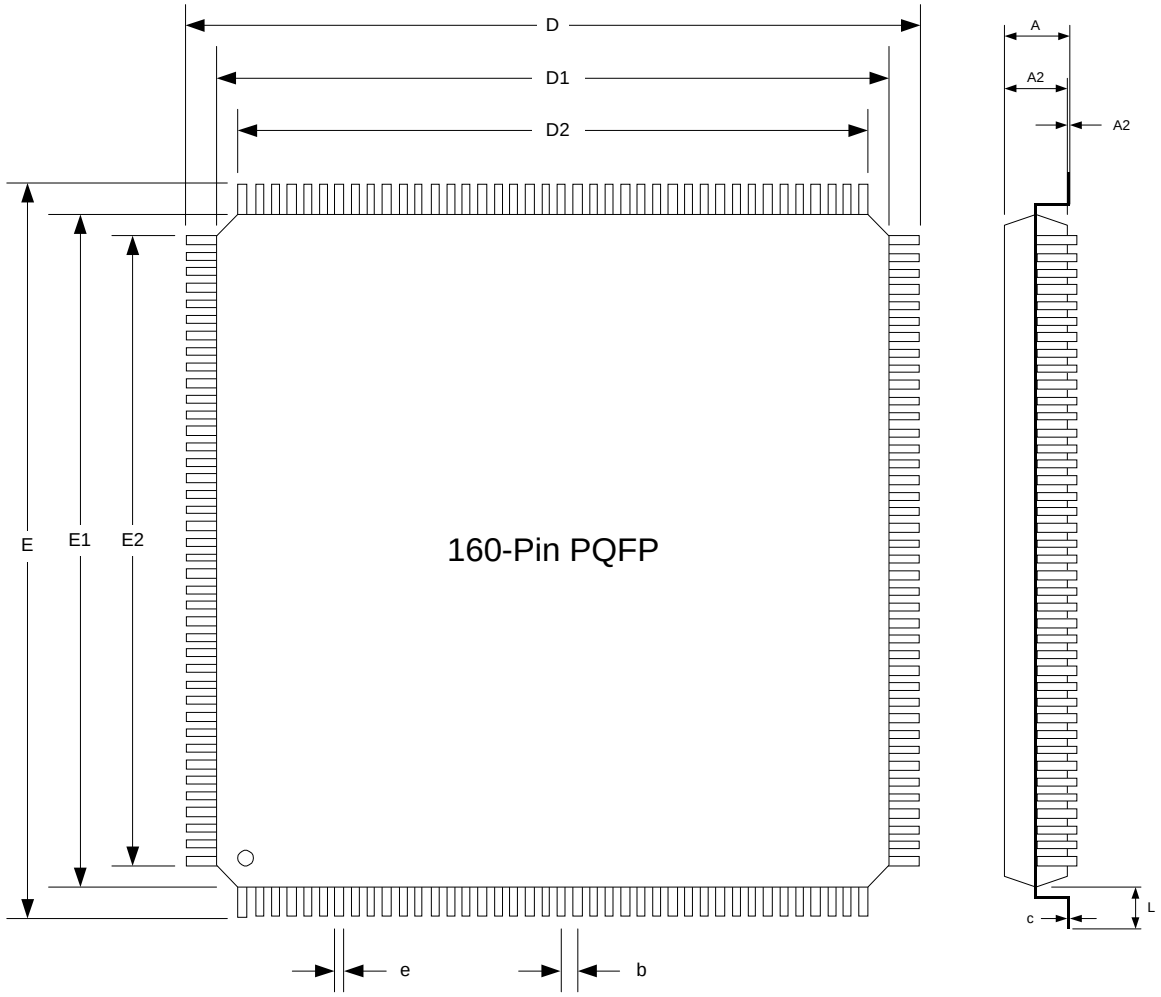
388-Pin PBGA



388-Pin PBGA Dimensions

	Dim. A	Dim. A1	Dim. b	Dim. D	D1	Dim. E	E1	Dim. e	Dim. F	Dim. L	L1
Min.			0.50	34.80		34.80				2.20	
Nom.	1.17	1.73		35.00	30.00	35.00	32.00	1.27	31.75	2.33	30°
Max.			O.70	35.20		35.20				2.46	

160-Pin PQFP



160-Pin PQFP Dimensions

	Dim. A	Dim. A1	Dim. A2	Dim. b	c	Dim. D	D1	D2	Dim. E	E1	E2	Dim. e	Dim. L
Min.		0.25	3.20	0.22	0.11								
Nom.			3.32	0.30	0.15	31.20	28.00	25.35	31.20	28.00	25.35	0.65	1.60
Max.	4.10		3.60	0.38	0.23								

ORDERING INFORMATION

Part Number	Cycle Time	Package	Temperature	Voltage
MUAA2K80-20QGC	20 ns	160-Pin PQFP	0–70° C	3.3 ± 0.3
MUAA2K80-30QGI	30 ns	160-Pin PQFP	-40–85° C	3.3 ± 0.3
MUAA8K80M-20B388C	20 ns	388-Pin PBGA	0–70° C	3.3 ± 0.3

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