



SANYO Semiconductors

DATA SHEET

LC7942KD — CMOS IC

Dot-Matrix LCD Drivers

Overview

The LC7942KD is a common driver LSI for driving large dot-matrix LCD displays. It features a built-in 64-bit bidirectional shift register and a 4-level LCD driver. It can also be connected in cascade to increase the number of bits. The LC7942KD is designed to be used with LC7940KD (QIP100D) or LC7941KDR (QIP100DR) segment drivers to drive large LCD panels.

Features

- 64 built-in LCD display drive circuits
- 1/64 to 1/128 display duty cycle
- Input/outputs for cascade connection
- Bias supply voltages can be supplied externally
- Operating supply voltage and ambient temperature:
 - 2.7 to 5.5V logic supply (V_{DD}) at $T_a = -20$ to $+85^{\circ}\text{C}$
 - 8 to 20V LCD supply ($V_{DD}-V_{EE}$) at $T_a = -20$ to $+85^{\circ}\text{C}$
- CMOS process
- package: QIP80D

■ Any and all SANYO Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO Semiconductor representative nearest you before using any SANYO Semiconductor products described or contained herein in such applications.

■ SANYO Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor products described or contained herein.

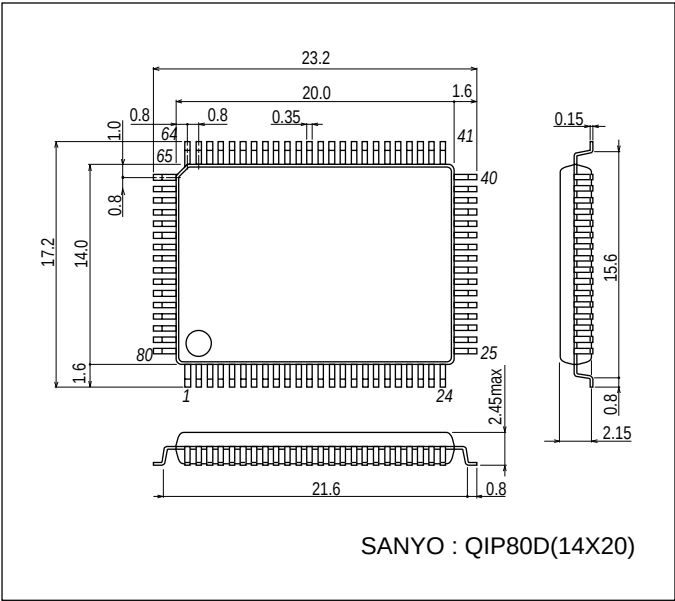
SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

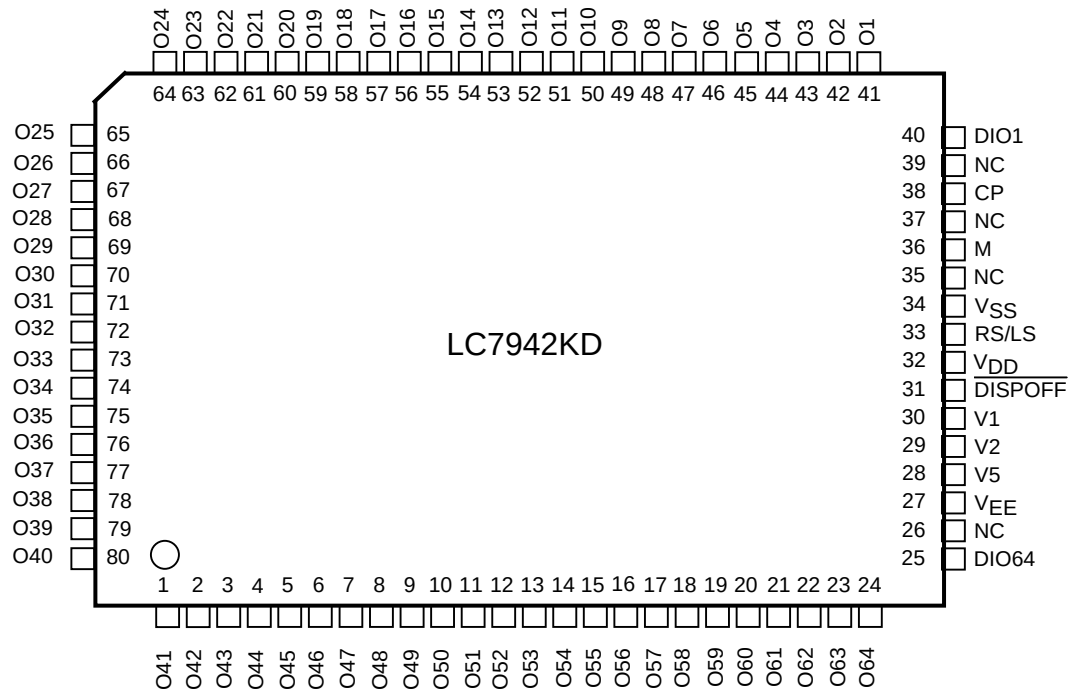
LC7942KD

Package Dimensions

unit: mm (typ)
3177

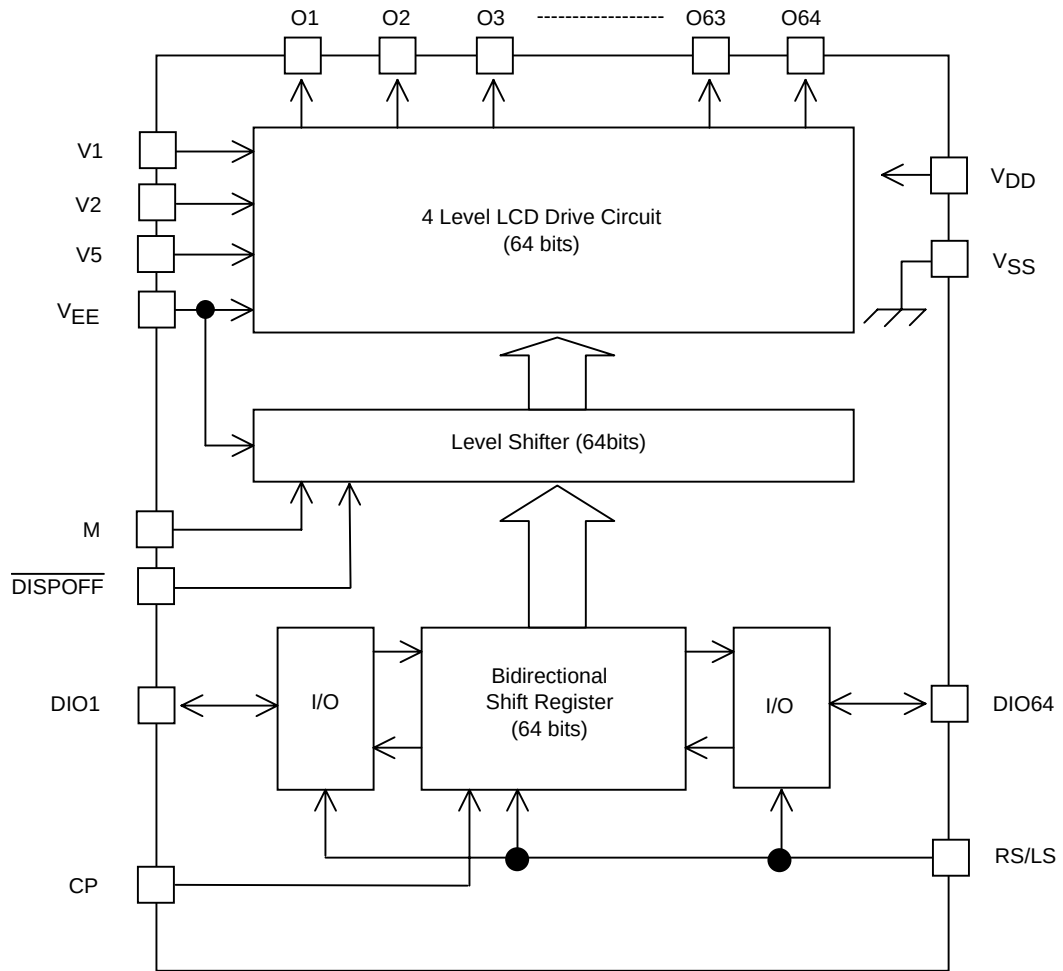


Pin Assignment



Top view

Block Diagram



LC7942KD

Pin Function

Pin No.	Pin name	Input/Output	Functions																											
32	V _{DD}	Supply	V _{DD} -V _{SS} is the logic supply. V _{DD} -V _{EE} is the LCD supply.																											
34	V _{SS}																													
27	V _{EE}																													
30	V1	Supply	LCD panel drive voltage supplies. V1 and V _{EE} are selected levels. V2 and V5 are non-selected levels.																											
29	V2																													
28	V5																													
38	CP	I	Display data input clock (falling-edge trigger).																											
40	DIO1	I/O	<table><tr><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO64</th></tr><tr><td>L (right shift)</td><td>O1→O64</td><td>IN</td><td>OUT</td></tr><tr><td>H (left shift)</td><td>O64→O1</td><td>OUT</td><td>IN</td></tr></table>				RS/LS	Data Transfer Direction	DIO1	DIO64	L (right shift)	O1→O64	IN	OUT	H (left shift)	O64→O1	OUT	IN												
RS/LS	Data Transfer Direction	DIO1					DIO64																							
L (right shift)	O1→O64	IN					OUT																							
H (left shift)	O64→O1	OUT	IN																											
25	DIO64	I/O																												
33	RS/LS	I																												
36	M	I	LCD panel drive voltage alternating control signal.																											
31	<u>DISPOFF</u>	I	O1 to O64 output control input pins.																											
41 to 80	O1 to O40	Output	LCD drive outputs The output drive level is determined by the display data, M signal and <u>DISPOFF</u> input as shown below. <table><tr><th>M</th><th>Data</th><th><u>DISPOFF</u></th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table> * Don't care (To be set to either "H" or "L")				M	Data	<u>DISPOFF</u>	Output	L	L	H	V2	L	H	H	V _{EE}	H	L	H	V5	H	H	H	V1	*	*	L	V1
M	Data						<u>DISPOFF</u>	Output																						
L	L						H	V2																						
L	H						H	V _{EE}																						
H	L						H	V5																						
H	H						H	V1																						
*	*						L	V1																						
1 to 24	O41 to O64																													
26	NC	-	No connection																											
35																														
37																														
39																														

Specifications

Absolute Maximum Ratings at $T_a=25\pm2^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (logic)	V_{DD} max	-	-0.3 to +7.0	V
Maximum supply voltage (LCD)	$V_{DD}-V_{EE}$ max	*1	0 to 22	V
Maximum input voltage	V_{IN} max	-	-0.3 to $V_{DD}+0.3$	V
Operating temperature range	T_{opr}	-	-20 to +85	$^\circ\text{C}$
Storage temperature range	T_{stg}	-	-40 to +125	$^\circ\text{C}$

Note *1 The voltages V_1 , V_2 , and V_5 must obey the relationships:

$$V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}, V_{DD}-V_2 \leq 7\text{V}, V_5-V_{EE} \leq 7\text{V}$$

Allowable Operating Ranges at $T_a = -20$ to 85°C , $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage (logic)	V_{DD}	-	2.7	-	5.5	V
Supply voltage (LCD)	$V_{DD}-V_{EE}$	*2, 3	8	-	20	V
Input high level voltage	V_{IH}	DIO1, DIO64, CP, M, RS/LS, $\overline{\text{DISPOFF}}$	$0.8V_{DD}$	-	-	V
Input low level voltage	V_{IL}	DIO1, DIO64, CP, M, RS/LS, $\overline{\text{DISPOFF}}$	-	-	$0.2V_{DD}$	V
CP (Shift clock)	f_{CP}	CP	-	-	1	MHz
CP (pulse width)	t_{WC}	CP	125	-	-	ns
Setup time	t_{SETUP}	DIO1 $\rightarrow$ CP, DIO64 $\rightarrow$ CP	100	-	-	ns
Hold time	t_{HOLD}	DIO1 $\rightarrow$ CP, DIO64 $\rightarrow$ CP	100	-	-	ns
CP rise time	t_R	CP	-	-	50	ns
CP fall time	t_F	CP	-	-	50	ns

Note *2 The voltages V_1 , V_2 , and V_5 must obey the relationships:

$$V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}, V_{DD}-V_2 \leq 7\text{V}, V_5-V_{EE} \leq 7\text{V}$$

*3 When applying power, apply power to the LCD drive block after applying power to the logic block or apply power to both the blocks simultaneously. When turning off power, turn off power to the logic block after turning off power to the LCD drive block or turn off power to both the blocks simultaneously.

LC7942KD

Electrical Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 2.7$ to 5.5V

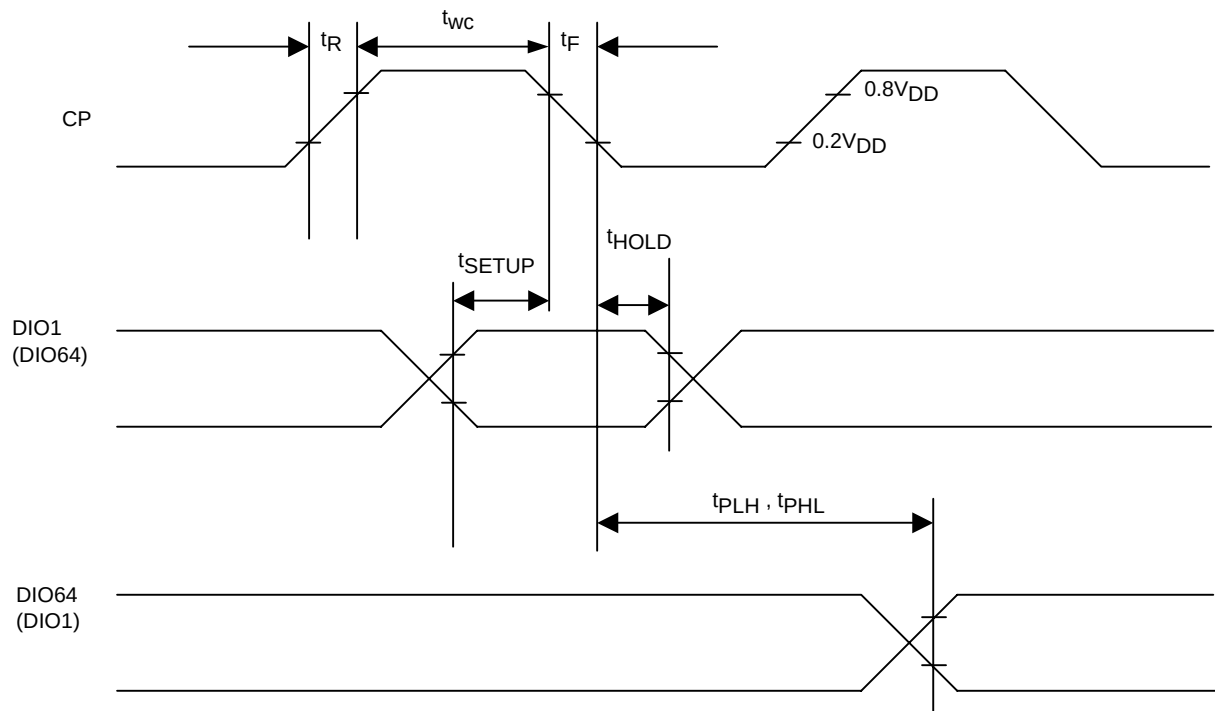
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level current	I_{IH}	$V_{IN} = V_{DD}$, $V_{DD} = 5.5\text{V}$, DIO1, DIO64, CP, M, RS/LS, DISPOFF	-	-	1	μA
Input low level current	I_{IL}	$V_{IN} = V_{SS}$, $V_{DD} = 5.5\text{V}$, DIO1, DIO64, CP, M, RS/LS, DISPOFF	-1	-	-	μA
Output high level voltage	V_{OH}	$I_{OH} = -0.4\text{mA}$, DIO1, DIO64	$V_{DD}-0.4$	-	-	V
Output low level voltage	V_{OL}	$I_{OL} = 0.4\text{mA}$, DIO1, DIO64	-	-	0.4	V
Driver on resistance	R_{ON}	$V_{DD}-V_{EE} = 18\text{V}$, $ V_{DE}-V_{OL} = 0.25\text{V}$ $V_{DD} = 4.5\text{V}$ *4; O1 to O64	-	-	1.5	$\text{k}\Omega$
V_{DD} static Current	I_{DD}	$V_{DD}-V_{EE} = 18\text{V}$, CP = V_{DD}	-	-	100	μA

Note *4 $V_{DE} = V_1$ or V_2 or V_5 or V_{EE} , $V_1 = V_{DD}$, $V_2 = 10/11(V_{DD}-V_{EE})$, $V_5 = 1/11(V_{DD}-V_{EE})$

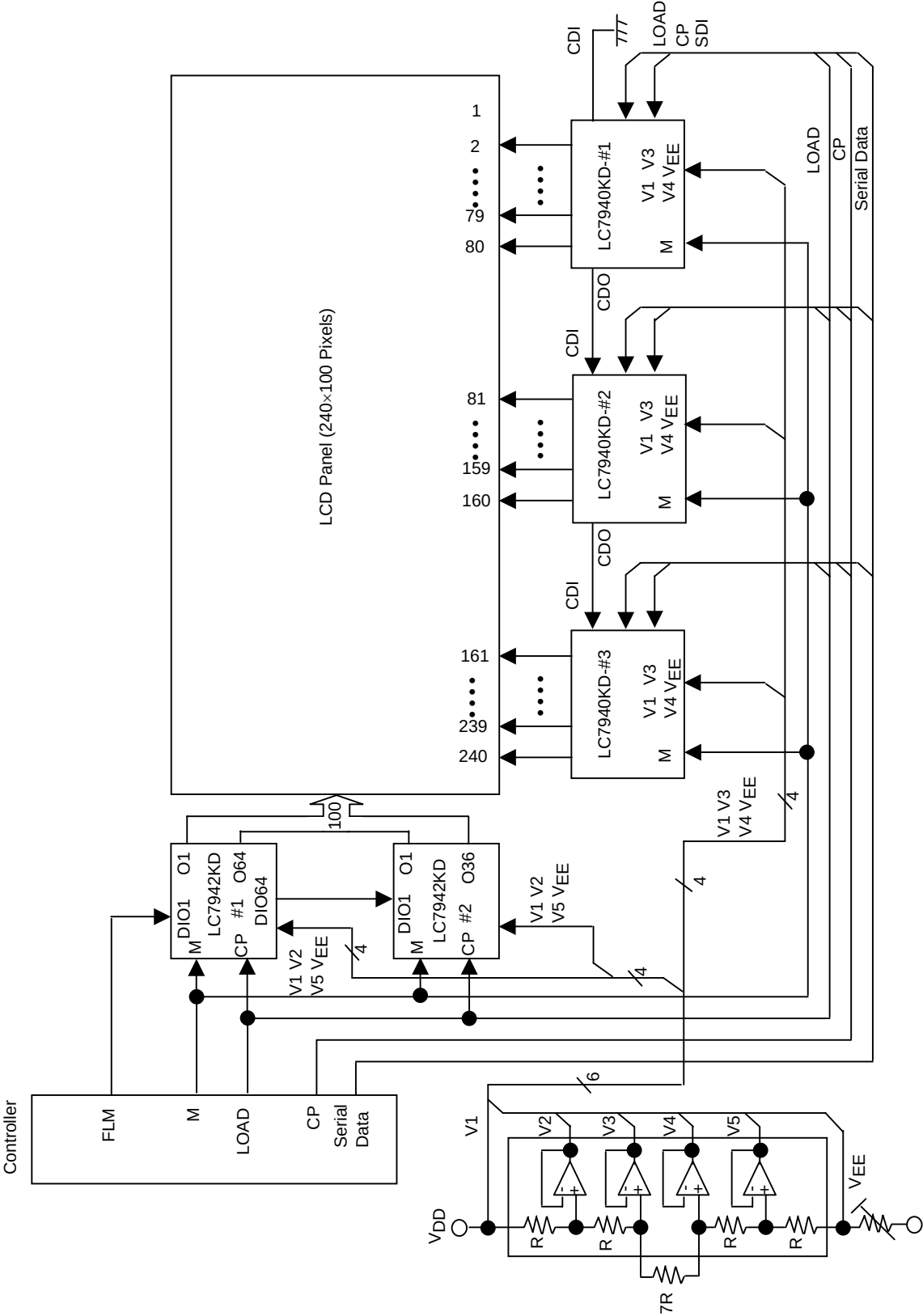
Switching Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 2.7$ to 5.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output delay time	t_{PLH}	$CL=30\text{pF}$; CP→DIO1, CP→DIO64	-	-	250	ns
	t_{PHL}	$CL=30\text{pF}$; CP→DIO1, CP→DIO64	-	-	250	ns

Switching Characteristics Diagram



Application Notes LCD Panel



- Specifications of any and all SANYO Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Semiconductor Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Semiconductor Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of November, 2006. Specifications and information herein are subject to change without notice.