National Semiconductor

PRELIMINARY
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LM3370
Dual Synchronous Step-Down DC-DC Converter with Dynamic Voltage Scaling Function

General Description

LM3370 is a dual step-down DC-DC converter optimized for powering an ultra-low voltage circuits from a single Li-Ion battery and input rail ranging from 2.7V to 5.5V. It provides two outputs with 600mA load per channel. The output voltage range varies from 1V to 3.3V and can be dynamically controlled using the I^2C compatible interface. This dynamic voltage scaling function allows processors to achieve maximum performance at the lowest power level. The I^2C compatible interface can also be used to control auto PFM-PWM/PWM mode selection and other performance enhancing features.

The LM3370 offers superior features and performance for portable systems with complex power management requirements. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system efficiency. Internal synchronous rectification enhances the converter efficiency without the use of futher external device.

There is a power-on-reset function that monitors the level of the output voltage to avoid unexpected power losses. The independent enable pin for each output allows for simple and effective power sequencing.

LM3370 is available in a 4mm by 5mm 16-lead non-pullback LLP package. A high switching frequency — 2MHz (typ) — allows use of tiny surface-mount components including a 2.2µH inductor.

Default fixed voltages for the 2 voltage outputs can be customized to fit system requirements by contacting National Semiconductor Corporation.

Features

- I^2C compatible interface
  - — V_{OUT1} = 1V to 2V in 50mV steps
  - — V_{OUT2} = 2.3V to 3.3V in 100mV steps
  - — Automatic PFM/PWM mode switching & Forced PWM mode for low noise operation
  - — Spread Spectrum capability using I^2C
- 600mA load per channel
- 2MHz PWM fixed switching frequency (typ.)
- Internal synchronous rectification for high efficiency
- Internal soft start
- Power-on-reset function for both outputs
- $2.7V \le V_{IN} \le 5.5V$
- Operates from a single Li-Ion cell or 3 cell NiMH/NiCd batteries and 3.3V/5.5V fixed rails
- 2.2µH Inductor, 4.7µF Input and 10µF Output Capacitor per channel
- 16-lead LLP Package (4mm x 5mm x 0.8mm)

Applications

- Baseband Processors
- Application Processors (Video, Audio)
- I/O Power
- FPGA Power and CPLD

Typical Application

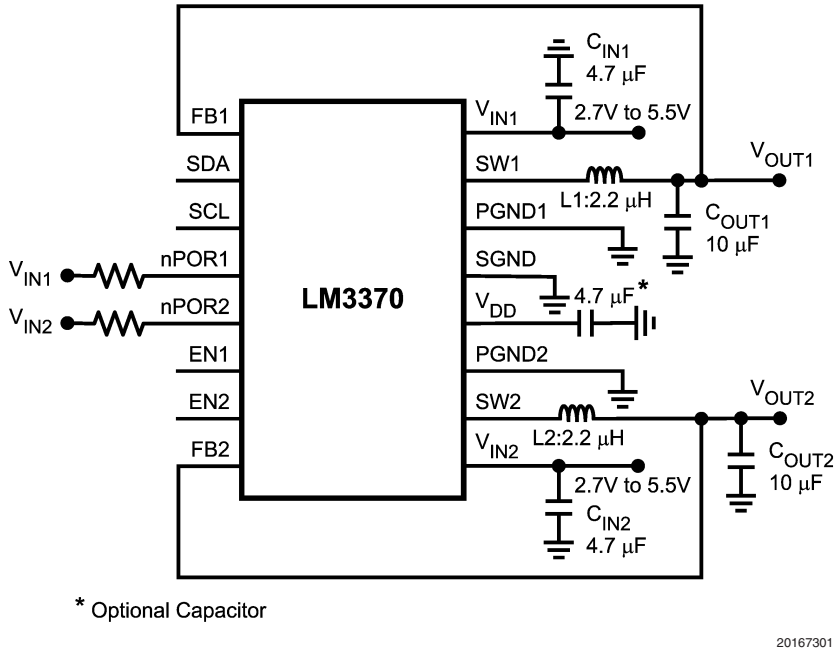

FIGURE 1. Typical Application Circuit

Functional Block Diagram

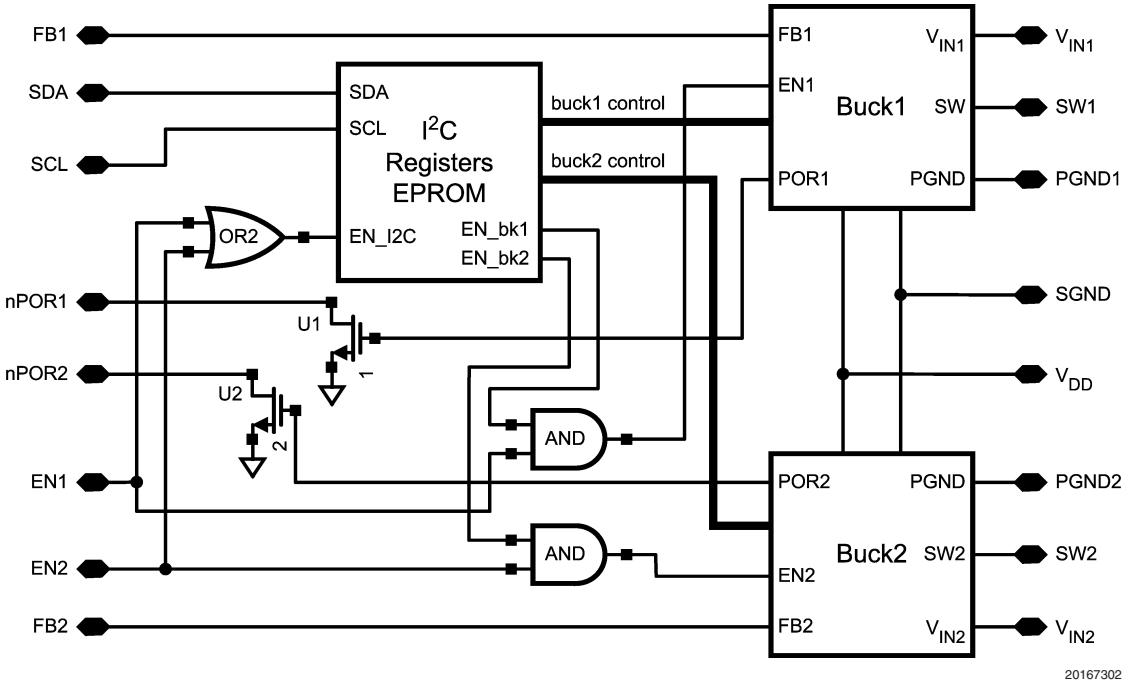

FIGURE 2. Functional Diagram

Package Marking Information

16-Lead LLP Package

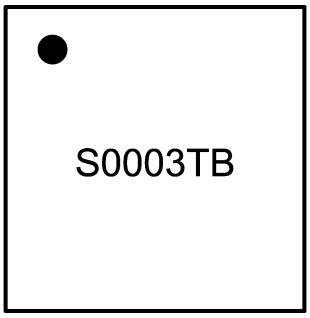

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FIGURE 3. Top Marking

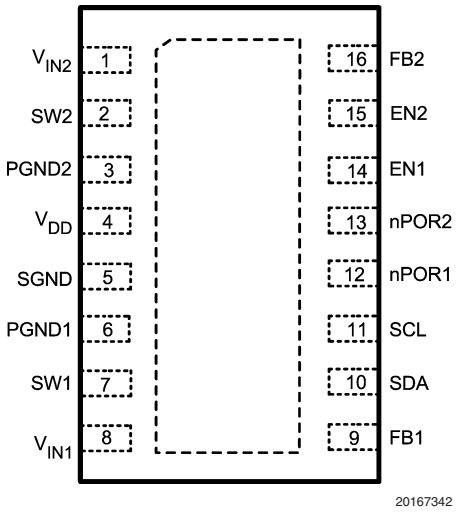

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FIGURE 4. Top View

Pin Descriptions

Pin #	Name	Description
1	V_{IN2}	Main Battery Power Input for Buck 2
2	SW2	Buck 2 Switch Pin
3	PGND2	Buck 2 Power Ground
4	V_{DD}	Analog and Digital V_{DD} Battery Input
5	SGND	Analog GND
6	PGND1	Buck 1 Power Ground
7	SW1	Buck 1 Switch Pin
8	V_{IN1}	Main Battery Power Input for Buck 1
9	FB1	Analog Feedback Input for Buck 1
10	SDA	I^2C Compatible Data, a 2 kΩ pull up resistor is required.
11	SCL	I^2C Compatible Clock, a 2 kΩ pull up resistor is required.
12	nPOR1	Power ON Reset for Buck 1, Open drain output Low when Buck 1 output is 92% of target output. A 100 kΩ pull up resistor is required
13	nPOR2	Power ON Reset for Buck 2, Open drain output Low when Buck 2 output is 92% of target output. A 100 kΩ pull up resistor is required
14	EN1	Buck 1 Enable
15	EN2	Buck 2 Enable
16	FB2	Analog feedback for Buck 2

I^2C Controlled Features

Features	Parameter	Comments
Output Voltage	V_{OUT1} & V_{OUT2}	Output voltage is controlled via I^2C compatible
Modes	Buck 1 & Buck 2	Mode can be controlled via I^2C compatible by either forcing device in Auto mode or forced PWM mode
Spread Spectrum	Buck 1 & Buck 2	Spread Spectrum capability via I^2C compatible for noise reduction

Ordering Information

Order Number	Voltage Option	Package Marking	Supplied As
LM3370SD-3013*	1.2V & 2.5V		250 units, Tape-and-Reel
LM3370SDX-3013*			3000 units, Tape and Reel
LM3370SD-3021	1.2V & 3.3V	S0003TB	250 units, Tape-and-Reel
LM3370SDX-3021		S0003TB	3000 units, Tape-and-Reel
LM3370SD-3416*	1.4V & 2.8V		250 units, Tape-and-Reel
LM3370SDX-3416*			3000 units, Tape-and-Reel
LM3370SD-4221*	1.8V & 3.3V		250 units, Tape-and-Reel
LM3370SDX-4221*			3000 units, Tape-and-Reel

Note the LM3370SD-3013 has the following default output voltages where V_{OUT1} = 1.2V & V_{OUT2} = 2.5V

* Contact National Semiconductor for availability

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN1} , V_{IN2} VDD to PGND & SGND	–0.2V to 6V
PGND to SGND	-0.2V to +0.2V
SDA, SCL, EN, EN2, nPOR1, nPOR2, SW1, SW2, FB1 & FB2	(GND - 0.2) to (V_{IN} + 0.2V)
Maximum Continuous Power Dissipation (P_{D_MAX}) (Note 3)	Internally Limited
Junction Temperature ($T_{J\text{-}MAX}$)	125˚C
Storage Temperature Range	–65˚C to +150˚C
Maximum Lead Temperature (Soldering)	(Note 4)
ESD Ratings (Note 5)	
All Pins	2 kV HBM 200V MM

Operating Ratings (Notes 1, 2)

Input Voltage Range ((Note 10))	2.7V to 5.5V
Recommended Load Current Per Channel	0mA to 600mA
Junction Temperature (T_J) Range	–30˚C to +125˚C
Ambient Temperature (T_A) Range (Note 6)	–30˚C to +85˚C

Thermal Properties (Note 7)

Junction-to-Ambient Thermal Resistance (θ_{JA})	26˚C/W

Electrical Characteristics (Notes 2, 8, 10)

Typical limits appearing in normal type apply for T_J = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range (T_A = T_J = –30˚C to +85˚C). Unless otherwise noted, V_{IN1} = V_{IN2} = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	(Note 11)	**-3.5**		**+3.5**	%
V_{OUT}	Line Regulation	2.7V ≤ V_{IN} ≤ 5.5V I_O = 10mA, V_{OUT} = 1.8V		0.031		%/V
	Load Regulation	100mA ≤ I_O ≤ 600mA V_{IN} = 3.6V, V_{OUT} = 1.8V		0.0013		%/mA
I_Q PFM	Quiescient Current “On”	PFM Mode, Both Bucks ON		34		µA
I_Q SD	Quiescient Current “Off”	EN1 = EN2 = 0V		0.2	**3**	µA
I_{LIM}	Peak Switching Current Limit	V_{IN} = 3.6V	**850**	1200	**1400**	mA
R_{DS_ON}	PFET	V_{IN} = 3.6V, I_{SW} = 200mA		390	500	mΩ
	NFET	V_{IN} = 3.6V, I_{SW} = 200mA		240	350	
F_{OSC}	Internal Oscillator Frequency		**1.5**	2.0	**2.4**	MHz
I_{EN}	Enable (EN) Input Current			0.01	**1**	µA
V_{IL}	Enable Logic Low				**0.4**	V
V_{IH}	Enable Logic High		**1.0**			V
POWER ON RESET THRESHOLD/FUNCTION (POR)						
nPOR1 & nPOR2 Delay Time	nPOR1 = Power ON Reset for Buck 1 nPOR2 = Power ON Reset for Buck 2	50 mS (default) Can be pre-trimmd to 50 uS, 100 mS & 200 mS		50		mS
POR Threshold	Percentage of Target V_{OUT}	V_{OUT} Rising		94		%
		V_{OUT} Falling, 85% (default), Can be pre-trimmed to 70% or 94%		85		

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. The thermal shutdown engages at T_J = 150˚C (typ.) and disengages at T_J = 140˚C(typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (LLP) (AN-1187).

Note 5: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin. (EAIJ)

Electrical Characteristics (Notes 2, 8, 10)Typical limits appearing in normal type apply for T_J = 25˚C. Limits appearing in boldface type apply over the entire junction temperature range (T_A = T_J = −30˚C to +85˚C). Unless otherwise noted, V_{IN1} = V_{IN2} = 3.6V. (Continued)

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 7: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2 x 1 array of thermal vias. Thickness of copper layers are 2/1/1/2oz.

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to *Application Note 1187: Leadless Leadframe Package (LLP)* and the *Power Efficiency and Power Dissipation* section of this datasheet.

Note 8: Min. and Max are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 9: Guaranteed by design.

Note 10: Input voltage range for all voltage options is 2.7V to 5.5V. The voltage range recommended for the specified output voltages:

V_{IN} = 2.7V to 5.5V for 1V ≤ V_{OUT} ≤ 1.7V and for V_{OUT} = 1.8V or greater, $V_{IN} = V_{OUT} + 1V$

or

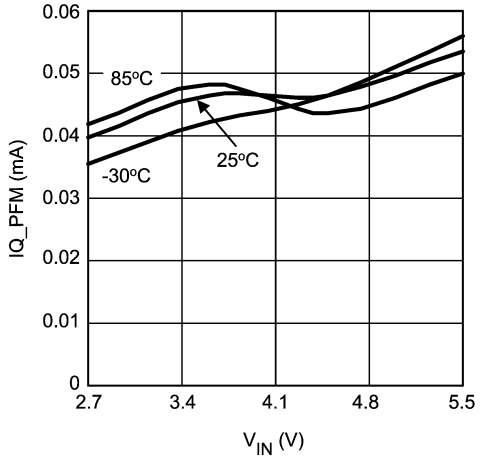
$V_{IN,MIN} = I_{LOAD} * (R_{DSON\_PFET} + R_{DCR\_INDUCTOR}) + V_{OUT}$

Note 11: Test condition: for V_{OUT} less than 2.5V, V_{IN} = 3.6V; for V_{OUT} greater than or equal to 2.5V, $V_{IN} = V_{OUT} + 1V$

Typical Performance Characteristics

LM3370, Circuit of Figure1, V_{IN} = 3.6V, V_{OUT1} = 1.5V & V_{OUT2} = 2.5V, L = 2,2µH (NR3015T2R2M), C_{IN} = 4.7µF (0805) and C_{OUT} = 10µF (0805) & T_A = 25˚C, unless otherwise noted.

IQ_PFM (Non Switching)
Both Channels



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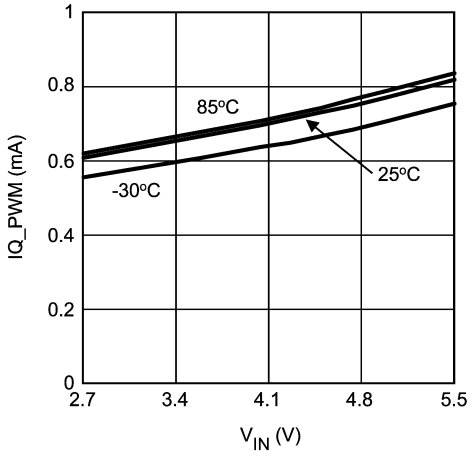
IQ_PWM (Non Switching)
Both Channels



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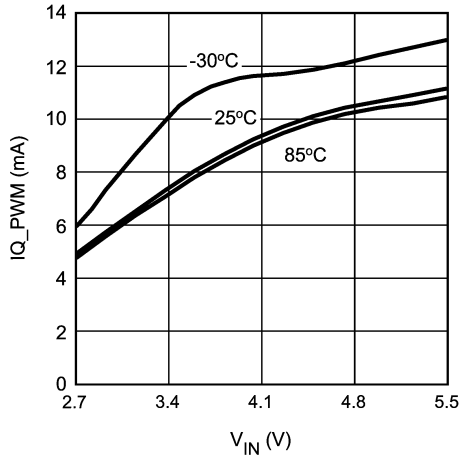
IQ_PWM (Switching)
Both Channels



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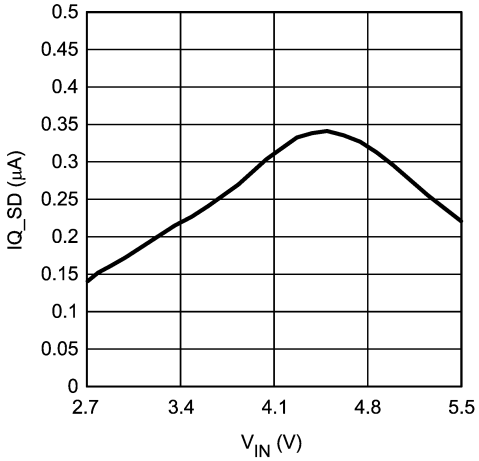
IQ_SD (EN1 = EN2 = 0V)©



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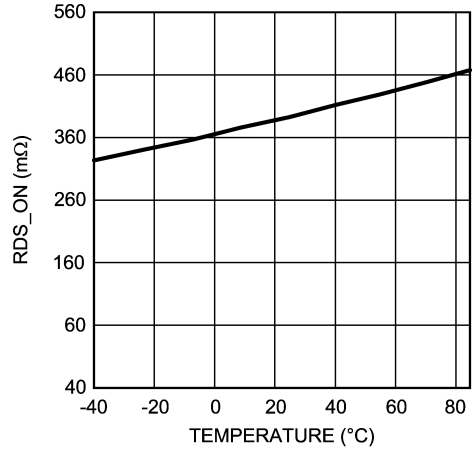
R_{DS_ON} (PFET) vs Temperature
V_{IN} = 3.6V



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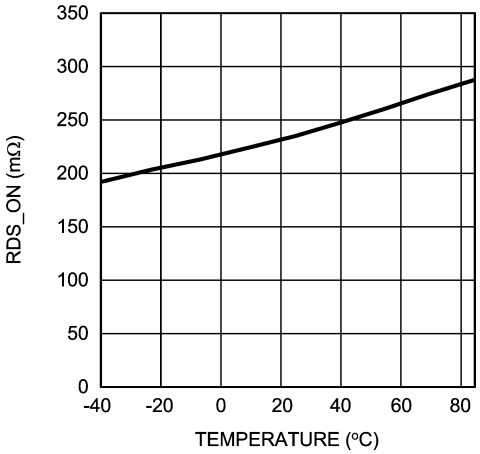
R_{DS_ON} (NFET) vs Temperature
V_{IN} = 3.6V



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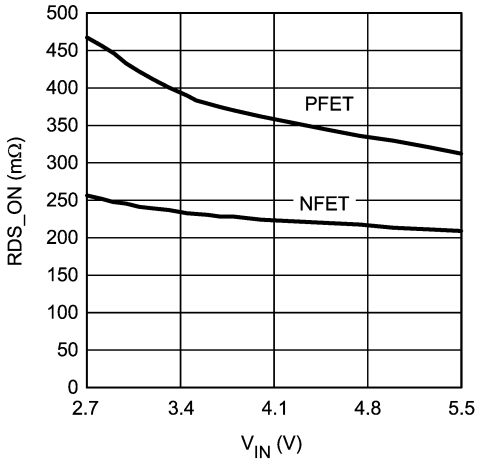
Typical Performance Characteristics

LM3370, Circuit of Figure1, V_{IN} = 3.6V, V_{OUT1} = 1.5V & V_{OUT2} = 2.5V, L = 2,2µH (NR3015T2R2M), C_{IN} = 4.7µF (0805) and C_{OUT} = 10µF (0805) & T_A = 25˚C, unless otherwise noted. (Continued)

R_{DS_ON} vs V_{IN}



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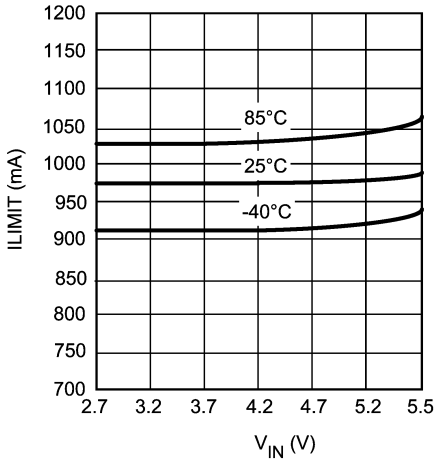
Current Limit vs V_{IN}



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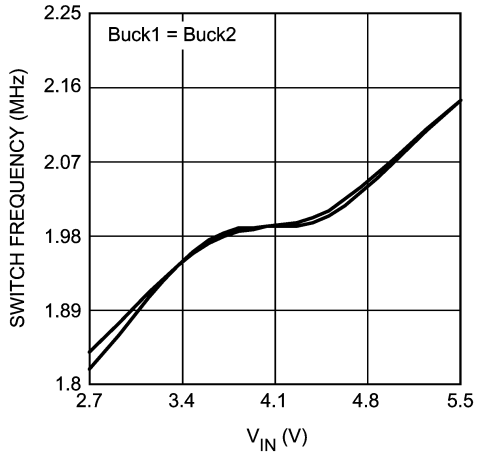
Switching Frequency vs V_{IN}



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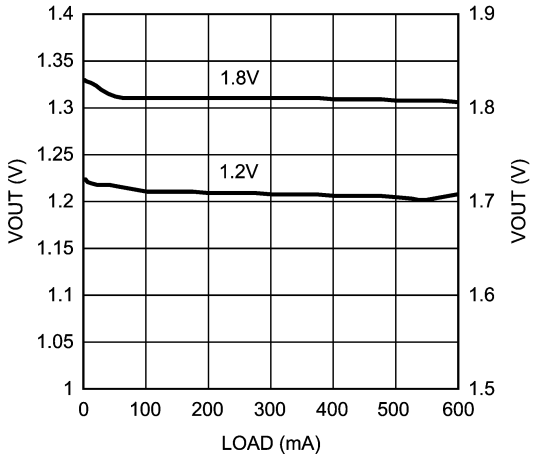
Output Voltage vs Output Current
V_{IN} = 3.6V (Forced PWM)



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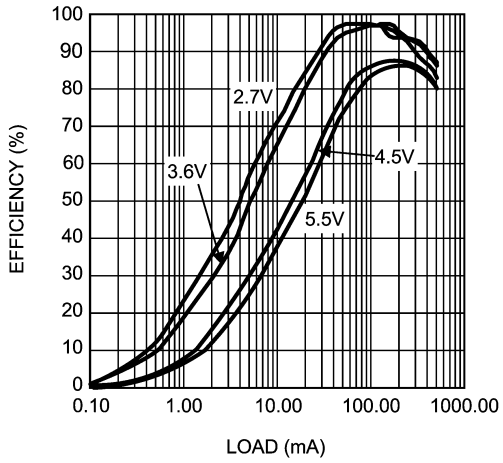
Efficiency vs Output Current
Forced PWM Mode, V_{OUT1} = 1.2V



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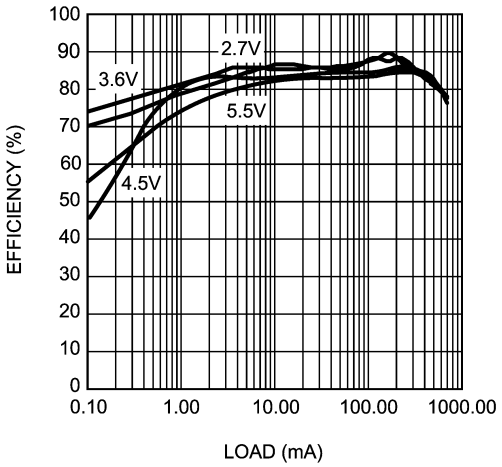
Efficiency vs Output Current
Auto Mode, V_{OUT1} = 1.2V



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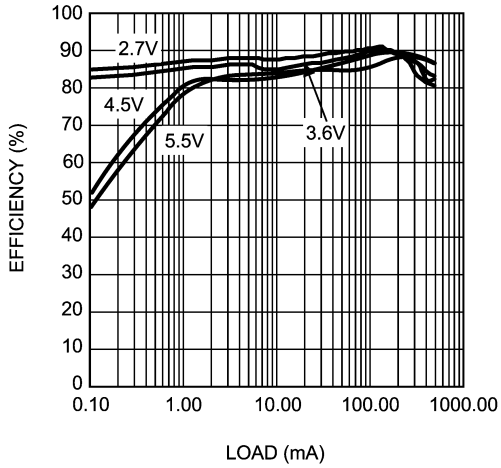
Typical Performance Characteristics

LM3370, Circuit of Figure1, V_{IN} = 3.6V, V_{OUT1} = 1.5V & V_{OUT2} = 2.5V, L = 2,2µH (NR3015T2R2M), C_{IN} = 4.7µF (0805) and C_{OUT} = 10µF (0805) & T_A = 25˚C, unless otherwise noted. (Continued)

Efficiency vs Output Current
Auto Mode, V_{OUT1} = 1.8V



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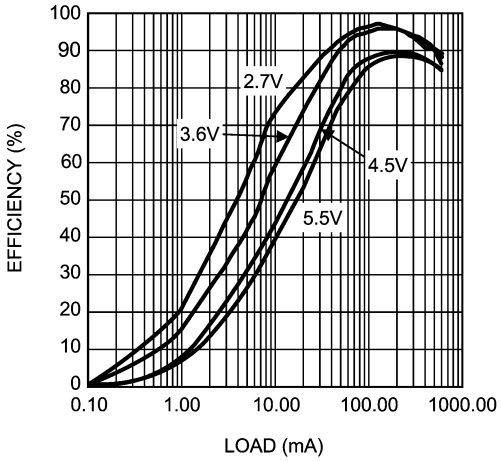
Efficiency vs Output Current
Forced PWM Mode, V_{OUT1} = 1.8V



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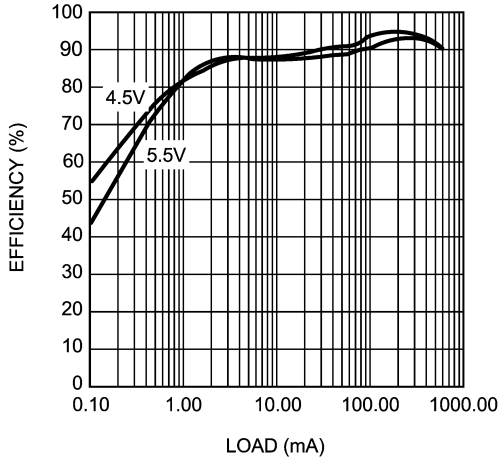
Efficiency vs Output Current
Auto Mode, V_{OUT2} = 3.3V



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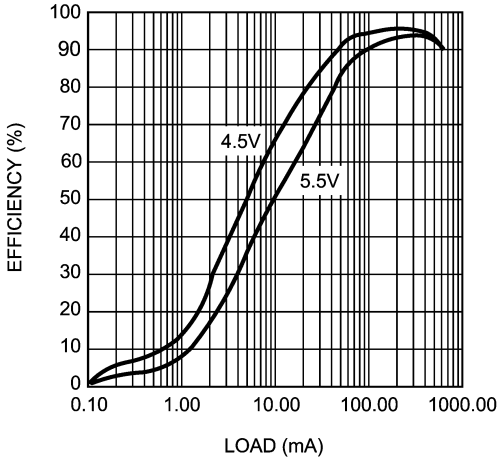
Efficiency vs Output Current
Forced PWM Mode, V_{OUT2} = 3.3V



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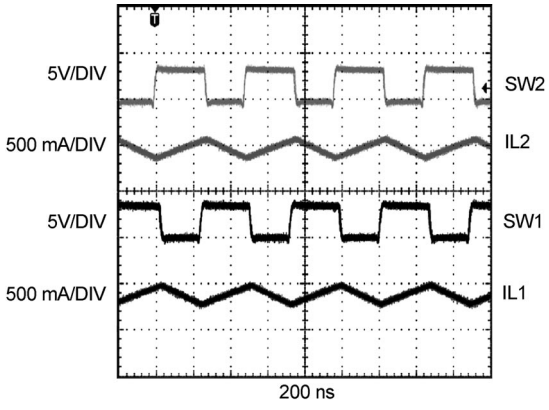
Typical Operation Waveform
V_{IN} = 3.6V, V_{OUT1} = 1.8V & V_{OUT2} = 1.8V
Load = 400mA



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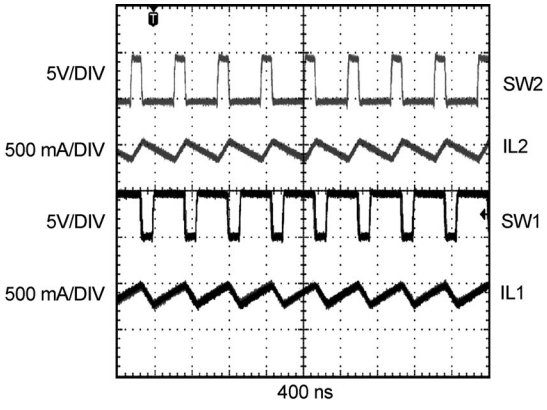
Typical Operation Waveform
V_{IN} = 4.8V, V_{OUT1} = 1V & V_{OUT2} = 3.3V
Load = 400mA



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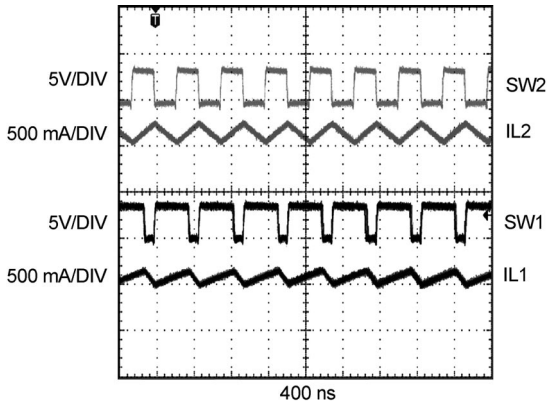
Typical Performance Characteristics

LM3370, Circuit of Figure1, V_{IN} = 3.6V, V_{OUT1} = 1.5V & V_{OUT2} = 2.5V, L = 2,2µH (NR3015T2R2M), C_{IN} = 4.7µF (0805) and C_{OUT} = 10µF (0805) & T_A = 25˚C, unless otherwise noted. (Continued)

Typical Operation Waveform
V_{IN} = 3.6V, V_{OUT1} = 1.5V, V_{OUT2} = 2.5V, Load = 600mA Each



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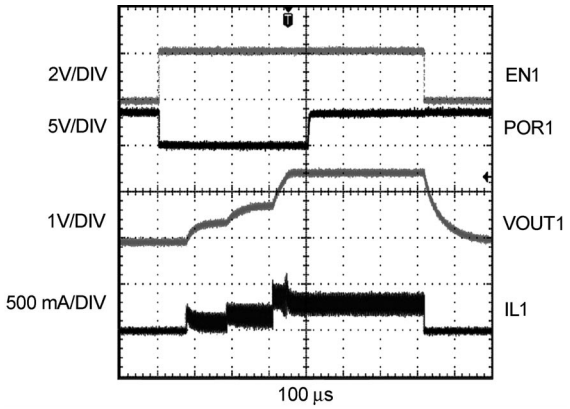
Start-up at PWM for BUCK1
(V_{IN} = 3.6V, V_{OUT} = 1.5V, Load = 200mA)



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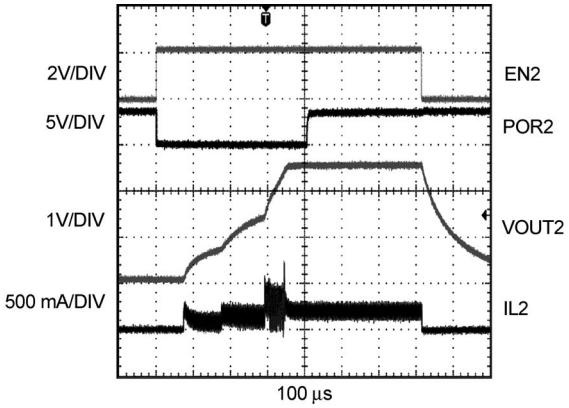
Start-up at PWM for BUCK2
(V_{IN} = 3.6V, V_{OUT} = 2.5V, Load = 200mA)



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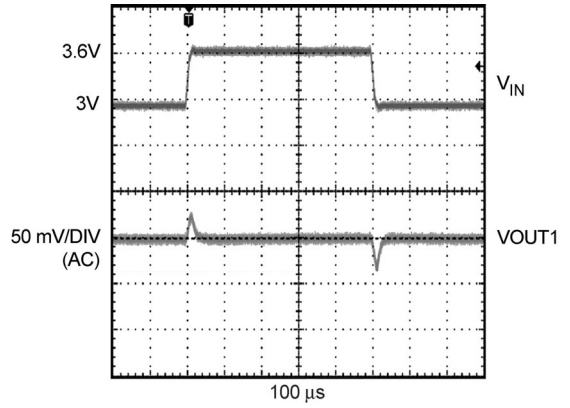
Line Transcient
(V_{OUT1} = 1.2V)



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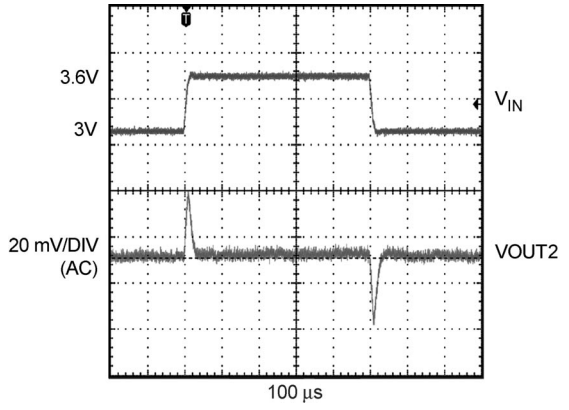
Line Transcient
(V_{OUT2} = 1.8V)



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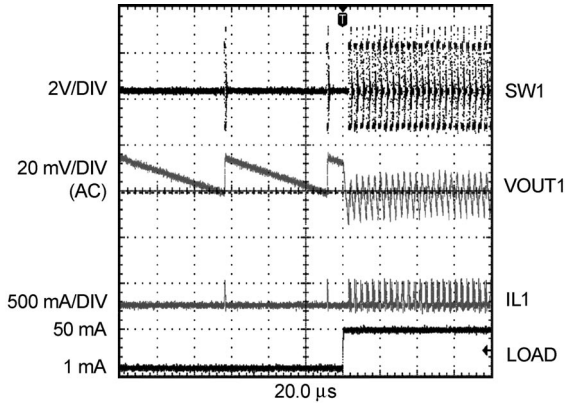
Load Transient in PFM MODE
(V_{OUT1} = 1.5V)



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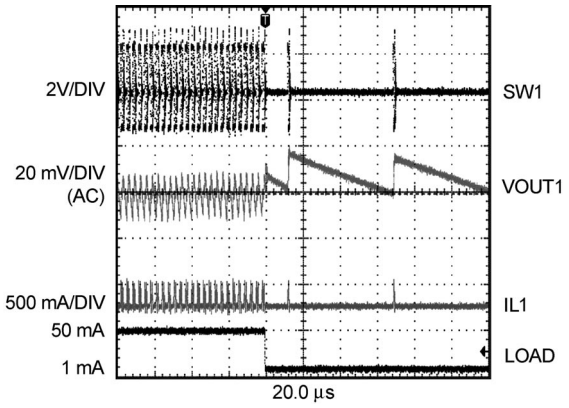
Typical Performance Characteristics

LM3370, Circuit of Figure1, V_{IN} = 3.6V, V_{OUT1} = 1.5V & V_{OUT2} = 2.5V, L = 2,2µH (NR3015T2R2M), C_{IN} = 4.7µF (0805) and C_{OUT} = 10µF (0805) & T_A = 25˚C, unless otherwise noted. (Continued)

Load Transient in PFM MODE (V_{OUT1} = 1.5V)



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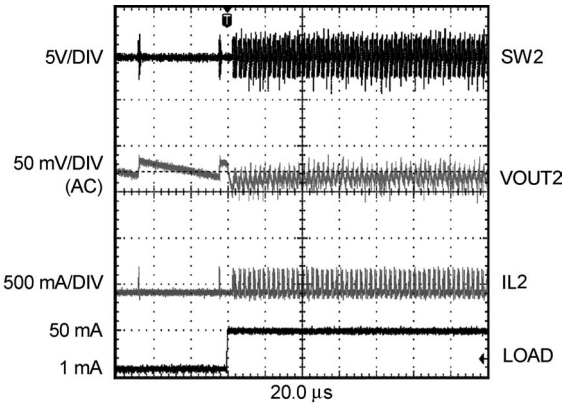
Load Transient in PFM MODE (V_{OUT1} = 1.8V)



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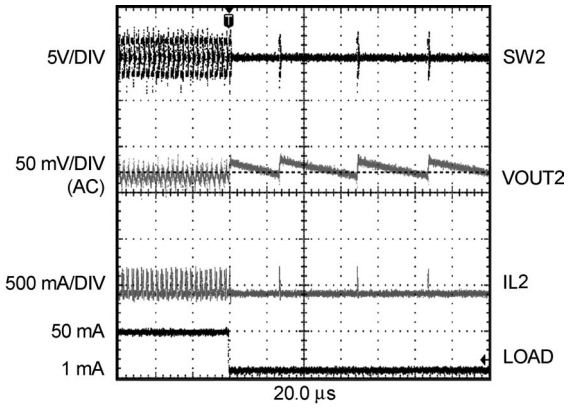
Load Transient in PFM MODE (V_{OUT1} = 1.8V)



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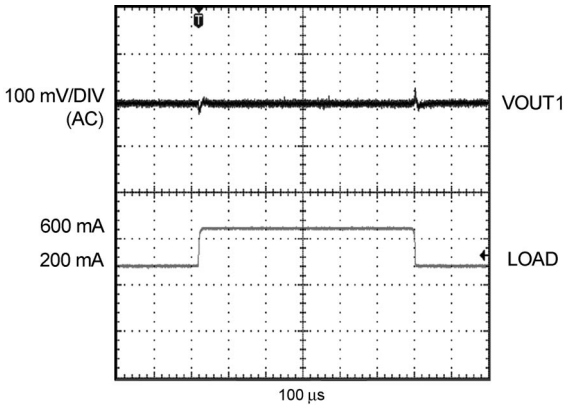
Load Transient in PWM MODE (V_{IN} = 3.6V, V_{OUT1} = 1.2V)



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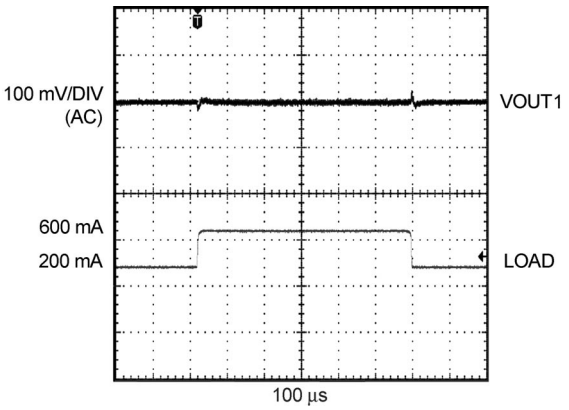
Load Transient in PWM MODE (V_{IN} = 3.6V, V_{OUT1} = 1.5V)



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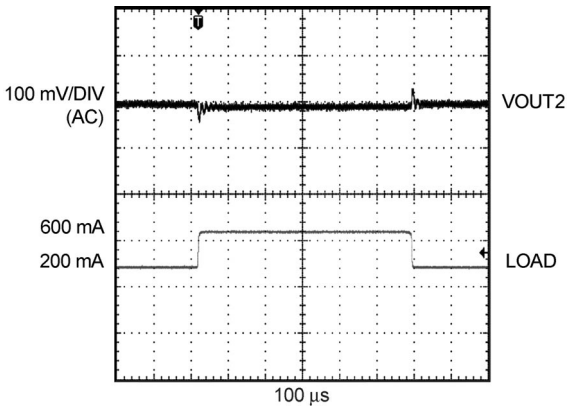
Load Transient in PWM MODE (V_{IN} = 3.6V, V_{OUT2} = 2.5V)

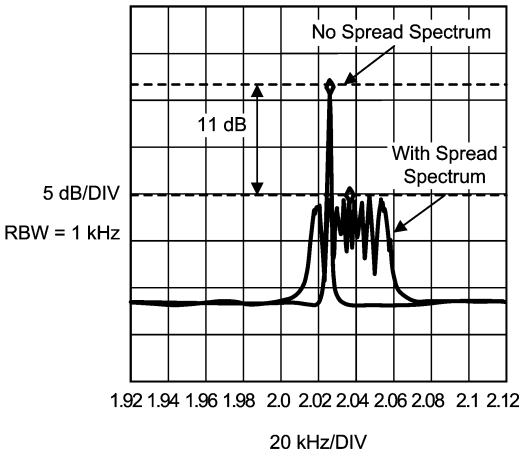


20167341

Typical Performance Characteristics

LM3370, Circuit of Figure1, V_{IN} = 3.6V, V_{OUT1} = 1.5V & V_{OUT2} = 2.5V, L = 2,2µH (NR3015T2R2M), C_{IN} = 4.7µF (0805) and C_{OUT} = 10µF (0805) & T_A = 25˚C, unless otherwise noted. (Continued)

Spread Spectrum Enabling
(V_{OUT} Signal at 2 MHz)



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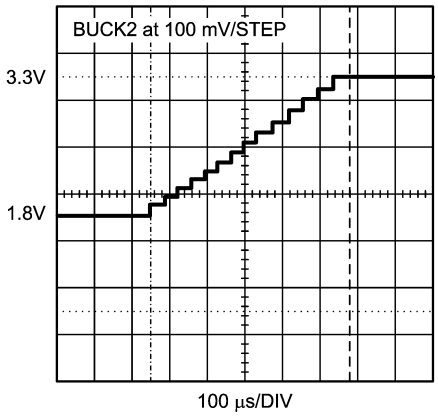
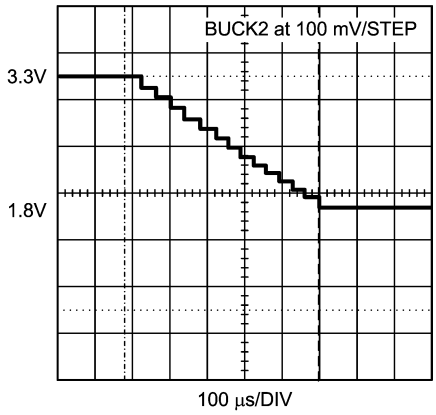
V_{OUT} Stepping
(From 1.8V to 3.3V)



20167371

V_{OUT} Stepping
(From 3.3V to 1.8V)



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Operation Description

DEVICE INFORMATION

The LM3370, a dual high efficiency step down DC-DC converter, delivers regulated voltages from input rails between 2.7V to 5.5V. Using voltage mode architecture with synchronous rectification, the LM3370 has the ability to deliver up to 600mA per channel. The performance is optimized for systems where efficiency and space are critical.

There are three modes of operation depending on the current required—PWM, PFM, and shutdown. PWM mode handles loads of approximately 70mA or higher with 90% efficiency or better. Lighter loads cause the device to automatically switch into PFM mode to maintain high efficiency with low supply current (I_Q = 20µA typ.) per channel.

The LM3370 can operate up to a 100% duty cycle (PFET switch always on) for low drop out control of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

Additional features include soft-start, under voltage lock out, current overload protection, and thermal overload protection.

CIRCUIT OPERATION

During the first portion of each switching cycle, the control block in the LM3370 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of

$$\frac{V_{IN} - V_{OUT}}{L}$$

by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of

$$\frac{-V_{OUT}}{L}$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the LM3370 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows the LM3370 to protect itself and external components during overload conditions. PWM mode implements cycle-by-cycle current limiting using an internal comparator that trips at 1200mA (typ.). If the outputs are shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions are true, for a duration of 32 or more clock cycles:

1. The NFET current reaches zero.
2. The peak PFET switch current drops below the I_{MODE} level .

$$\left(\text{Typically } I_{MODE} < 66\ mA + \frac{V_{IN}}{160\Omega}\right)$$

Supply current during this PFM mode is less than 20µA per channel, which allows the part to achieve high efficiency under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.2% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see *Figure 5*) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PFET power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is:

I_{PFM} = 115mA + $V_{IN}/57\Omega$

Once the PFET power switch is turned off, the NFET power switch is turned on until the inductor current ramps to zero. When the NFET zero-current condition is detected, the NFET power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see *Figure 5*), the PFET switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NFET switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode.

Operation Description (Continued)

FORCED PWM MODE

The LM3370 auto mode can be bypassed by forcing the device to operate in PWM mode, this can be implemented through the I^2C compatible interface; see Output Table on page 19.

SOFT-START

The LM3370 has a soft start circuit that limits in-rush current during start up. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.7V.

LDO - LOW DROP OUT OPERATION

The LM3370 can operate at 100% duty cycle (no switching, PFET switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. The minimum input voltage needed to support the output voltage is $V_{IN,MIN} = I_{LOAD}*(R_{DSON,PFET} + R_{INDUCTOR}) + V_{OUT}$

- I_{LOAD} load current
- $R_{DSON/PFET}$ drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ inductor resistance

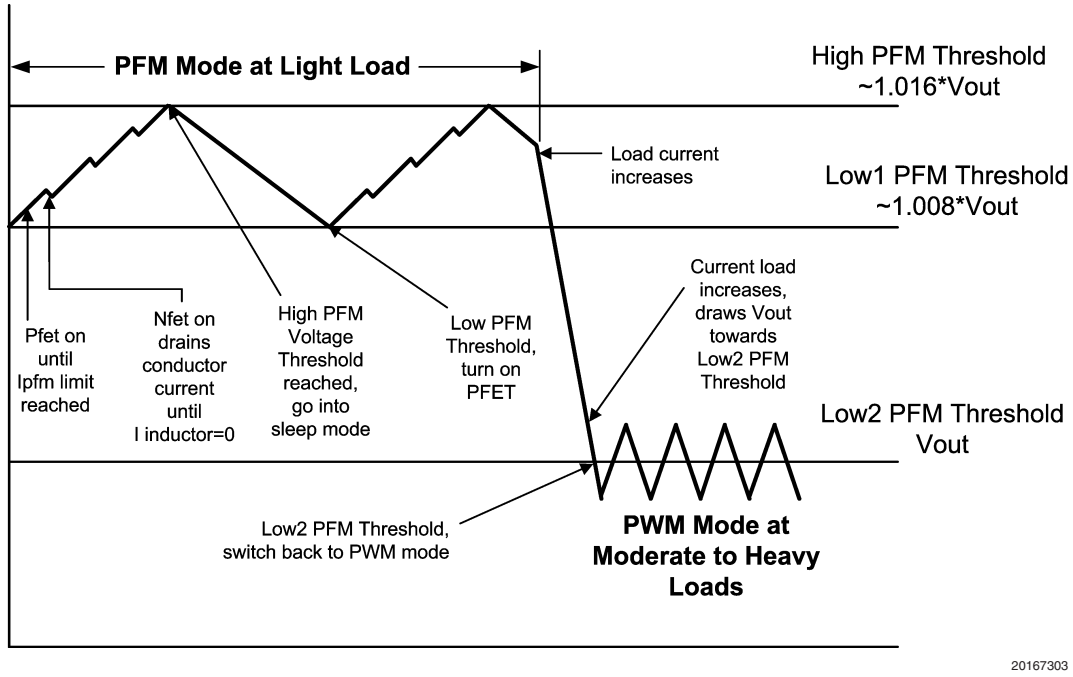


FIGURE 5. Operation in PFM Mode and Transfer to PWM Mode

I²C Compatible Interface Electrical Specifications

Unless otherwise noted, V_{BATT} = 2.7V to 5.5V. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −30˚C to +125˚C. (Notes 2, 8, 9)

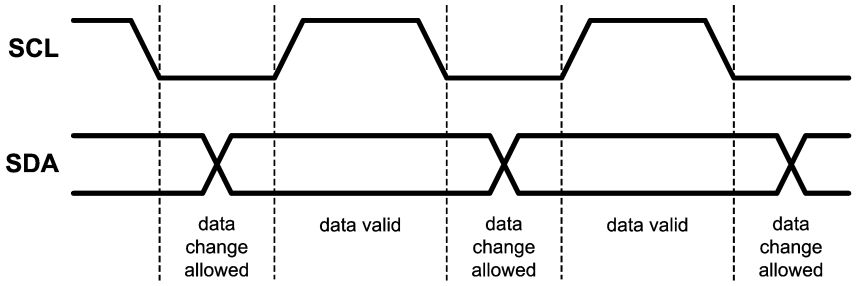
Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{CLK}	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time between Start and Stop	(Note 10)	**1.3**			µS
t_{HOLD}	Hold Time Repeated Start Condition	(Note 10)	**0.6**			µS
t_{CLKLP}	CLK Low Period	(Note 10)	**1.3**			µS
t_{CLKHP}	CLK High Period	(Note 10)	**0.6**			µS
t_{SU}	Set Up Time Repeated Start Condition	(Note 10)	**0.6**			µS
$t_{DATAHLD}$	Data Hold Time	(Note 10)	**200**			nS
t_{CLKSU}	Data Set Up Time	(Note 10)	**200**			nS
T_{SU}	Set Up Time for Start Condition	(Note 10)	**0.6**			µS
T_{TRANS}	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both DATA & CLK signals.	(Note 10)		50		nS
VDD_I²C	I²C Logic High Level		1		V_{IN}	V

I²C Compatible Interface

In I²C compatible mode, the SCL pin is used for the I²C clock and the SDA pin is used for the I²C data. Both these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistor are determined by the capacitance of the bus (typ. ~1.8k). Signal timing specifications are according to the I²C bus specification. Maximum frequency is 400 kHz.

I²C COMPATIBLE DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



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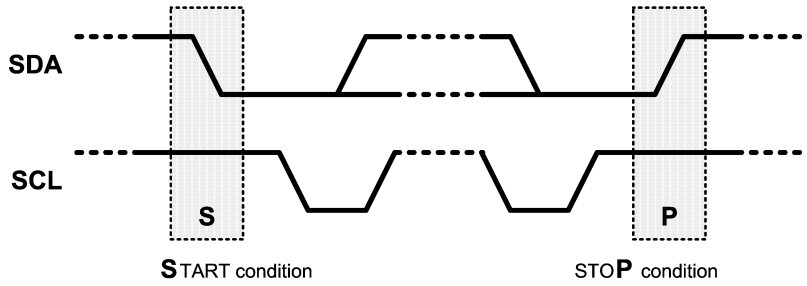
I²C COMPATIBLE START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



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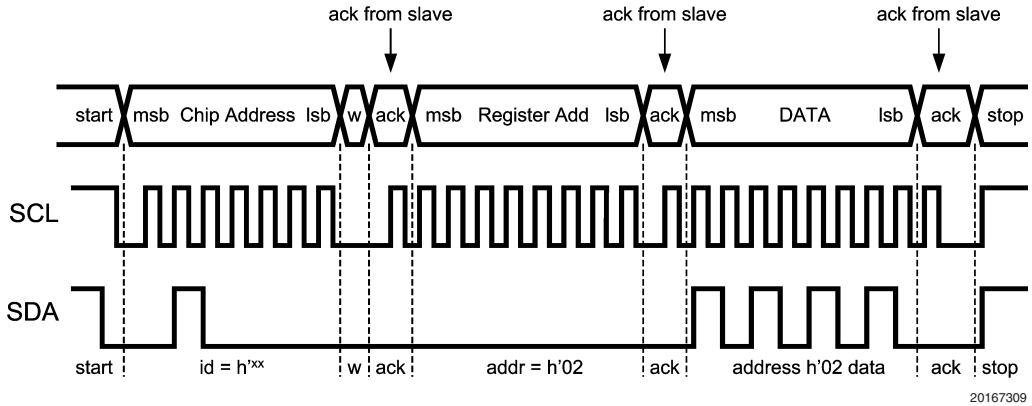
I²C Compatible Interface (Continued)

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

I²C Compatible Write Cycle



W = write (SDA = "0")

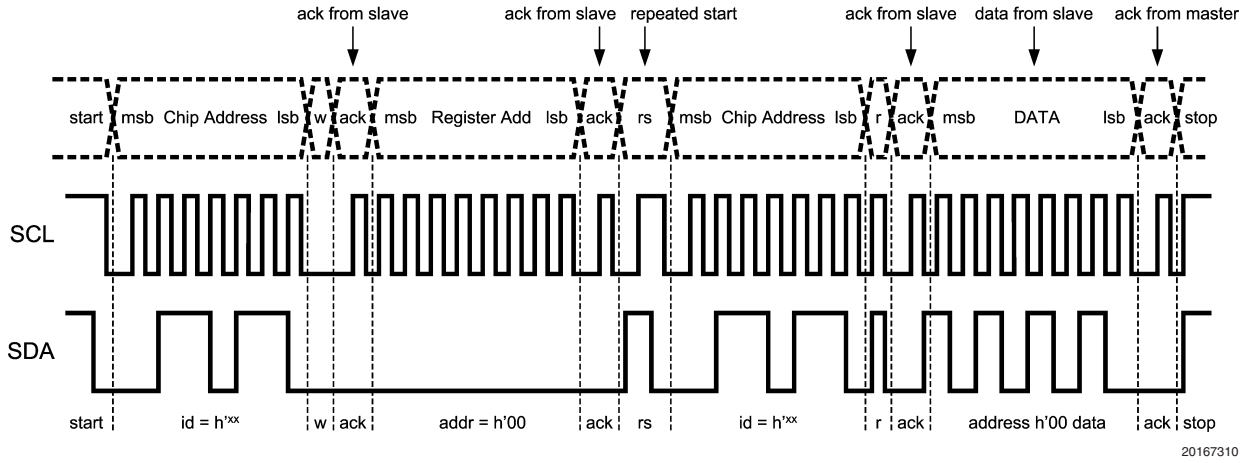
r = read (SDA = "1")

ack = acknowledge (SDA pulled down by either master or slave)

rs = repeated startxx=36h

However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the read cycle waveform.

I²C Compatible Read Cycle

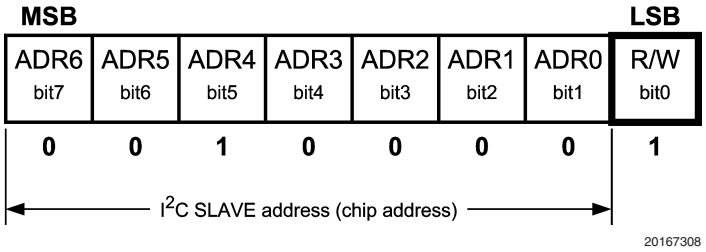


Device Register Information

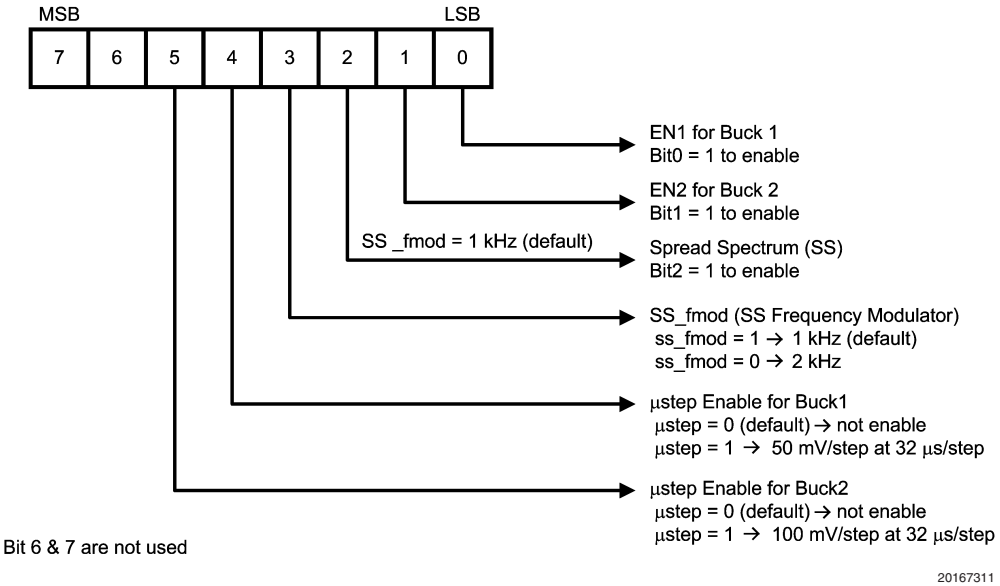
Register Information

Register Name	Location	Type	Function
Control	00	R/W	Control signal for Buck 1 and Buck 2
Buck 1	01	R/W	Output setting & Mode selection for Buck 1
Buck 2	02	R/W	Output setting & Mode selection for Buck 2 and POR disable

I²C CHIP ADDRESS INFORMATION



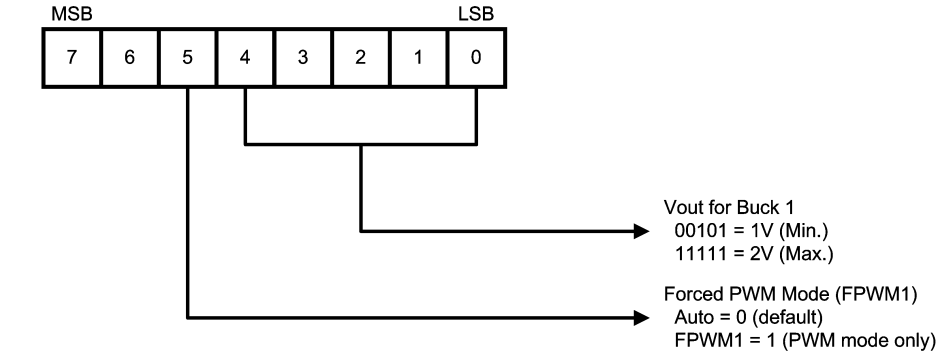
REGISTER 00



Device Register Information

(Continued)

REGISTER 01



Bit 6 and 7 are not used

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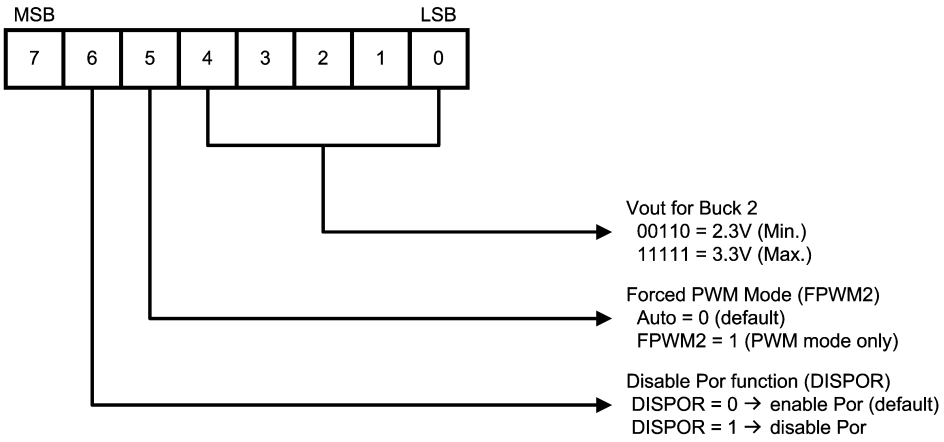
REGISTER 02



Bit 7 is not used

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Output Selection Table via I^2C Programing

Buck Output Voltage Selection Codes		
Data Code	**Buck_1 (V)**	**Buck_2 (V)**
00000	NA	NA
00001	NA	NA
00010	NA	NA
00011	NA	NA
00100	NA	NA
00101	1.00	NA
00110	1.05	2.3
00111	1.10	2.4
01000	1.15	2.5
01001	1.20	2.6
01010	1.25	2.7
01011	1.30	2.8
01100	1.35	2.9

Buck Output Voltage Selection Codes		
Data Code	**Buck_1 (V)**	**Buck_2 (V)**
01101	1.40	3.0
01110	1.45	3.1
01111	1.50	3.2
10000	1.55	3.3
10001	1.60	NA
10010	1.65	NA
10011	1.70	NA
10100	1.75	NA
10101	1.80	NA
10110	1.85	NA
10111	1.90	NA
11000	1.95	NA
11001	2.00	NA

Application Information

SETTING OUTPUT VOLTAGE VIA I²C Compatible

The outputs of the LM3370 can be programmed through Buck 1 & Buck 2 registers via I²C. Buck 1 output voltage can be dynamically adjusted between 1V to 2V in 50mV steps and Buck 2 output voltage can be adjusted between 2.3V to 3.3V in 100mV steps. Please refer to voltage selection table on page 19 for programming the desire output voltage. If the I²C compatible feature is not used, the default output voltage will be the pre-trimmed voltage. For example, LM3370SD-3021 refers to 1.2V for Buck 1 and 3.3V for Buck 2.

Micro-Stepping:

The Micro-Stepping feature minimizes output voltage overshoot/undershoot during large output transients or large iumps in output voltage. If Micro-stepping is enabled through I²C, the output voltage automatically ramps at 50mV per step for Buck 1 and 100mV per step for Buck 2. The steps are summarized as follow:

Buck 1: 50mV/step and 32µs/step

Buck 2: 100mV/step and 32µs/step

For example if changing Buck 1 voltage from 1V to 1.8V yields 20 steps [(1.8 - 1)/ 0.05 = 20]. This translates to 640µs [(20 x 32µs) = 640µs] needed to reach the final target voltage.

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple.

There are two methods to choose the inductor current rating.

method 1:

The total current is the sum of the load and the inductor ripple current. This can be written as

$$I_{MAX} = I_{LOAD} + \left(\frac{I_{RIPPLE}}{2}\right)$$

$$= I_{LOAD} + \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

- I_{LOAD} load current
- V_{IN} input voltage
- L inductor
- f switching frequency

method 2:

A more conservative approach is to choose an inductor that can handle the maximum current limit of 1400mA.

Given a peak-to-peak current ripple (I_{PP}) the inductor needs to be at least

$$L >= \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

A 2.2µH inductor with a saturation current rating of at least 1400mA is recommended for most applications. The inductor's resistance should be less than around 0.2Ω for good efficiency. *Table 1* lists suggested inductors and suppliers.

For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 4.7µF, 6.3V is sufficient for most applications. A larger value may be used for improved input voltage filtering. The input filter capacitor supplies current to the PFET switch of the LM3370 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with a surge current rating sufficient for the power-up surge from the input power source. The power-up surge current is approximately the capacitor's value (µF) times the voltage rise rate (V/µs).

The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case IRMS is:

$$I_{RMS} = \frac{I_{OUTMAX}}{2} \qquad \text{(duty cycle = 50\%)}$$

Below are some suggested inductor manufacturers include but are not limited to:

TABLE 1. Suggested Inductors and Suppliers

Model	Vendor	Dimensions (mm)	I_{SAT}
DO3314-222	Coilcraft	3.3 x 3.3 x 1.4	1.6A
LPO3310-222		3.3 x 3.3 x 1.0	1.1A
SD3114-2R2	Cooper	3.1 x 3.1 x 1.4	1.48A
NR3010T2R2M	Taiyo Yuden	3.0 x 3.0 x 1.0	1.1A
NR3015T2R2M		3.0 x 3.0 x 1.5	1.48A
VLF3010AT-2R2M1R0	TDK	2.6 x 2.8 x 1.0	1.0A

OUTPUT CAPACITOR SELECTION

DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. The output ripple current can be calculated as:

Voltage peak-to-peak ripple due to capacitance =

Application Information (Continued)

$$V_{PP-C} = \frac{I_{PP}}{f*8*C}$$

Voltage peak-to-peak ripple due to ESR = V_{PP-ESR} = $I_{PP}*R_{ESR}$

Voltage peak-to-peak ripple, root mean squared =

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2}$$

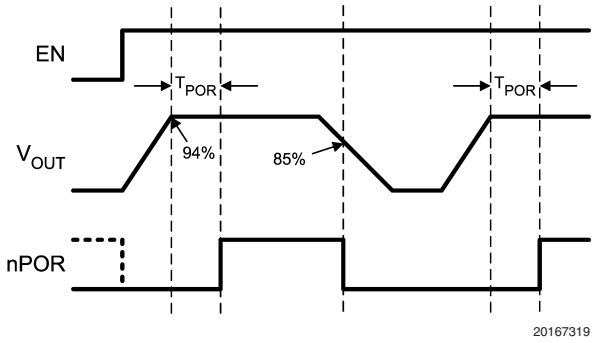
Note that the output ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent (as well as temperature dependent); make sure that the frequency of the R_{ESR} given is the same order of magnitude as the switching frequency.

TABLE 2. Suggested Capacitors and Their Suppliers

Model	Description	Case Size	Vendor
4.7µF for C_{IN}			
C1608X5R0J475	Ceramic, X5R, 6.3V Rating	0603	TDK
C2012X5R0J475	Ceramic, X5R, 6.3V Rating	0805	
JMK212BJ475	Ceramic, X5R, 6.3V Rating	0805	Taiyo Yuden
GRM21BR60J475	Ceramic, X5R, 6.3V Rating	0805	muRata
GRM219R60J-475KE19D	Ceramic, X5R, 6.3V Rating	0805(Thin) <1mm Height	
10µF C_{OUT}			
C2012X5R0J106	Ceramic, X5R, 6.3V Rating	0805	TDK
JMK212BJ106	Ceramic, X5R, 6.3V Rating	0805	Taiyo Yuden
GRM21BR60J106	Ceramic, X5R, 6.3V Rating	0805	muRata
GRM219R60J-106KE19D	Ceramic, X5R, 6.3V Rating	0805(Thin) < 1mm Height	

POR (POWER ON RESET)

The LM3370 has an independent POR functions (nPOR) for each buck converter. The nPOR1 and nPOR2 are open drain circuits which pull low when the outputs are below 94% (rising V_{OUT}) or 85% (falling V_{OUT}) of the desire output. The inherent delay between the output (at 94% of V_{OUT}) to the time at which the nPOR is enabled is about 50ms. A pull up resistor of 100kΩ at nPOR pin is required. Please refer to the electrical specification table for other timing options. The diagram below illustrates the timing response of the POR function.



20167319

SPREAD SPECTRUM (SS)

The LM3370 features Spread Spectrum capability, via I^2C, to reduce the noise amplitude of the switching frequency during data transmission. The feature can be enabled by activating the appropriate control register bit (see register information section for detail). The main clock of the LM3370 features spread spectrum, where : F_{OSC} = 2MHz ± 22kHz. This help reduce noise caused by the harmonics present in the waveforms at the switch pins of the buck regulators. It is controlled by I^2C in the following manner:

I^2C bit	Modulation Frequency
SS_fmod = 1 (default)	1 kHz
SS_fmod = 0	2 kHz

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Good layout for the LM3370 can be implemented by following a few simple design rules:

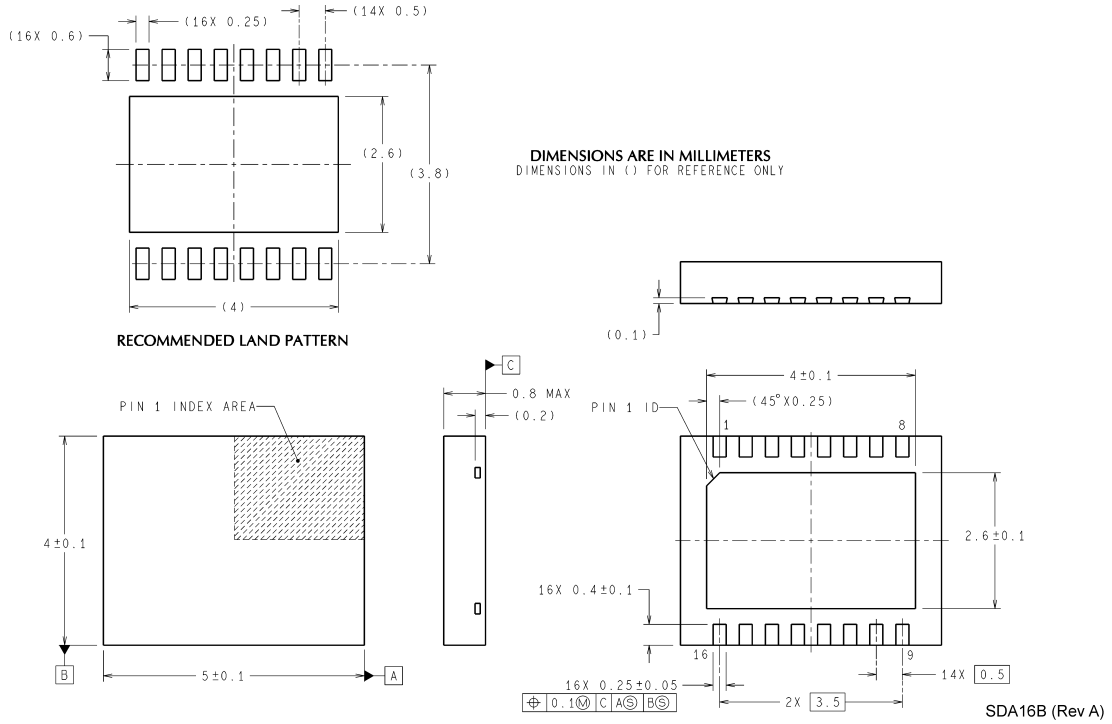
1. *Place the LM3370, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2 in. (5mm) of the LM3370.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor, through the LM3370 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3370 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.

Application Information (Continued)

3. *Connect the ground pins of the LM3370, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3370 by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit*. This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3370 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

Physical Dimensions inches (millimeters) unless otherwise noted



SDA16B (Rev A)

NOTES: UNLESS OTHERWISE SPECIFIED

1. For solder thickness and composition, see “Solder Information” in the packaging section of the National Semiconductor Web Page (www.national.com)
2. Maximum allowable metal burn on lead tips at the package edges is 76 microns.
3. No JEDEC registration as of December 2004.

16-Lead LLP Package
4 mm x 5 mm x 0.75 mm
NS Package Number SDA16B

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