SFF GPON ONT Diplexer
FTM-9423P(T)-K(F)GH(i)G

(ITU-T Rec.G.984.2)

Members of Flexon^{TM} Family

Standard

◆ Compliant with ITU-T G.984.2, G.984.2 Amendment 1
◆ Compliant with FCC 47 CFR Part 15, Class B
◆ Compliant with FDA 21 CFR 1040.10 and 1040.11, Class I

Description

FTM-9423P(T)-K(F)GH(i)G is Optical Network Terminal (ONT) diplexer for 1244/2488M Class B+ application in ITU-T Rec.G.984.2 and G.984.2 Amendment 1.

The diplexers are the high performance modules for 1244/2488M data link in single fiber by using 1310nm burst mode transmitter and 1490nm continuous mode receiver with 1550nm optical signal rejection.

The transmitter section uses a multiple quantum well 1310nm DFB laser, which is Class I laser compliant product according to international safety standard IEC-60825. The receiver section uses an integrated 1490nm APD and preamplifier mounted in an optical header and limiting post-amplifier IC.

The optical burst output can be enabled by a LVTTL logic high-level input of TX_BRST. Signal Detected (SD) output is provided to indicate the detection of an input optical signal of receiver.

The Digital diagnostic monitoring interface is incorporated into the 2×10 SFF transceivers and allows real time access to the transceiver operating parameters such as power supply, operating temperature, laser bias current, receiver optical power by reading a built-in memory with I^2C interface.

Features

◆ Single fiber bi-directional data links with asymmetric 1244Mbit/s upstream and 2488Mbit/s downstream
◆ Integrated with micro-optics WDM filter for dual wavelength Tx/Rx operation at 1310/1490nm
◆ Burst mode operation transmitter with 1310nm DFB laser
◆ Power levelling mechanism(for 2×10 SFF)
◆ Continuous mode operation receiver with 1490nm high sensitivity APD-TIA with 1550nm optical signal rejection
◆ Different operating case temperature class
  0 to 70℃ Standard Class
  -40 to 85℃ Industrial Class
◆ 2×5 and 2×10 SFF package
◆ SC/UPC or SC/APC connector
◆ Single 3.3V power supply
◆ LVPECL data input interface and CML data output interface
◆ LVTTL transmitter burst-mode control
◆ LVTTL receiver signal-detected indication
◆ Low EMI and excellent ESD protection
◆ Class I laser safety standard IEC-60825 compliant

Applications

◆ Gigabit-capable Passive Optical Networks(GPON) ONT with video-overlay

Document Confidential Level: In public   Template ver. 1e

Regulatory Compliance

The transceivers have been tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Flexon^{TM} regulatory specification and safety guidelines, or contact with Fiberxon, Inc. America sales office listed at the end of documentation.

Table 1 - Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class Ⅰ (>500 V)
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compliant with standards
Immunity	IEC 61000-4-3	Compliant with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compliant with Class I laser product
Component Recognition	UL and CSA	Compliant with standards
RoHS	2002/95/EC 4.1&4.2	Compliant with standards

Absolute Maximum Ratings

Absolute Maximum Ratings are those values, beyond which, some damages may occur to the devices. Exposure to conditions above the Absolute Maximum Ratings listed in Table 2 may negatively impact the reliability of the products.

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Ambient Temperature	T_{STG}	-40	85	°C	
Operating Case Temperature (Note)	T_C	0	70	°C	FTM-9423P(T)-K(F)GHG
		-40	85		FTM-9423P(T)-K(F)GHiG
Operating Humidity	H_{OPR}	5	95	%	
Power Supply Voltage	V_{CC}	0	4	V	
Input Voltage		GND	Vcc	V	
Receiver Damaged Threshold		0		dBm	
Soldering Temperature			260/10	°C/s	
Bending Radius		30		mm	

Note: Refer to temperature testing area marked in Figure 6

Recommended Operating Conditions

Table 3 - Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	3.13		3.47	V	3.3V±5%
Operating Case Temperature	T_C	0		70	°C	FTM-9423P(T)-K(F)GHG
		-40		85		FTM-9423P(T)-K(F)GHiG
Operating Humidity	H_{OPR}	5		95	%	
Data Rate(Upstream/Downstream)			1244.16/2488.32		Mbit/s	
Consecutive Identical Digital Immunity		72			Bit	

Optical and Electrical Characteristics

Table 4- Transmitter Optical and Electrical Characteristics

FTM-9423P(T)-K(F)GHG   (0°C <T_C<70°C and 3.13V<V_{CC}<3.47V)

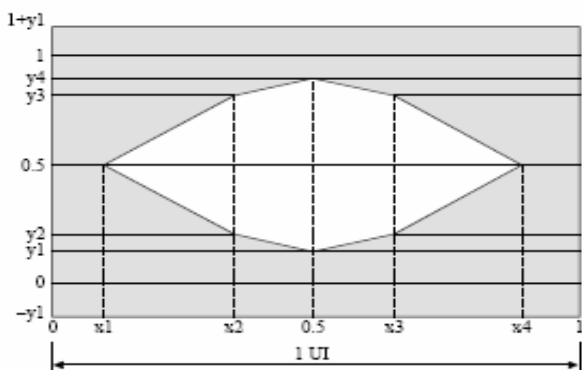FTM-9423P(T)-K(F)GHiG   (-40°C <T_C<85°C and 3.13V<V_{CC}<3.47V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Optical Center Wavelength	λ_C	1260		1360	nm	
Optical Spectrum Width(-20dB)	$\Delta\lambda$			1	nm	
Side Mode Suppression Ratio	SMSR	30				
Average Launch Power (mode 0)		+0.5	2	+5		
Average Launch Power (mode 1)	P_{OUT}	-2.5		+2	dBm	1
Average Launch Power (mode 2)		-5.5		-1		
Average Launch Power-OFF Transmitter	P_{OFF}			-45	dBm	
Extinction Ratio	ER	10			dB	2
Burst Turn On Time	T_{ON}			12.8	ns	3
Burst Turn Off Time	T_{OFF}			12.8	ns	
Transmitter Reflectance				-10	dB	
Tolerance to Transmitter Incident Light Power		-15			dB	
Optical Penalty				0.5	dB	
Optical Eye Diagram	Compliant With ITU-T G984.2					2,4
Data Input Differential Swing	V_{IN}	200		1600	mV	
Common-Mode Input Voltage	V_{CM}	Vcc-1.49	Vcc-1.32	Vcc-V_{IN}/4	V	5
Input Differential Impedance	Z_{IN}	90	100	110	Ω	
Power Supply Current	I_{CC_TX}			250	mA	
Transmitter Burst Control Voltage - Low	$V_{BURST, L}$	0		0.8	V	6
Transmitter Burst Control Voltage - High	$V_{BURST, H}$	2.0		V_{CC}	V	

Note 1: Launched into 9/125um SMF, mode 1, 2 are implemented by power leveling mechanism in 2×10 SFF

Note 2: Measured with PRBS 2^{23}-1 plus 72bits CID test pattern @1244.16Mbit/s, and the Bessel-Thompson filter is turned on.

Note 3: Refer to [Timing Parameter Definition in Burst Mode Sequence](#)

Note 4: Transmitter eye mask definition is shown as below.

		1244.16Mbit/s
x1/x4		0.22/0.78
x2/x3		0.40/0.60
y1/y4		0.17/0.83
y2/y3		0.20/0.80

Note 5: Compatible with LVPECL input (See Recommended Interface Circuit)

Note 6: TX_BRST (See Pin Function Definitions)

Table 5 - Receiver Optical and Electrical Characteristics

FTM-9423P(T)-K(F)GHG   (0°C <T_C<70°C and 3.13V<V_{CC}<3.47V)

FTM-9423P(T)-K(F)GHiG   (-40°C <T_C<85°C and 3.13V<V_{CC}<3.47V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Wavelength		1480	1490	1500	nm	
Sensitivity	P_{SEN}		-31	-29	dBm	1
Overload	P_{OV}	-7				
Signal-Detected Assert Level	P_{SDA}			-30	dBm	2
Signal-Detected Deassert Level	P_{SDD}	-39			dBm	3
Signal-Detected Hysteresis	P_{SDA}- P_{SDD}	0.5		6	dB	
Tolerance to Reflected Optical Power				10	dB	
Receiver Reflectance				-20	dB	
Power Supply Current	I_{CC_RX}			150	mA	
Data Output Differential Swing	V_{OUT}	400		1000	mV	4
Signal-Detected Voltage - Low	$V_{SD, L}$	0		0.4	V	5
Signal-Detected Voltage - High	$V_{SD, H}$	2.4		V_{CC}	V	
Signal-Detected Assert Time	T_{ASS}			100	µs	
Signal-Detected Deassert Time	T_{DAS}			100	µs	

Note 1: Measured with PRBS 2^{23}-1 plus 72bits CID test pattern @2488.32Mbit/s 1310nm, ER=10dB, BER =10^{-10}

Note 2: An increase in optical power above the specified level will cause the Signal Detect output to switch from a low state to a high state.

Note 3: A decrease in optical power below the specified level will cause the Signal Detect output to switch from a high state to a low state.

Note 4: CML output, AC coupled internally, guaranteed in the full range of input optical power (See Recommended Interface Circuit)
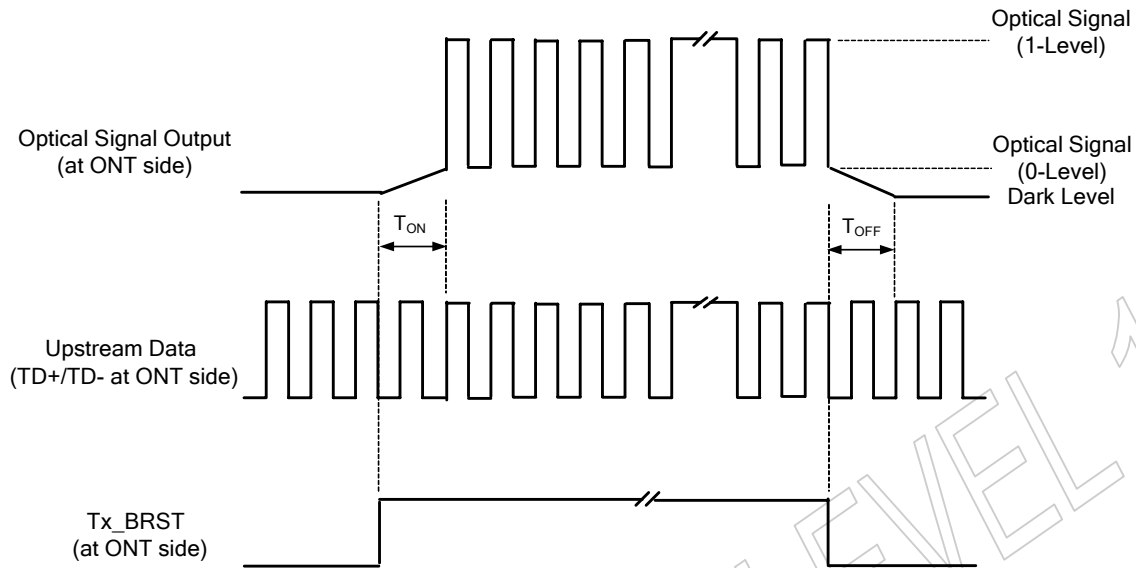
Note 5: SD (See Pin Function Definitions)

Figure 1 Timing Parameter Definition in Burst Mode Sequence

Recommended Interface Circuit

Figure 2 shows the recommended interface scheme for FTM-9423P(T)-FGH(i)G
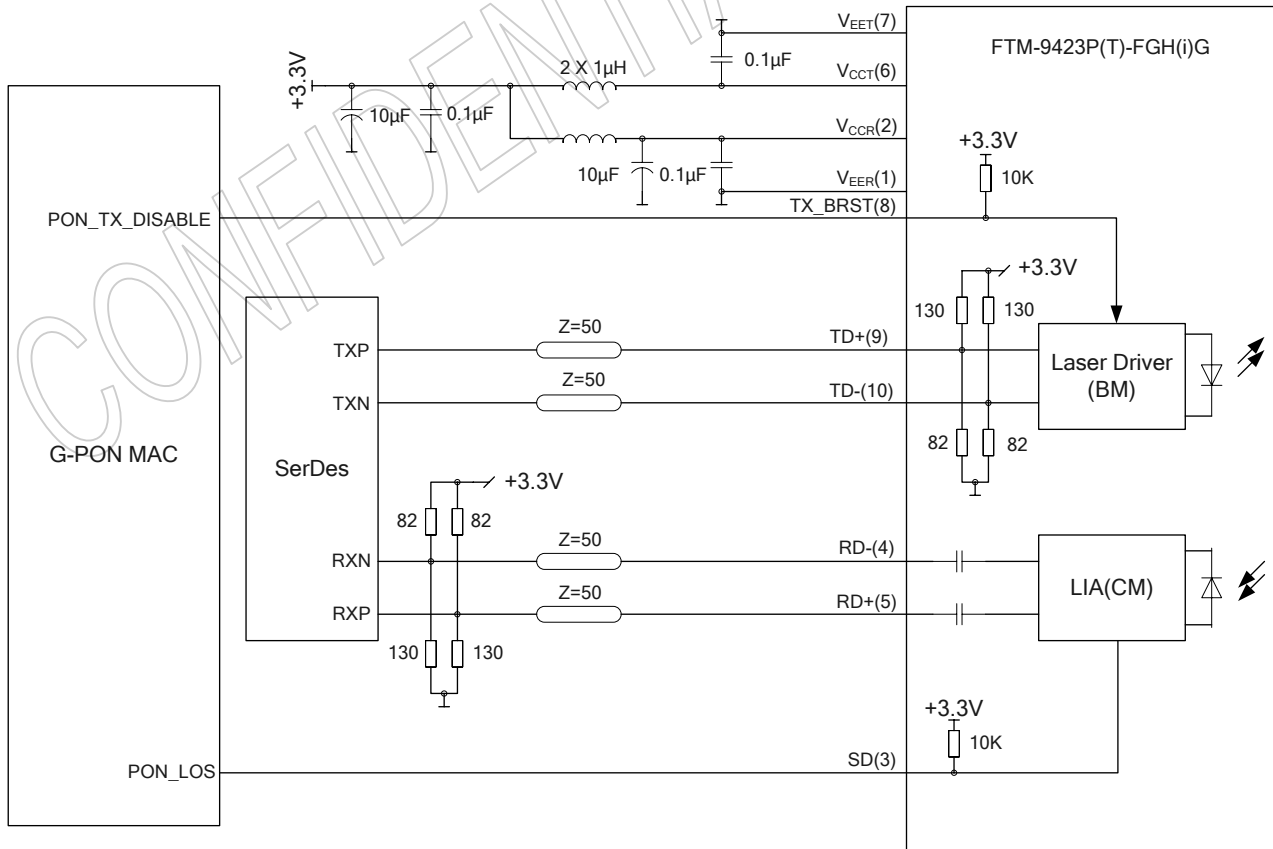

Figure 2 Recommended Interface Circuit for FTM-9423P(T)-FGH(i)G

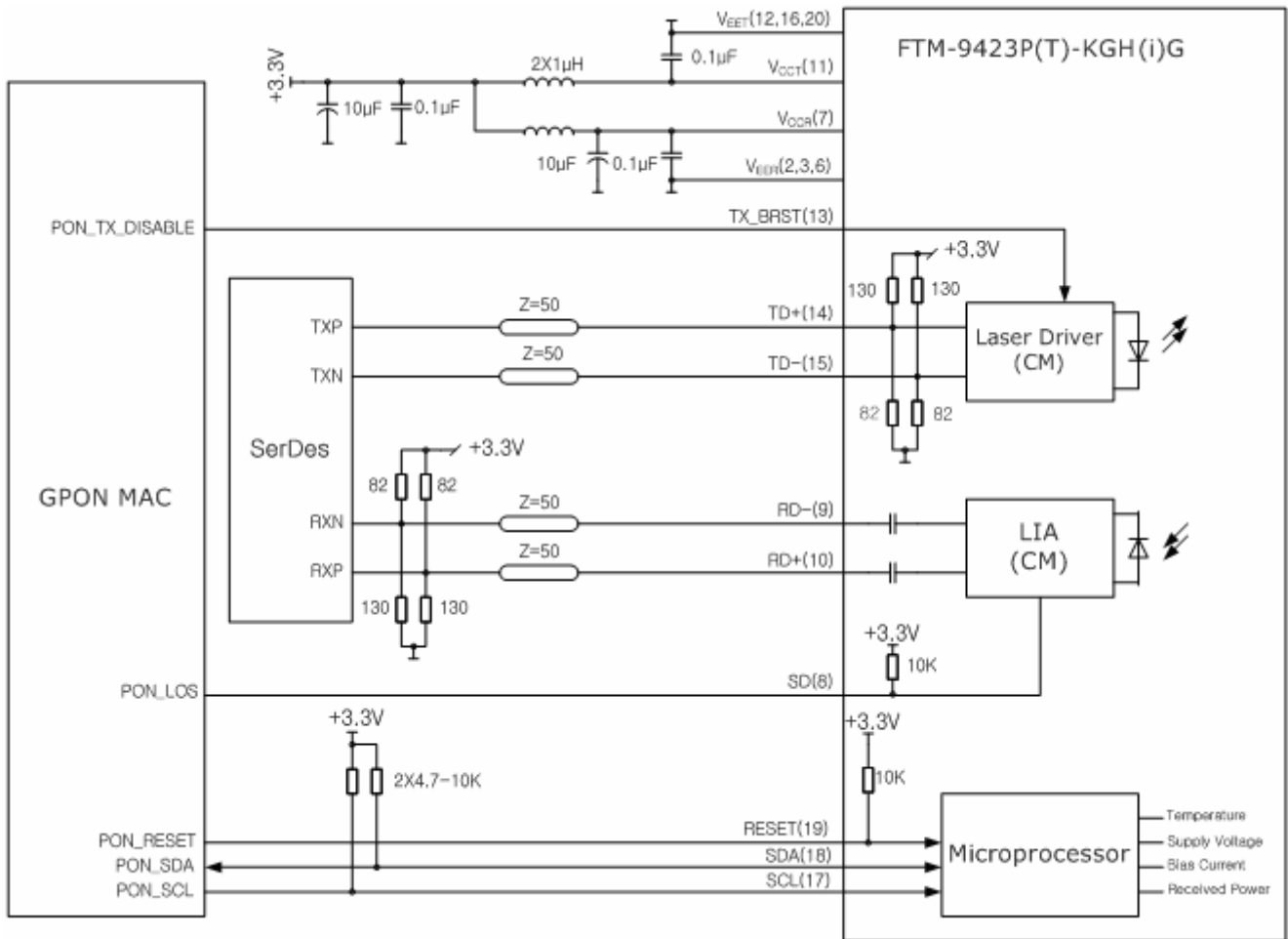Figure 3 shows the recommended interface scheme for FTM-9423P(T)-KGH(i)G
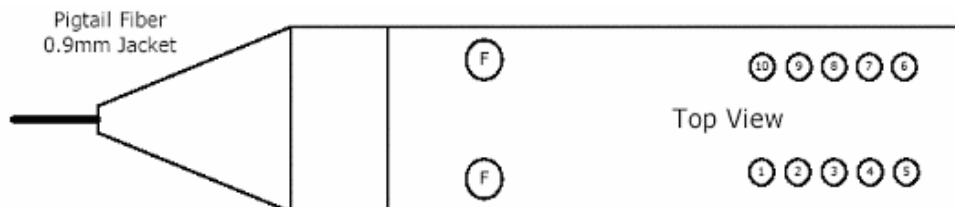

Figure 3 Recommended Interface Circuit FTM-9423P(T)-KGH(i)G

Pin Definitions

2×5/2×10 SFF planform in Figure 4 below shows the pin information of electrical interface and mounting studs. Functions are described in Table 6 and Table 7 with some accompanying notes.
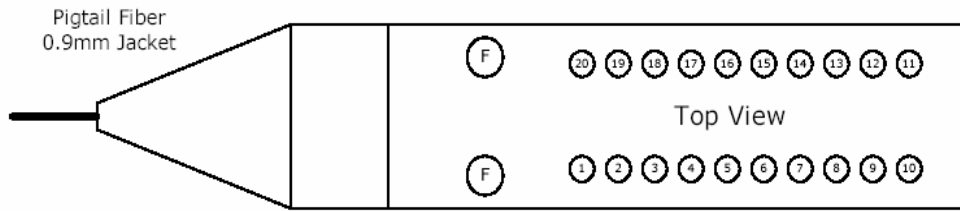
Figure 4 2×5/2×10 SFF Planform

Table 6 - Pin Function Definitions (2x5 SFF)

Pin No.	Name	Description	Notes
1	V$_{EER}$	Receiver Signal Ground	
2	V$_{CCR}$	Receiver Power Supply	
3	SD	Receiver Signal-Detected Indication	1
4	RD-	Inverted Receiver Data Output	2
5	RD+	Non-inverted Receiver Data Output	
6	V$_{CCT}$	Transmitter Power Supply	
7	V$_{EET}$	Transmitter Signal Ground	
8	TX_BRST	Transmitter Burst Control	3
9	TD+	Transmitter Non-inverted Data Input	4
10	TD-	Transmitter Inverted Data Input	
F	MS	Mounting Studs	5

Table 7 - Pin Function Definitions (2x10 SFF)

Pin No.	Name	Description	Notes
1	NC	No Function Definition	Not connected
2	V$_{EER}$	Receiver Signal Ground	
3	V$_{EER}$	Receiver Signal Ground	
4	NC	No Function Definition	Not connected
5	NC	No Function Definition	Not connected
6	V$_{EER}$	Receiver Signal Ground	
7	V$_{CCR}$	Receiver Power Supply	
8	SD	Receiver Signal-Detected Indication	1
9	RD-	Inverted Receiver Data Output	2
10	RD+	Non-inverted Receiver Data Output	
11	V$_{CCT}$	Transmitter Power Supply	
12	V$_{EET}$	Transmitter Signal Ground	
13	TX_BRST	Transmitter Burst Control	3
14	TD+	Transmitter Non-inverted Data Input	4
15	TD-	Transmitter Inverted Data Input	
16	V$_{EET}$	Transmitter Signal Ground	
17	SCL	Clock Line of the I^{2}C interface	6

18	SDA	Data Line of the I^{2}C interface	6
19	RESET	Reset Input to Microprocessor	7
20	V$_{EET}$	Transmitter Signal Ground	
F	MS	Mounting Studs	5

Note 1: LVTTL logic output, with internal 10KΩ pull-up resistor.

      Optical Signal-Detected: High; Optical Signal Loss: Low

Note 2: CML logic output, AC coupled internally. (See Recommended Interface Circuit)

Note 3: A positive level enable optical signal output under burst mode.

      (See Timing Parameter Definition in Burst Mode Sequence)

Note 4: Compatible with LVPECL input, DC coupled internally

      (See Recommended Interface Circuit)

Note 5: The mounting studs are provided for transceiver mechanical attachment to circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground. The holes in the circuit board must be tied to chassis ground. It is not recommended that the mounting studs be connected to signal ground.

Note 6: I^{2}C interface, they should be pulled up with two 4.7-10KΩ resistors on the host board.

Note 7: LVTTL reset input to microprocessor, with internal 10KΩ pull-up resistor, active low.

Mechanical Design Diagram

The form factor is 2×5/2×10 SFF with pigtail fiber. The pigtail fiber length is 520 - 550mm and its minimum bending radius is 30mm. The fiber connector type is SC/UPC or SC/APC. The mechanical design diagram is shown in Figure 5 and Figure 6. (Dimension in mm)
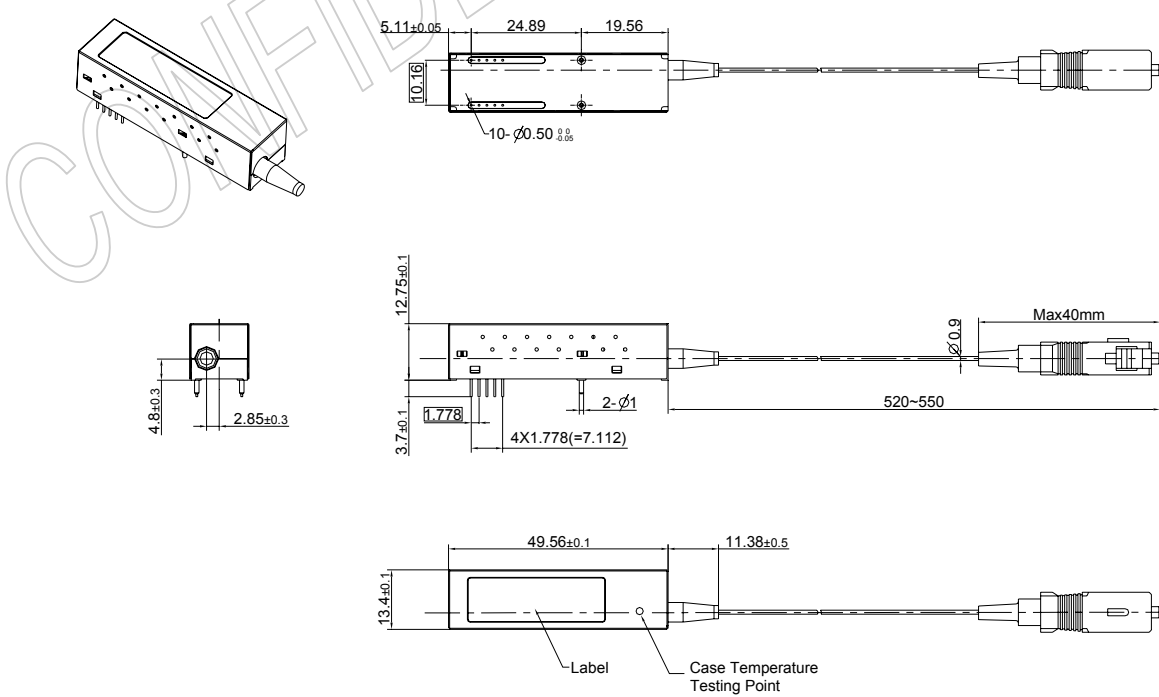

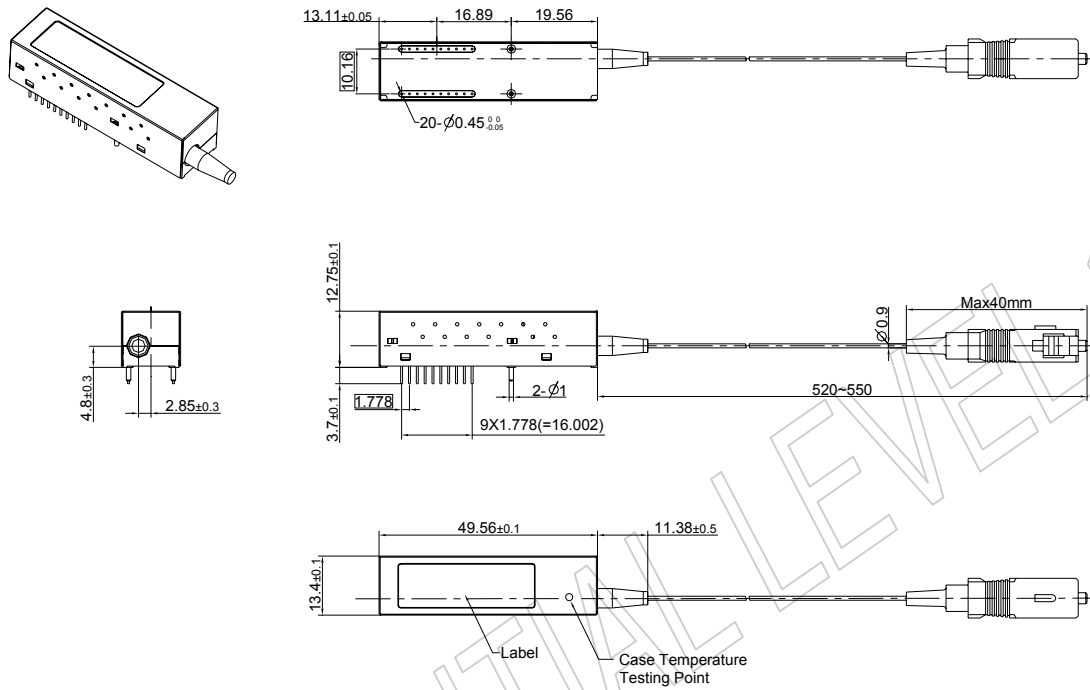**Figure 5 Mechanical Design Diagram (2x5 SFF)**

Figure 6 Mechanical Design Diagram (2x10 SFF)

Table 8 - Pigtail Fiber Characteristics

Parameter	Min.	Typical	Max.	Unit
Mode Field Diameter		9		μm
Cladding Diameter		125		μm
Jacket Diameter		0.9		mm
Bending Radius of Pigtail Fiber	30			mm
Tension Force on Pigtail Fiber			1	Kg
Pigtail Fiber Length	520		550	mm
Optical Return Loss (UPC type) -1310nm	50			dB
Optical Return Loss (APC type) -1310nm	60			dB

EEPROM Information

The SFF-8472 defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard interfaces, manufacture, and other information, which is accessible over 2 wire interface at the 8-bit address 1010000X(A0h). The memory contents refer to Table 9.

Table 9 - EEPROM Serial ID Memory Contents (A0h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
0	1	Identifier	02	SFF Tranceiver
1	1	Ext. Identifier	04	MOD4
2	1	Connector	0B	Optical pigtail
3-10	8	Transceiver	XX XX XX XX XX XX XX XX	(Transmitter Code, not defined for GPON)
11	1	Encoding	03	NRZ
12	1	BR, Nominal	0C	1.244Gbps transmission
13	1	Reserved	00	
14	1	Length (9um)-km	14	20(km)
15	1	Length (9um)	C8	200(100m)
16	1	Length (50um)	00	Not Support MMF
17	1	Length (62.5um)	00	Not Support MMF
18	1	Length (Copper)	00	Not Support Copper
19	1	Reserved	00	
20-35	16	Vendor name	46 49 42 45 52 58 4F 4E 20 49 4E 43 2E 20 20 20	"FIBERXON INC." (ASCII)
36	1	Reserved	00	
37-39	3	Vendor OUI	00 00 00	
40-55	16	Vendor PN	46 54 4D 39 34 32 33 50(54) 4B(46) 47 48 47 20 20 20 20	"FTM-9423P(T)-K(F)GHG" (ASCII)
			46 54 4D 39 34 32 33 50(54) 4B(46) 47 48 69 47 20 20 20	"FTM-9423P(T)-K(F)GHiG" (ASCII)
56-59	4	Vendor Rev	XX XX 20 20	ASCII("31 30 20 20" means 1.0 Revision)
60-61	2	Wavelength	05 1E	1310nm Laser Wavelength
62	1	Reserved	00	
63	1	CC_BASE	XX	Check sum of byte 0-62
64-65	2	Options	00 06	SD,LAS_FAIL and TX_DISABLE
66	1	BR, max	00	
67	1	BR, min	00	
68-83	16	Vendor SN	XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX	ASCII
84-91	8	Date code	XX XX XX XX XX XX 20 20	Year(2 bytes),Month(2 bytes),Day(2 bytes)

92	1	Diagnostic Monitoring Type	68	Compliant with SFF-8472 V9.5 Internally Calibrated Received power measurement type -Average Power
93	1	Enhanced Options	80	Diagnostics (Optional Alarm/warning flags)
94	1	SFF-8472 Compliance	02	Diagnostics Compliance(SFF-8472 V9.5)
95	1	CC_EXT	XX	Check sum of byte 64-94
96-255	164	Vendor Specific		

Monitoring Specification

The digital diagnostic monitoring interface defines 256 bytes memory map in EEPROM, which makes use of the 8 bit address 1010001X(A2h). Please see Figure 7. Table 10~12 show the EEPROM definition from 0 to 119 byte, please refer to the SFF-8472 Rev 9.5 for the data format of these tables. The monitoring specification of this product is described in Table 13.
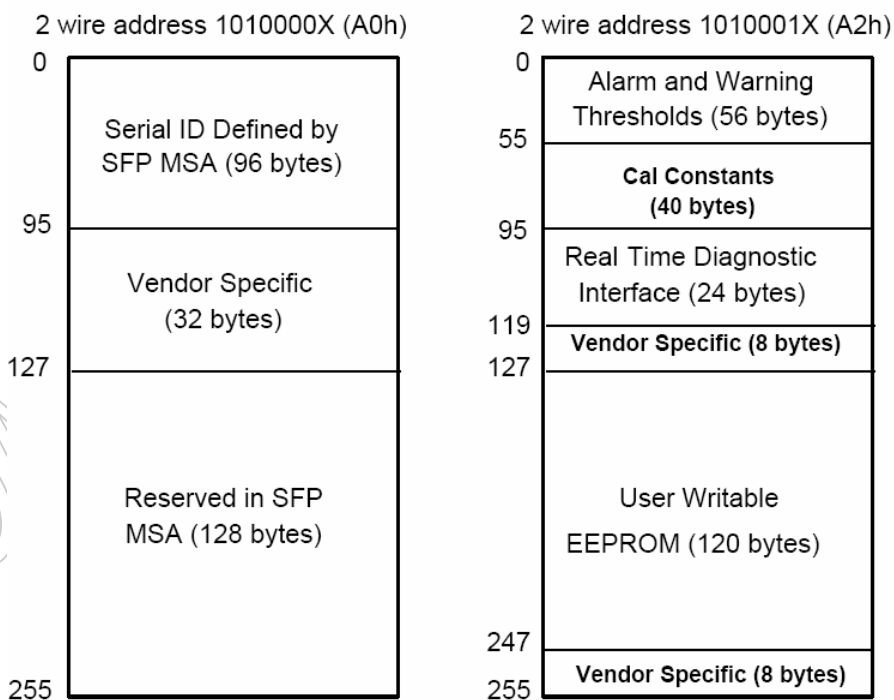

Figure 7 EEPROM Memory Map Specific Data Field Descriptions

Table 10 - EEPROM Serial ID Memory of the Alarm and Warning Thresholds Contents in A2h

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
00-01	2	Temp High Alarm	XX XX	Based on difference operation case temperature class product
02-03	2	Temp Low Alarm	XX XX	
04-05	2	Temp High Warning	XX XX	

06-07	2	Temp Low Warning	XX XX	
08-09	2	Voltage High Alarm	94 70	3.8 V
10-11	2	Voltage Low Alarm	6D 60	2.8 V
12-13	2	Voltage High Warning	8C A0	3.6 V
14-15	2	Voltage Low Warning	75 30	3.0 V
16-17	2	Bias High Alarm	75 30	60 mA
18-19	2	Bias Low Alarm	05 DC	3 mA
20-21	2	Bias High Warning	61 A8	50 mA
22-23	2	Bias Low Warning	07 D0	4 mA
24-31	8	Reserved	00 00	
32-33	2	RX Power High Alarm	0F 8D	-4dBm
34-35	2	RX Power Low Alarm	00 0A	-30dBm
36-37	2	RX Power High Warning	0C 5A	-5dBm
38-39	2	RX Power Low Warning	00 0C	-29dBm
40-55	24	Reserved	00 00	0

Table 11 - EEPROM Serial ID Memory of the Calibration Constants Contents in A2h

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
56-59	4	Rx_PWR(4)	00 00 00 00	0
60-63	4	Rx_PWR(3)	00 00 00 00	0
64-67	4	Rx_PWR(2)	00 00 00 00	0
68-71	4	Rx_PWR(1)	3F 80 00 00	1
72-75	4	Rx_PWR(0)	00 00 00 00	0
76-77	2	Tx_I(Slope)	01 00	1
78-79	2	Tx_I(Offset)	00 00	0
80-81	2	Tx_PWR(Slope)	01 00	1
82-83	2	Tx_PWR(Offset)	00 00	0
84-85	2	T (Slope)	01 00	1
86-87	2	T (Offset)	00 00	0
88-89	2	V (Slope)	01 00	1
90-91	2	V (Offset)	00 00	0
92-94	3	Reserved	00 00 00	0
95	1	Checksum	XX	Check sum of byte 0-94

Table 12 - EEPROM Serial ID Memory of the A/D Values and Status Bits Contents in A2h

Addr.	Bit	Name of Field	Hex	Description
96-97	7-0	Temperature	XX XX	
98-99	7-0	V_CC	XX XX	
100-101	7-0	TX Bias	XX XX	
102-103	7-0	Reserved	XX XX	

104-105	7-0	RX Power	XX XX	
106-109	7-0	Reserved	00 00 00 00	0
110	7	TX Disable State		
110	6	Soft TX Disable		
110	5~3	Reserved	XX	
110	2	TX Fault		
110	1	LOS		
110	0	Data_Ready_Bar		
111	7-2	Reserved	00	0
111	1-0	Power leveling control	00	00 for the power levelling mode 0
			01	01 for the power levelling mode 1
			10	10 for the power levelling mode 2
112	7	Temp High Alarm		
112	6	Temp Low Alarm		
112	5	V$_{CC}$ High Alarm		
112	4	V$_{CC}$ Low Alarm	XX	
112	3	TX Bias High Alarm		
112	2	TX Bias Low Alarm		
112	1-0	Reserved		
113	7	RX Power High Alarm		
113	6	RX Power Low Alarm		
113	5-0	Reserved	"000000"	0
114-115	7-0	Reserved	00 00	0
116	7	Temp High Warning		
116	6	Temp Low Warning		
116	5	V$_{CC}$ High Warning		
116	4	V$_{CC}$ Low Warning	XX	
116	3	TX Bias High Warning		
116	2	TX Bias Low Warning		
116	1-0	Reserved		
117	7	RX Power High Warning		
117	6	RX Power Low Warning		
117	5-0	Reserved	"000000"	0
118-119	0-7	Reserved	00 00	0

Note: The "XX" byte should be filled in according to practical case. For more information, please refer to the related document of SFF-8472 Rev 9.5.

Table 13- Monitoring Specification

Parameter	Range	Accuracy	Calibration
Temperature	-40 to 100°C	±3°C	Internal
Voltage	3.0 to 3.6V	±3%	Internal
Bias Current	0 to 100mA	±10%	Internal
RX Power	-30 to -4dBm	±3dB	Internal

Ordering Information

Part No.	Product Description
FTM-9423P-FGHG	1310nm(TX)/1490nm(RX), SC/UPC Pigtailed 2×5 SFF for GPON ONT 1244/2488M Class B+ application, 0°C ~ 70°C, RoHS compliance
FTM-9423P-FGHiG	1310nm(TX)/1490nm(RX), SC/UPC Pigtailed 2×5 SFF for GPON ONT 1244/2488M Class B+ application, -40°C ~ 85°C, RoHS compliance
FTM-9423P-KGHG	1310nm(TX)/1490nm(RX), SC/UPC Pigtailed 2×10 SFF for GPON ONT 1244/2488M Class B+ application, power levelling supported, 0°C ~ 70°C, RoHS compliance
FTM-9423P-KGHiG	1310nm(TX)/1490nm(RX), SC/UPC Pigtailed 2×10 SFF for GPON ONT 1244/2488M Class B+ application, power levelling supported, -40°C ~ 85°C, RoHS compliance
FTM-9423T-FGHG	1310nm(TX)/1490nm(RX), SC/APC Pigtailed 2×5 SFF for GPON ONT 1244/2488M Class B+ application, 0°C ~ 70°C, RoHS compliance
FTM-9423T-FGHiG	1310nm(TX)/1490nm(RX), SC/APC Pigtailed 2×5 SFF for GPON ONT 1244/2488M Class B+ application, -40°C ~ 85°C, RoHS compliance
FTM-9423T-KGHG	1310nm(TX)/1490nm(RX), SC/APC Pigtailed 2×10 SFF for GPON ONT 1244/2488M Class B+ application, power levelling supported, 0°C ~ 70°C, RoHS compliance
FTM-9423T-KGHiG	1310nm(TX)/1490nm(RX), SC/APC Pigtailed 2×10 SFF for GPON ONT 1244/2488M Class B+ application, power levelling supported, -40°C ~ 85°C, RoHS compliance

Related Documents

For further information, please refer to the following documents:

- ITU-T G.984.2
- ITU-T G.984.2. Amendment 1

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Revision History

Reversion	Initiate	Review	Approve	Subject	Release Date
Pre 1a	Gary Chen	Peter Tang	Peter Tang	Initial datasheet(temporary version) (Doc No. DS0000002-1a)	Jul. 7, 2006
Pre.1b	Gary Chen	Peter Tang	Peter Tang	Revised Datasheet 1. Modify the pin definition 2. Update Figure 3 (Doc No. DS0000002-1b)	Aug. 7, 2006
Pre.1c	Gary Chen	Peter Tang	Peter Tang	Revised Datasheet: 1. Added the module figure 2. Modify the order information	Sep. 26, 2006
Pre.1d	Jacob Cai	Gary Chen	Peter Tang	Revised Datasheet: 1. Update the value of overload in Table 4 from -5dBm to -7dBm 2. Delete FTM-9423P(T)-K(F)GHEG. (Doc No. DS0000002-1d)	May 15, 2007

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