800 MHz to 3800 MHz Crest Factor Detector

Preliminary Technical Data

ADL5502

FEATURES

- True rms response detector
- Envelope output with peak hold option
- Excellent temperature stability
- ±0.25 dB rms detection accuracy vs. temperature
- ±0.25 dB envelope detection accuracy vs. temperature; over the top 15 dB of the input range
- Over 30 dB input power dynamic range, inclusive of crest factor, up to 3.8 GHz
- RF bandwidths from 800 MHz to 3.8 GHz
- Envelope bandwidths of 10 MHz
- 500 Ω input impedance
- Single-supply operation: 2.7 V to 3.5 V
- Low power: 5 mA at 3 V supply
- RoHS compliant

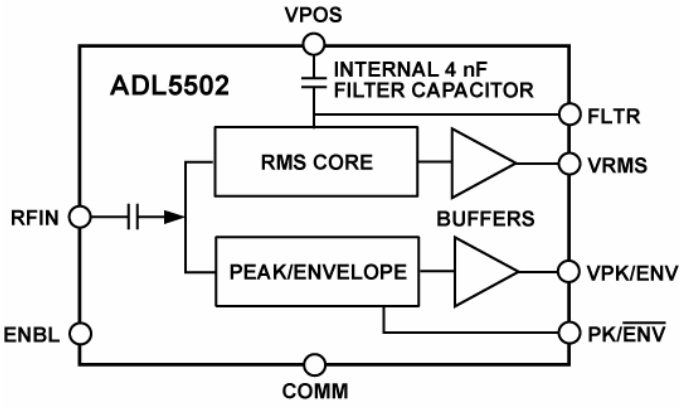

Figure 1.

APPLICATIONS

- Power and envelope measurement of W-CDMA, CDMA2000, and QPSK-/QAM-based OFDM, and other complex modulation waveforms
- RF transmitter or receiver power and envelope measurement

GENERAL DESCRIPTION

The ADL5502 is a mean-responding power detector in combination with an envelope detector to accurately determine the crest factor of a modulated signal. It can be used in high frequency receiver and transmitter signal chains from 800 MHz to 3.8 GHz with envelope bandwidths over 10 MHz. Requiring only a single supply between 2.7 V and 3.5 V, the detector draws less than 5 mA. The input is internally ac-coupled and has a nominal input impedance of 500 Ω.

The rms output is a linear-responding dc voltage with a conversion gain of 2.0 V/Vrms at 900 MHz. The envelope output with a conversion gain of 1.4 V/V can be toggled between real-time envelope measurement or peak hold with less than TBD mV droop in over 200 μS.

The ADL5502 is a highly accurate, easy to use means of determining the peak to average value of complex waveforms. It can be used for crest factor measurements of both simple and complex waveforms, but is particularly useful for measuring high crest factor (high peak-to-rms ratio) signals, such as CDMA2000, W-CDMA, and QPSK/QAM-based OFDM waveforms. The peak hold function allows the capture of short peaks in the envelope with lower sampling rate ADC's.

The crest factor detector operates from −40°C to +85°C and is available in an 8-ball, 1.5 mm × 1.5 mm wafer-level chip scale package. It is fabricated on a high f_T silicon BiCMOS process.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

SPECIFICATIONS

T_A = 25°C, V_S = 3.0 V, R_{FLT} = 100 nF, light condition ≤ 600 LUX, unless otherwise noted. Including 50 ohm input termination resistor.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	450		3800	MHz
RMS CONVERSION (f = 450 MHz)	Input RFIN to output VRMS				
Input Impedance			TBD||TBD		Ω||pF
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		25		dB
±2 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error		TBD		dBm
Minimum Input Level	±1 dB error		TBD		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.82		V/V rms
Output Intercept[4]			0.001		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V
ENVELOPE CONVERSION	Input RFIN to output VENV				
Dynamic Range[1]	CF=3.5 dB, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error[3]		TBD		dBm
Minimum Input Level	±1 dB error[3]		TBD		dBm
Conversion Gain			1.4		V/V
Output Intercept[4]			TBD		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V
RMS TO ENVELOPE TRACKING	CW input, −40°C < T_A < +85°C				
±0.25 dB Error	V_S = 3 V		15		dB
±1 dB Error	V_S = 3 V		25		dB
±2 dB Error	V_S = 3 V		30		dB
RMS CONVERSION (f = 800 MHz)	Input RFIN to output VRMS				
Input Impedance			331||1.0		Ω||pF
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		25		dB
±2 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error		TBD		dBm
Minimum Input Level	±1 dB error		TBD		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.81		V/V rms
Output Intercept[4]			0.001		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V

Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 900 MHz)	Input RFIN to output VRMS				
Input Impedance			316||0.9		Ω||pF
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		25		dB
±2 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error		TBD		dBm
Minimum Input Level	±1 dB error		TBD		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.80		V/V rms
Output Intercept[4]			0.001		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V
RMS CONVERSION (f = 1900 MHz)	Input RFIN to output VRMS				
Input Impedance			215||0.9		Ω||pF
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		25		dB
±2 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error		TBD		dBm
Minimum Input Level	±1 dB error		TBD		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.75		V/V rms
Output Intercept[4]			−0.005		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V
RMS CONVERSION (f = 2350 MHz)	Input RFIN to output VRMS				
Input Impedance			TBD||TBD		Ω||pF
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		25		dB
±2 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error		TBD		dBm
Minimum Input Level	±1 dB error		TBD		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.56		V/V rms
Output Intercept[4]			−0.004		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V
RMS CONVERSION (f = 2700 MHz)	Input RFIN to output VRMS				
Input Impedance			TBD||TBD		Ω||pF
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		25		dB
±2 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error		TBD		dBm
Minimum Input Level	±1 dB error		TBD		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.53		V/V rms
Output Intercept[4]			−0.006		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V

Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 3500 MHz)	Input RFIN to output VRMS				
Input Impedance			TBD||TBD		Ω||pF
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	V_S = 3 V		15		dB
±1 dB Error[3]	V_S = 3 V		25		dB
±2 dB Error[3]	V_S = 3 V		30		dB
Maximum Input Level	±0.25 dB error		TBD		dBm
Minimum Input Level	±1 dB error		TBD		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.33		V/V rms
Output Intercept[4]			−0.005		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		TBD		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		TBD		V
VRMS OUTPUT	Pin VRMS				
Output Offset	No signal at RFIN		150		mV
Response time	5 dB Step, 10% to 90% of settling level, no filter cap		15		µS
Available Output Current			3		mA
VENV OUTPUT	Pin VENV				
Envelope Modulation Bandwidth		5	10		MHz
Maximum Output Voltage	V_s = 2.7 V, R_{LOAD} ≥ 10 kΩ		1.5		V
Output Offset	No signal at RFIN		TBD		mV
Response time	5 dB Step, 10% to 90% of settling level, no filter cap		TBD		µS
Available Output Current			3		mA
PEAK HOLD					
Hold Time		100	200		µS
Hold Voltage Drop			TBD		mV/ µS
CONTROL INTERFACE					
Logic Level to, Real Time Envelope, HI	2.7 V ≤ V_S ≤ 3.5 V, −40°C < T_A < +85°C	1.8		V_{POS}	V
Input Current when HI	2.7 V at ENBL, −40°C ≤ T_A ≤ +85°C		0.05	0.1	µA
Logic Level for Peak Hold Condition, LO	2.7 V ≤ V_S ≤ 3.5 V, −40°C < T_A < +85°C	−0.5		+0.5	V
Enable Time	C_{FLTR} = Open, 0 dBm at RFIN		TBD		µs
Disable Time	C_{FLTR} = 100 nF, 0 dBm at RFIN		TBD		µs
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power, HI Condition	2.5 V ≤ V_S ≤ 3.5 V, −40°C < T_A < +85°C	1.8		V_{POS}	V
Input Current when HI	2.5 V at ENBL, −40°C ≤ T_A ≤ +85°C		0.05	0.1	µA
Logic Level to Disable Power, LO Condition	2.5 V ≤ V_S ≤ 3.5 V, −40°C < T_A < +85°C	−0.5		+0.5	V
Power-Up Response Time[5]	C_{FLTR} = Open, 0 dBm at RFIN		TBD		µs
	C_{FLTR} = 100 nF, 0 dBm at RFIN		TBD		µs
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.5		3.5	V
Quiescent Current	No signal at RFIN[6]		5.0		mA
Disable Current	ENBL in LO Condition, no signal at RFIN		< TBD	5	µA

[1] The available output swing, and hence the dynamic range, is altered by the supply voltage; see TBD.
[2] Error referred to delta from 25°C response.
[3] Error referred to best-fit line at 25°C
[4] Calculated using linear regression.
[5] The response time is measured from 10% to 90% of settling level
[6] Supply current is input level dependant; see TBD.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage V_S	3.5 V
VRMS, VPK/ENV, ENBL, PK/ENV	0 V, V_S
RFIN	1.25 V rms
Equivalent Power, re 50 Ω	15 dBm
Internal Power Dissipation	TBD mW
θ_{JA} (SC-70)	TBD°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

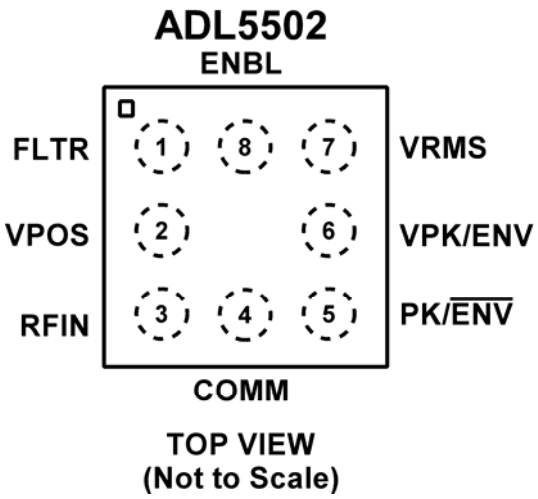


Figure 2. 8-Bump WLCSP Configuration

Table 3. Pin Function Descriptions

Ball No.	Mnemonic	Description
1	FLTR	Modulation Filter Pin. Connection for an External Capacitor to lower the corner frequency of the modulation filter
2	VPOS	Supply Voltage Pin. Operational range 2.7 V to 3.5 V.
3	RFIN	Signal Input Pin. Internally ac-coupled after internal termination resistance. Nominal 500 Ω input impedance.
4	COMM	Device Ground Pin.
5	PK/ENV	Control Pin. Connect pin to ground for real-time envelope measurement mode. Connect pin to V_S for peak-hold mode. Reset peak-hold by placing device in real-time envelope measurement mode.
6	VPK/ENV	Envelop Output. Function can switched between real-time envelop measurement or peak-hold using PK/ENV.
7	VRMS	RMS Output Pin. Rail-to-rail voltage output with limited current drive capability. The output has an internal TBD kΩ series resistance. High resistive loads are recommended to preserve output swing.
8	ENBL	Enable Pin. Connect pin to V_S for normal operation. Connect pin to ground for disable mode.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 3.0 V, C_{FLTR} = open, C_{OUT} = 4.7 nF, Colors: black = +25°C, blue = −40°C, red = +85°C, unless otherwise noted.

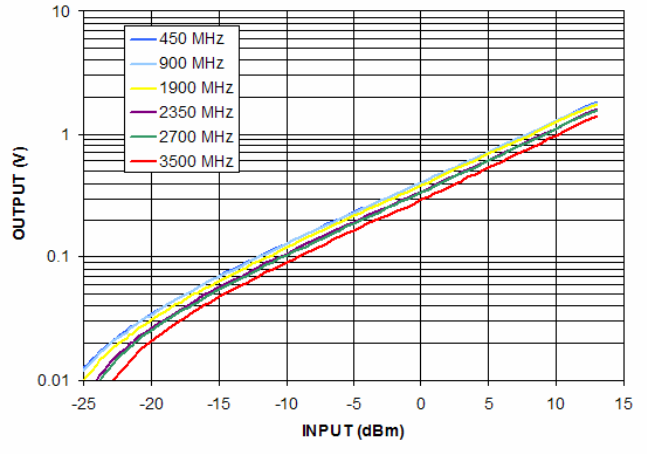


Figure 3. VRMS Output vs. Input Level, Frequencies 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, and 3500 MHz, Supply 3.0 V

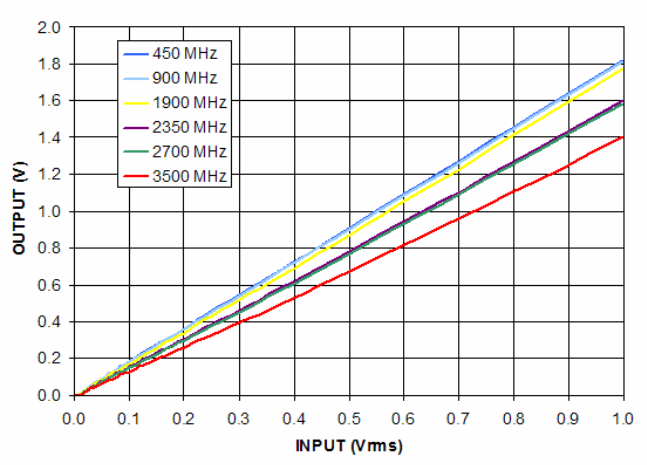


Figure 4. VRMS Output vs. Input Level (Linear Scale), Freq 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, and 3500 MHz, Supply 3.0 V

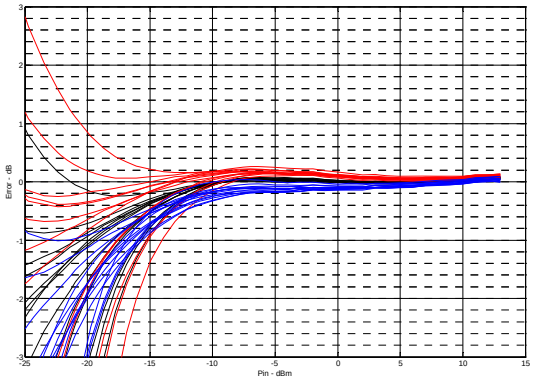


Figure 5. VRMS Temperature Drift Distributions for Multiple Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 900 MHz

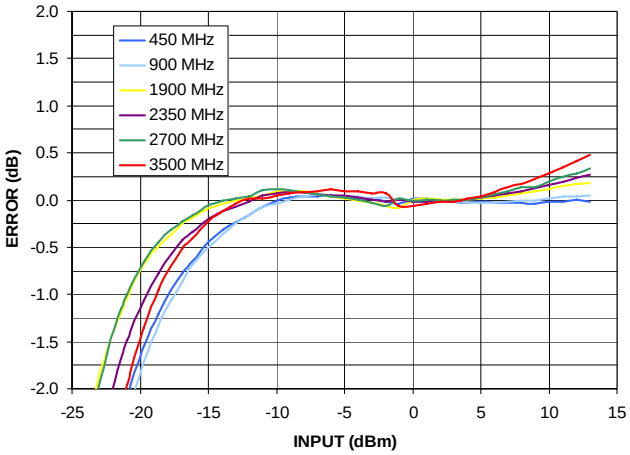


Figure 6. VRMS Linearity Error vs. Input Level, Freq 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, and 3500 MHz, Supply 3.0 V

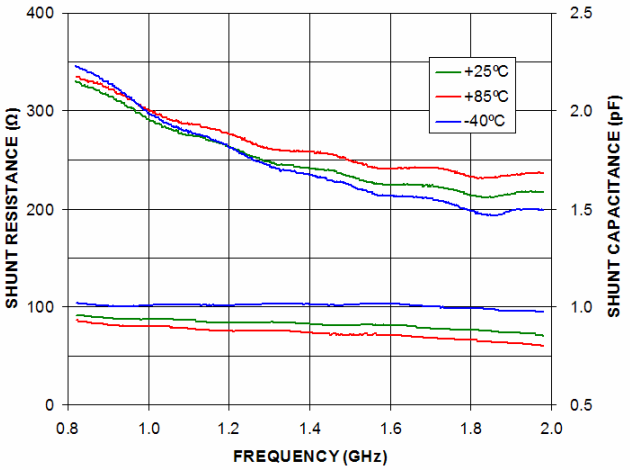


Figure 7. Input Impedance vs. Frequency, Supply 3.0 V, Temperatures −40°C, +25°C, and +85°C

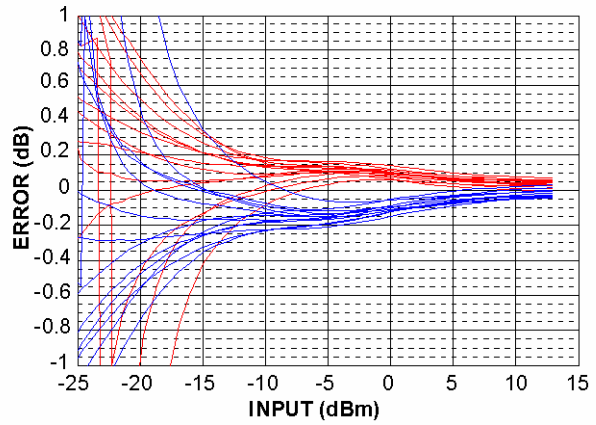


Figure 8. VRMS Delta from +25°C Output Voltage for Multiple Devices at −40°C and +85°C, Frequency 900 MHz

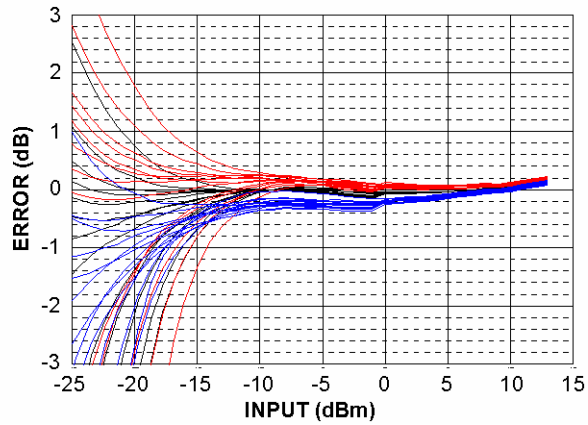


Figure 9. VRMS Temperature Drift Distributions for Mulitple Devices at –40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency1 900 MHz

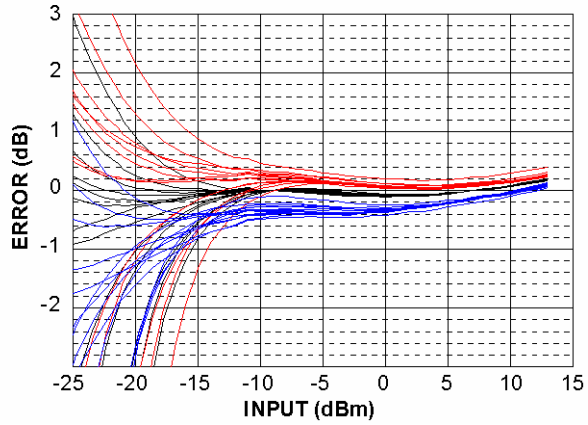


Figure 10. VRMS Temperature Drift Distributions for Mulitple Devices at –40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 2350 MHz

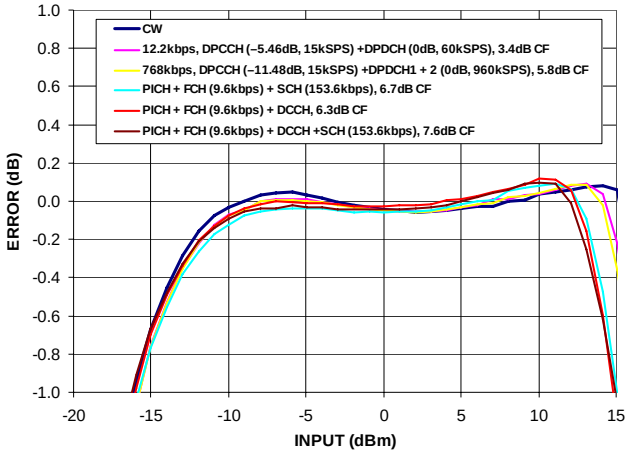


Figure 11. VRMS Error from CW Linear Reference vs. Input with Various WCDMA & CDMA2000 Rev Link Waveforms at 1900 MHz, C_{FLTR} = 22 nF

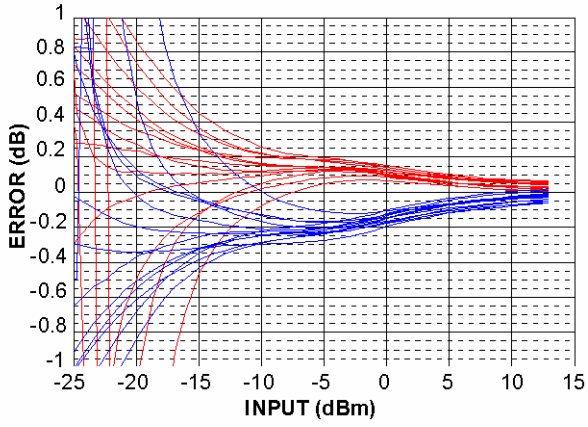


Figure 12. VRMS Delta from +25°C Output Voltage for Multiple Devices at –40°C and +85°C, Frequency 1900 MHz

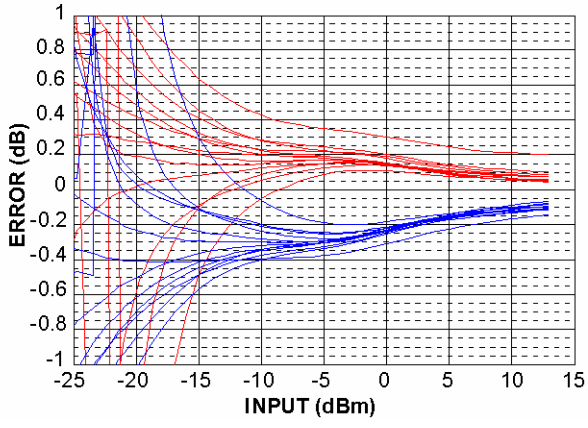


Figure 13. VRMS Delta from +25°C Output Voltage for Multiple Devices at –40°C and +85°C, Frequency 2350 MHz

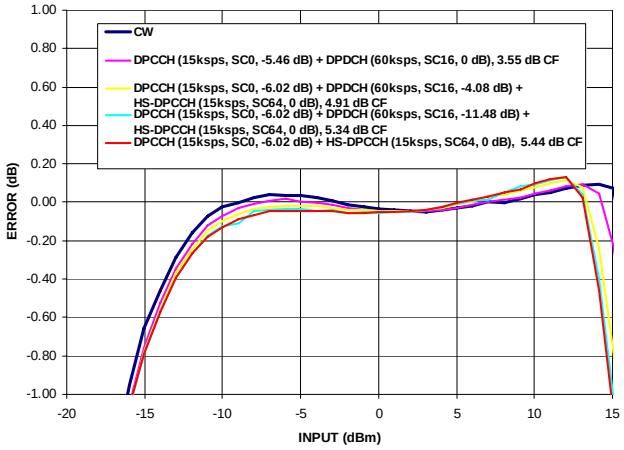
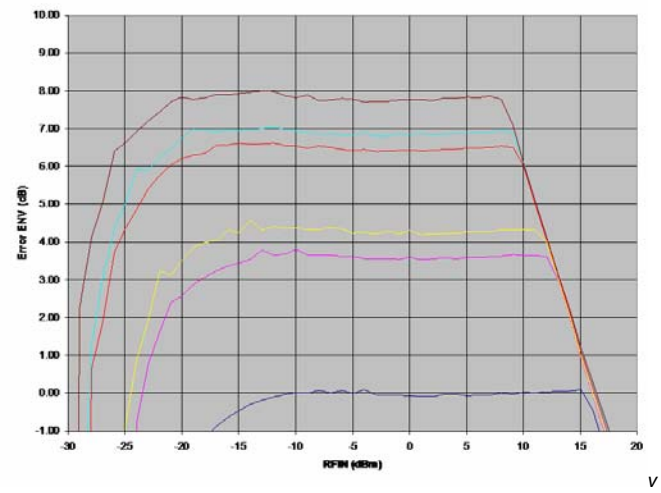


Figure 14. VRMS Error from CW Linear Reference vs. Input with Various WCDMA HSPA Reverse Link Waveforms at 1900 MHz, C_{FLTR} = 22 nF



v

Figure 15.v Envelope Error (representative of Crest Factor) from rms Reference vs. Input with Various WCDMA and CDMS2000 Reverse Link Waveform,; at 1900 MHz, C_{FLTR} = 22 nF, C_{OU} = 4.7 nF,

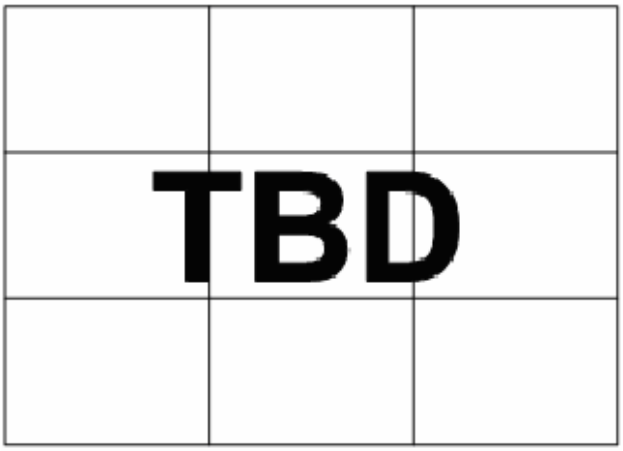


Figure 16. Peak Hold Response Time

APPLICATIONS

BASIC CONNECTIONS

Figure 17 shows the basic connections for the ADL5502. The device is powered by a single supply between 2.5 V and 3.5 V, with a quiescent current of 5 mA. The VPOS pin is decoupled using 100 pF and 0.1 μF capacitors.

Placing a single 75 Ω resistor at the RF input provides a broadband match of 50 Ohms. More precise resistive or reactive matches can be applied for narrow frequency band use (see impedance plot, Figure 7).

The rms averaging can be augmented by placing additional capacitance at CFLT. The ac residual can be further reduced by increasing the output capacitance, COUT. The combination of the internal 100 Ω output resistance and COUT produce a low-pass filter to reduce output ripple of the VRMS output. Note that a minimum of 4.7 nF capacitive load should be kept on the RMS output.

To operate the device in peak-hold mode, the control line must be temporally set to HI (reset or envelope mode) and then set back to LO (peak-hold mode). This allows the ADL5502 to be initialize to a known state.

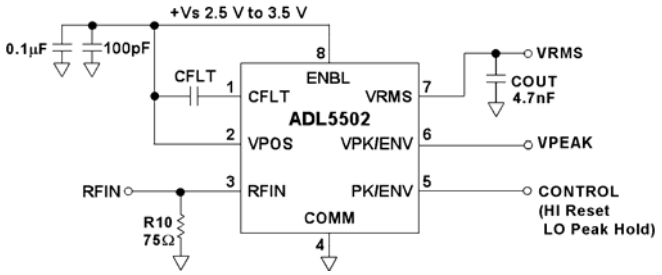


Figure 17. Basic Connections for ADL5502

EVALUATION BOARD

Figure 18 shows the schematic of the ADL5502 evaluation board. The board is powered by a single supply in the 2.5 V to 3.5 V range. The power supply is decoupled by 100 pF and 0.1 μF capacitors. Table 4 details the various configuration options of the evaluation board. Figure 19 and Figure 20 show the component and circuit layouts of the evaluation board.

The RF input has a broadband match of 50 Ohms using a single 75 Ω resistor at R10. More precise matching at spot frequencies is possible using the pads for components C15, C16, and R10.

The two outputs, accessible via the SMAs labeled VRMS and VENV, provide the rms response and the envelope/peak-hold vmeasurement of the RF input power level. The device must be enabled by switching SW1 to HI (setting the switch to the position opposite that of the "SW1" label).

The device is place in peak-hold mode by placing switch SW2 in the position closes to the "SW2" label. Envelope-tracking mode is possible by setting SW2 in the opposite switch position (away from the "SW2" label). A signal generator can drive the control mode via the SMA labeled CNTL (see Table 4 for more details).

OPERATING IN PEAK-HOLD MODE

To operate the device in peak-hold mode, the control line must be temporally set to HI (envelope mode) and then set back to LO (peak-hold mode). This allows the ADL5502 to be initialize to a known state.

For envelope mode or rms use only, the control line can simply be set to HI.

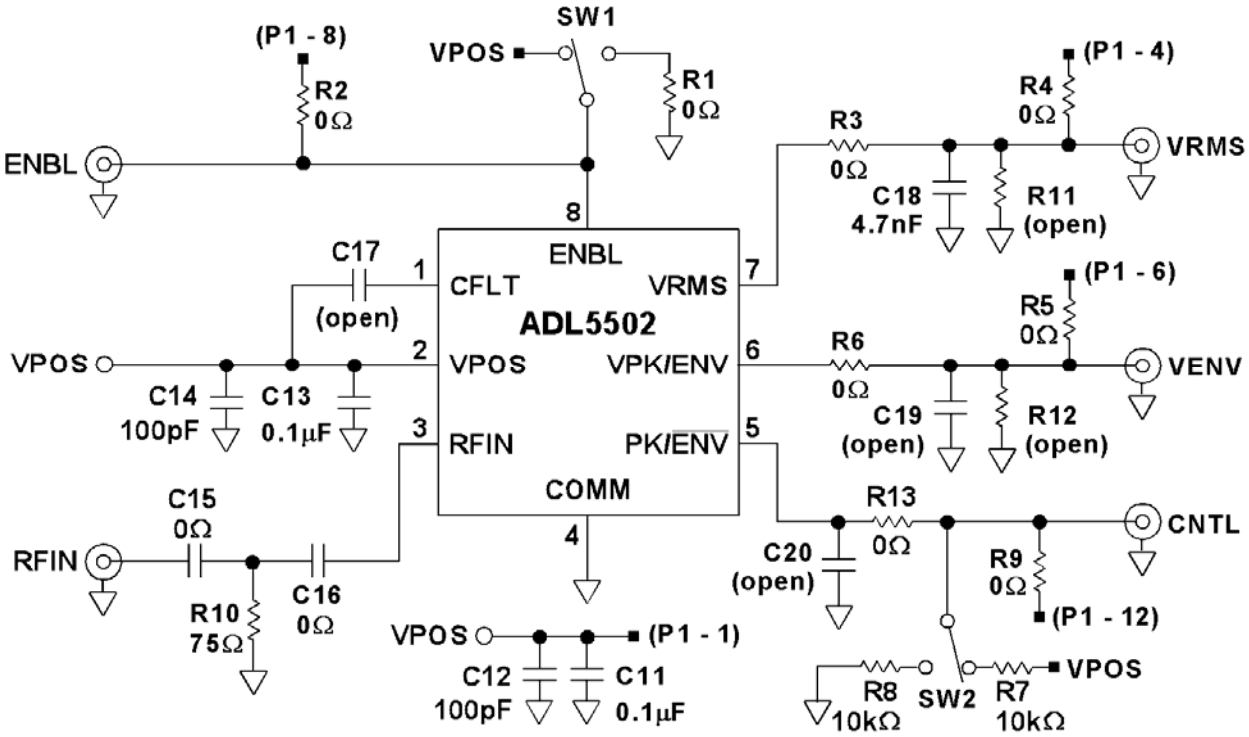


Figure 18. Evaluation Board Schematic

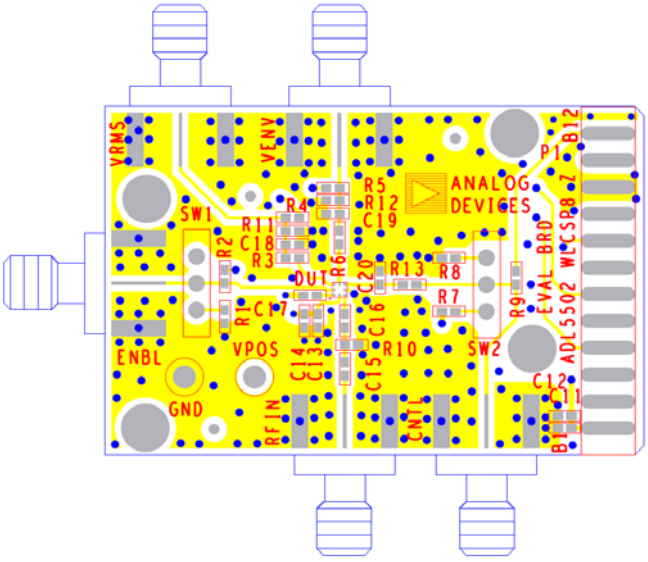


Figure 19. Layout of Evaluation Board, Component Side

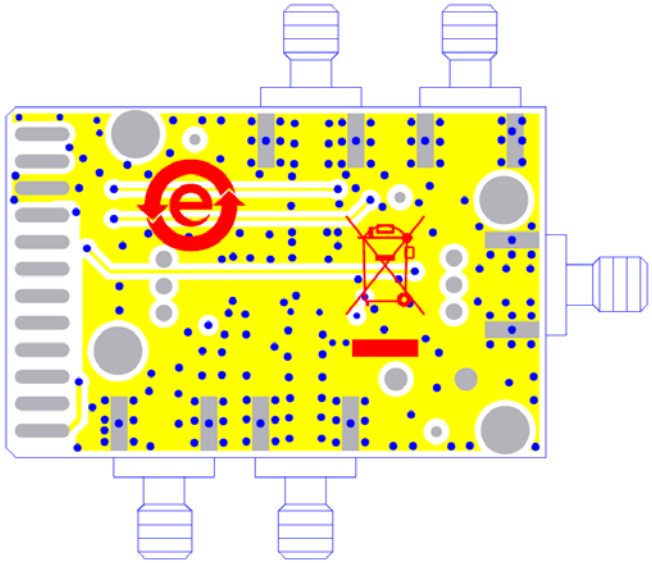


Figure 20. Layout of Evaluation Board, Circuit Side

Table 4. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and Supply Vector Pins.	Not Applicable
C13, C14	Power Supply Decoupling. Nominal supply decoupling of 0.01 µF and 100 pF.	C13 = 0.1 µF (Size 0402) C14 = 100 pF (Size 0402)
C17	Filter Capacitor. The internal rms averaging capacitor can be augmented by placing additional capacitance in C17.	C17 = Open (Size 0402)
R10, C15, C16	RF Input interface. The 75 Ω resistor at R10 combines with the ADL5502 internal input impedance to give a broadband input impedance of around 50 Ω. The pads for components C15, C16, and R10 can be used for more precise matching at a particular frequency.	R10 = 75 Ω (Size 0402) C15, C16 = 0 Ω (Size 0402)
R3, R6, R11, R12, C18, C19	Output Filtering. The combination of the internal 100 Ω output resistance and C18 produce a low-pass filter to reduce output ripple of the VRMS output. Similarly, C19 and the internal 100 Ω output resistance will form a low-pass filter to at the VPK/ENV output. Either output can be scaled down using the resistor divider pads, R3, R11, R6, and R12. Note that a minimum of 4.7 nF capacitive load should be kept on the RMS output.	R11, R12 = Open (Size 0402) R3, R6 = 0 Ω (Size 0402) C18 = 4.7 nF (Size 0402) C19 = Open (Size 0402)
R1, SW1	Device Enable. When the switch is set towards the "SW1" label, the ENBL pin is grounded (through the 0 Ω resistor) putting the device in power-down mode. In the opposite switch position, the ENBL pin is connected to VPOS and the ADL5502 is in operating mode. While the switch is in the disabled position, the ENBL pin can be driven by a signal generator via the SMA labeled ENBL. In this case, R1 must be removed or changed to provide a 50 Ω match.	R1 = 0 Ω (Size 0402) SW1 = away from "SW1" label
R7, R8, R13, C20, SW2	Control Interface. When the switch is set towards the "SW2" label, the PK/ENV pin is grounded (through a 10 kΩ resistor) putting the device in peak-hold mode. In the opposite switch position, the pin is connected to VPOS (through a 10 kΩ resistor) and the ADL5502 is in envelope-tracking mode. While the switch is in the peak-hold position, the PK/ENV pin can be driven by a signal generator via the SMA labeled CNTL. In this case, R8 may be removed or changed to provide a 50 Ω match. R13 and C20 allow for low-pass filter design for the control pin.	R7, R8 = 10 kΩ (Size 0402) R13 = 0 Ω (Size 0402) C20 = Open (Size 0402) SW2 = away from "SW1" label
R2, R4, R5, R9, C11, C12	Alternate Interface. The end connector, P1, allows access to various ADL5502 signals. These signal paths are only used during factory test and characterization.	R2, R4, R5, R9 = 0 Ω (Size 0402) C11 = 0.1 µF (Size 0402) C12 = 100 pF (Size 0402)

OUTLINE DIMENSIONS

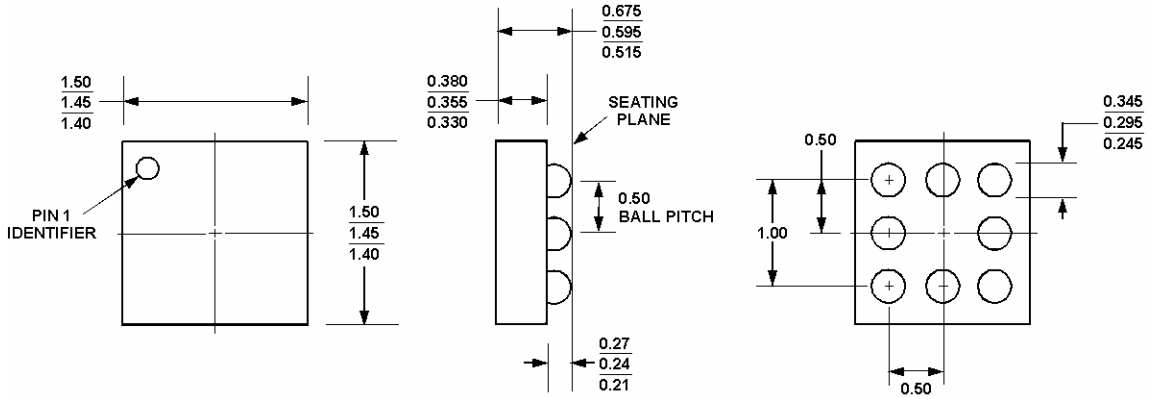


Figure 21. 8-Bump Wafer Level Chip Scale Package [WLCSP]
(TBD)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline	Branding	Ordering Quantity
ADL5502ACBZ-P7[1]	–40°C to +85°C	8-Lead WLCSP, 7″ Pocket Tape and Reel	KS-8	TBD	3,000
ADL5502ACBZ-P2[1]	–40°C to +85°C	8-Lead WLCSP, 7″ Pocket Tape and Reel	KS-8	TBD	250
ADL5502-EVALZ[1]		Evaluation Board			

[1] Z = Pb-free part.

NOTES

PR07631-0-6/08(PrD)