Brief Description

The ZSSC1750 and ZSSC1751 are System Basis Chips (SBCs) with a dual-channel ADC for battery sensing/management in automotive, industrial, and medical systems. The ZSSC1750 and ZSSC1751 feature an SPI interface; in addition, the ZSSC1750 has an integrated LIN 2.1 transceiver.

One of the two input channels measures the battery current I_{BAT} via the voltage drop at the external shunt resistor. The second channel measures the battery voltage V_{BAT} and the temperature.

By simultaneously measuring V_{BAT} and I_{BAT}, it is possible to determine dynamically the internal resistance of the battery, Rdi, which is correlated with the state-of-health (SOH) of the battery. By integrating I_{BAT}, it is possible to determine the state-of-charge (SOC) and the state-of-function (SOF) of the battery.

During Sleep Mode, the system makes periodic measurements to monitor the discharge of the battery. Measurement cycles are controlled by user software and include various wake-up conditions. The ZSSC1750/51 is optimized for ultra-low power consumption drawing only 60µA or less in this mode.

Features

- Two high-precision 24-bit sigma-delta ADCs (18-bit with no missing codes); sample rate: 1Hz to 16kHz
- On-chip voltage reference (5ppm/K typical)
- Current channel
  - I_{BAT} offset error: ≤ 10mA
  - I_{BAT} resolution: ≤ 1mA
  - Programmable gain: 4 to 512
  - Max. differential input stage input range: ±300mV
- Voltage channel
  - Input range: 4 to 28.8V
  - Voltage accuracy: ±60ppm FSR* = 1.73mV
- Temperature channel
  - External temperature sensor (NTC)
  - Factory-calibrated internal temp. sensor: ±2°C
- LIN 2.1/SAE J2602-1 transceiver (ZSSC1750 only)
- Typical current consumption
  - Normal Mode: 12mA
  - Sleep Mode: ≤ 60µA

Benefits

- Integrated, precision measurement solution for accurate prediction of battery state of health (SOH), state of charge (SOC), or state of function (SOF)
- Robust power-on-reset (POR) concept for harsh automotive environments
- On-chip precision oscillator accuracy: ±1%
- On-chip low-power oscillator
- Only a few external components needed
- Easy communication via SPI interface
- Power supply, interrupt, and reset signals for external microcontroller
- Watchdog timer with dedicated oscillator
- Industry's smallest footprint allows minimal module size and cost
- AEC-Q100 qualified solution

Available Support

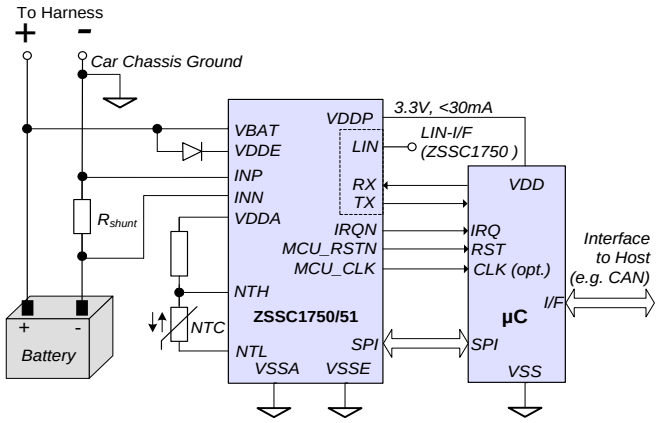
- Evaluation Kit
- Application Notes

Physical Characteristics

- Operation temperature up to -40°C to +125°C
- Supply voltage: 4.2 to 18V
- Small footprint package: PQFN36 6x6 mm

* FSR = full-scale range.

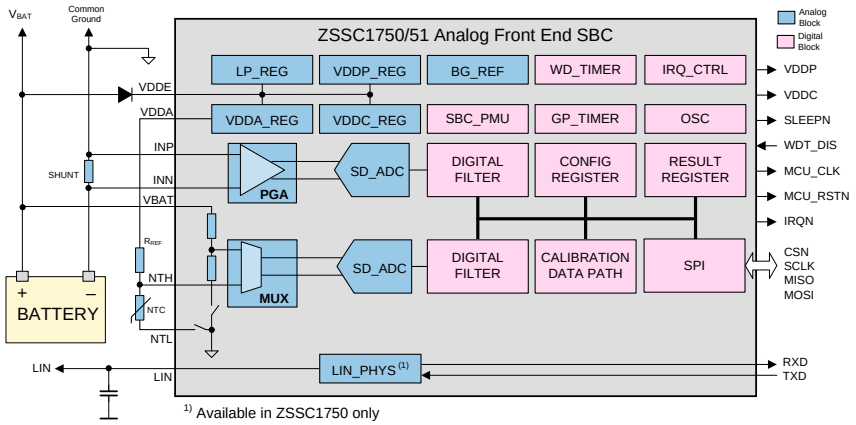
Basic ZSSC1750/51 Application Circuit



ZSSC1750/51 Block Diagram

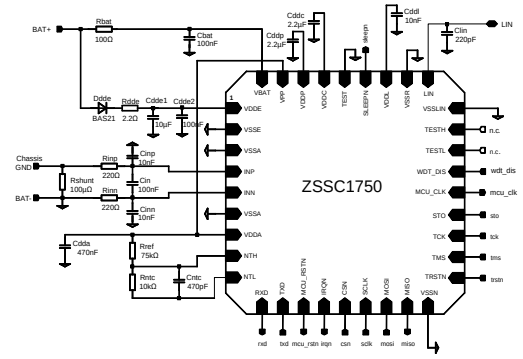
Applications

- Intelligent battery monitoring in automotive applications; start/stop systems, e-bikes, scooters, and e-carts
- Battery monitoring in Industrial, medical and photovoltaic applications;
- High precision data acquisition

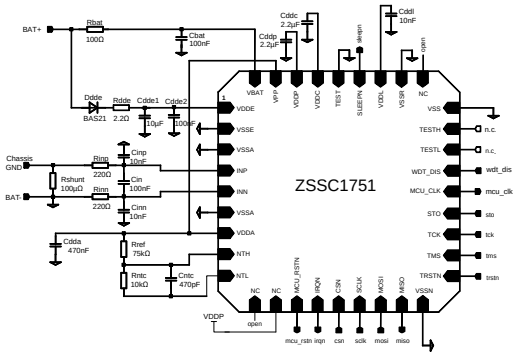


1) Available in ZSSC1750 only

ZSSC1750 Typical Application Circuit



ZSSC1751 Typical Application Circuit



Ordering Information

Product Sales Code	Description	Package
ZSSC1750EA3R	ZSSC1750 Battery Sensing SBC—Temperature Range: -40°C to 125°C	PQFN36 6x6 mm, reel
ZSSC1751EA3R	ZSSC1751 Battery Sensing SBC—Temperature Range: -40°C to 125°C	PQFN36 6x6 mm, reel
ZSSC1750KIT V1.1	ZSSC1750/51 Evaluation Kit: modular evaluation and development board for ZSSC1750/51, 3 IC samples, and USB cable (software and documentation can be downloaded from www.IDT.com)	

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1 IC Characteristics

The absolute maximum ratings are stress ratings only. The ZSSC1750/51 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

1.1 Absolute Maximum Ratings

Table 1.1 Absolute Maximum Ratings (referenced to VSSE)

No	Parameter	Symbol	Conditions	Min	Max	Unit
1.1.1.	External power supply	V_{DDE}		V_{SSE}-0.3	40	V
1.1.2.	Current sensing, INP pin	V_{INP}		V_{SSE}-0.3	V_{DDA}+0.3	V
1.1.3.	Current sensing, INN pin	V_{INN}		V_{SSE}-0.3	V_{DDA}+0.3	V
1.1.4.	Voltage sensing, VBAT pin	V_{VBAT}		-18	33	V
1.1.5.	Voltage sensing, VBAT pin	V_{VBAT}	1h over lifetime	-18	40	V
1.1.6.	Temperature sensing, NTH pin	V_{NTH}		V_{SSE}-0.3	V_{DDA}+0.3	V
1.1.7.	Temperature sensing, NTL pin	V_{NTL}		V_{SSE}-0.3	V_{DDA}+0.3	V
1.1.8.	LIN bus interface, LIN pin	V_{LIN}		-16	33	V
1.1.9.	LIN bus interface, LIN pin	V_{LIN}	1h over lifetime	-16	40	V
1.1.10.	Digital IO pins	V_{IO}		V_{SSE}-0.3	V_{DDP}+0.3	V
1.1.11.	Ambient temperature under bias	T_{AMB}			125	°C
1.1.12.	Junction temperature	T_j			135	°C
1.1.13.	Storage temperature	T_{STOR}		-50	125	°C

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1.2 Recommended Operating Conditions

Table 1.2 Operating Conditions

No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
1.2.1	Operating temperature range	T_{AMB}	Ambient temperature; RTH_{JA}=27K/W	-40		115	°C
1.2.2	Extended temperature range	T_{AMB_Ext}	Ambient temperature; reduced accuracies	-40		125	°C
1.2.3	Supply voltage at BAT+ terminal[1)] for normal operation	V_{BAT+}		6	13	18	V
1.2.4	Minimum supply voltage at VDDE pin: a) When BAT+ < 6V, i.e. operation with low battery b) When V_{BAT} = V_{DDE} , i.e. without using Ddde and Rdde [1)]	V_{DDE_low}	Normal accuracy for current and temperature measurements Reduced accuracy for voltage measurements	4.8			V
			Reduced accuracy for all measurements	4.2			
1.2.5	Digital input voltage LOW	V_{IL}		0		0.3∗V_{DDP}	V
1.2.6	Digital input voltage HIGH	V_{IH}		0.7∗V_{DDP}		V_{DDP}	V

1) See application diagram on page 2.

1.3 Electrical Parameters

Note: See important notes at the end of the following table. See section 3.7 for definitions of the ULP and OFF power states.

Table 1.3 Electrical Specifications

No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Supply							
1.3.1.	Average supply current at VDDE	I_{DDE_avg}	Normal Mode (FP State, both ADCs on)	10	12	14	mA
1.3.2.	Average power dissipation	P_{DDE_avg}	Normal Mode, V_{DDE}=13V	130	156	182	mW
1.3.3.	Current at VDDE in Sleep Mode (ULP State with no measurement)	I_{DDE_slp}	T_{AMB} = room temperature (RT)		55		µA
			T_{AMB} = 115°C		100		µA
1.3.4.	Average current at VDDE in Comparator Mode (ULP State with wake-up interval = 30s and current ADC only)	I_{DDE_cmp}	T_{AMB} = RT		160		µA
1.3.5.	Average current at VDDE in OFF State (no measurements)	I_{DDE_off}	T_{AMB} = RT		50		µA
1.3.6.	Internal analog power supply voltage, VDDA pin	V_{DDA}		2.4	2.5	2.6	V
1.3.7.	Internal digital power supply voltage, VDDL pin	V_{DDL}		1.62	1.8	1.98	V
External Microcontroller (MCU) Supply							
1.3.8.	External microcontroller core power supply voltage, VDDC pin	V_{DDC}	Default	1.62	1.8	1.98	V
			Configuration option (see section 2.2)	1.08	1.2	1.32	V
1.3.9.	External microcontroller power supply voltage (periphery), VDDP pin	V_{DDP}	Default	2.97	3.3	3.63	V
			Configuration option (see section 2.2)	2.25	2.5	2.75	V
1.3.10.	Output current of VDDP regulator	I_{VDDP_OUT}		-	-	40	mA

No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
1.3.11.	Output current capability of VDDP pin	I_{VDDP}	See Figure 1.1 for test circuit	-	-	30	mA
1.3.12.	Output current of VDDC regulator	I_{VDDC_OUT}				40	mA
1.3.13.	Output current capability of VDDC pin	I_{VDDC}				40	mA
Digital IO Pins Parameters (VDDP = 3.3V)							
1.3.14.	Input low-to-high threshold voltage	V_{LH_th}		55	60	65	% of V_{DDP}
1.3.15.	Input high-to-low threshold voltage	V_{HL_th}		35	40	45	% of V_{DDP}
1.3.16.	Internal pull-down resistor	R_{PULL_down}	Vpin = V_{DDP}	70	190	310	kΩ
1.3.17.	Leakage current	$I_{LEAK_I/O}$		-	-	1	µA
1.3.18.	Output low level	V_{OL}	$I_{OUT} = I_{_I/O}$	-	-	20	% of V_{DDP}
1.3.19.	Output high level	V_{OH}	$I_{OUT} = I_{_I/O}$	80	-	-	% of V_{DDP}
1.3.20.	Output low level of SLEEPN pin	V_{L_SLEEPN}	I_{SLEEPN} = 0.1mA	-	-	0.40	V
1.3.21.	Output high level of SLEEPN pin	V_{H_SLEEPN}	I_{SLEEPN} = 0.1mA	1.40	-	-	V
1.3.22.	Pin output current [1)]	$I_{_I/O}$	MCU_CLK pin	-	-	3.0	mA
1.3.23.			All other IOs	-	-	1.5	mA
1.3.24.		I_{SLEEPN}	SLEEPN pin	-	-	0.1	mA
1.3.25.	Pin capacitance [1)]	$C_{_I/O}$		4.5	5.5	6.5	pF
Current Channel							
1.3.26.	Input signal range [1)]	$Range_C$	Gain = 4	-300		300	mV
			Gain = 8	-150		150	mV
			Gain = 16	-75		75	mV
			Gain = 32	-38		38	mV
			Gain = 64	-19		19	mV
			Gain = 128	-9.5		9.5	mV
			Gain = 256	-4.7		4.7	mV
			Gain = 512	-2.3		2.3	mV
1.3.27.	Input leakage current [1)]	I_{LEAK_C}	T_{AMB} = 25°C	-3		+3	nA

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No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
1.3.28.	Input offset current [1)]	I_{OFFSET_C}	For input signal < 10mV		0.5	1.5	nA
1.3.29.	Conversion rate [1), 2)]	$Rate_C$	Programmable	1		16000	Hz
1.3.30.	Oversampling ratio (OSR) [1)] (Sinc^4 decimation filter)	OSR_C	Programmable	32		256	
1.3.31.	No missing codes [1)]	NMC_C		18			Bits
1.3.32.	Integral nonlinearity [1), 3)]	INL	Maximum input range		±10	±60	ppm of FSR [4)]
1.3.33.	PGA gain range [1)]	A_{PGA}		4		512	
1.3.34.	Total gain error [1)]	err_{PGA_C}		-1		1	%
1.3.35.	Gain drift [1)]	$err_drift_{PGA_C}$			±3		ppm/°C
1.3.36.	Offset error after calibration [1)]	V_{OFFSET_C}	Normal Mode chop on, external short (VSSA)	-2		2	µV
			Low-Power State, chop on, external short (VSSA)	-0.6		+0.6	µV
1.3.37.	Offset error drift [1)]	$V_{OFFSET_DRIFT_C}$	Chop on		±20		nV/°C
			Chop off		±80		nV/°C
1.3.38.	Output noise with chop on [1)]	V_{NOISE_C}	Gain = 512, conversion rate = 10Hz		1.1		μV^{RMS}
			Gain = 512, conversion rate = 1kHz		1.1		μV^{RMS}
			Gain = 32, conversion rate = 1kHz		3		μV^{RMS}
			Gain = 4, conversion rate = 1kHz		11		μV^{RMS}

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No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
1.3.39.	Current offset [1)]	I_{BAT_offset}	Chop on, gain = 512, R_{shunt} = 100µΩ			10	mA
1.3.40.	Resolution [1)]	I_{RES}	Chop on, gain = 512, R_{shunt} = 100µΩ	1			mA
Voltage Channel							
1.3.41.	Input signal range (at VBAT pin) [1)]	$Range_V$	Resistive divider (1:24)	0		28.8	V
1.3.42.	Input measurement range [1)]	$Range_{meas_V}$	Resistive divider (1:24)	3.6		28.8	V
1.3.43.	Input valid range for ADC [1)]	$Range_{ADC_V}$	Resistive divider (1:24)	0.15		1.2	V
1.3.44.	Voltage resistive divider ratio [1)]	$Ratio_V$			24		
1.3.45.	Resistor divider mismatch drift [1)]	$Ratio_mis_{drift_v}$			±3		ppm/°C
1.3.46.	Conversion rate [1), 2)]	$Rate_V$	Programmable	1		16000	Hz
1.3.47.	Oversampling ratio ($Sinc^4$ decimation filter) [1)]	OSR_V	Programmable	32		256	
1.3.48.	No missing codes [1)]	NMC_V		18			Bits
1.3.49.	Integral nonlinearity [1), 3)]	INL_V	Maximum input range		±10	±60	ppm of FSR [4)]
1.3.50.	Total gain error [1)] (includes resistor divider mismatch)	err_{PGA_V}		-0.25		0.25	%
1.3.51.	Gain drift [1)]	$err_drift_{PGA_V}$			±3		ppm/°C
1.3.52.	Offset error after calibration: Normal Mode [1)]	V_{OFFSET_V}	Chop on external short (1.25V)		200		µV
			Chop off external short (1.25V)		1		mV
1.3.53.	Offset error drift [1)]	$V_{OFFSET_DRIFT_V}$	Chop on		±10		µV/°C
			Chop off		±20		µV/°C

No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
1.3.54.	Output noise [1]	V_{NOISE_V}	Chop on gain = 1, conversion rate =10Hz		30	50	μV^{RMS}
			Chop on gain = 1, conversion rate = 1kHz		1		μV^{RMS}
Temperature Channel (External NTC/Reference Resistor and Internal Temperature Sensor)							
1.3.55.	Voltage drop over NTC resistor [1]	V_{NTC}		0		1.2	V
1.3.56.	Voltage drop over reference resistor [1]	V_{REF_Res}		0		1.2	V
1.3.57.	Conversion rate [1]	$Rate_T$	Programmable	1		16000	Hz
1.3.58.	Oversampling ratio ($Sinc^4$ decimation filter) [1]	OSR_T	Programmable	32		256	
1.3.59.	Integral nonlinearity [1), 3)]	INL_T	Maximum input range		±10	±60	ppm of FSR
1.3.60.	No missing codes [1]	NMC_T		16			Bit
1.3.61.	Offset error after ZSSC1750/51 calibration [1]	V_{OFFSET_T}	Normal Mode, chop on, external short (1.25V)	-100		100	µV
			Normal Mode, chop off, external short (1.25V)	-2		2	mV
1.3.62.	Offset error drift [1]	$V_{OFFSET_DRIFT_T}$	Chop on		±10		µV/°C
			Chop off		±20		µV/°C
1.3.63.	Output noise [1]	V_{NOISE_T}	Chop on, gain = 1, conversion rate =500Hz			50	μV^{RMS}
1.3.64.	Resistor to ground at pin NTL [1]	GND_{RES}			50		kΩ
1.3.65.	Internal temperature sensor resolution [1]	RES_{ITS}		-	1/32	-	°C/LSB
1.3.66.	Linearity error of internal temperature sensor [1]	LE_{ITS}		-	±2	-	°C

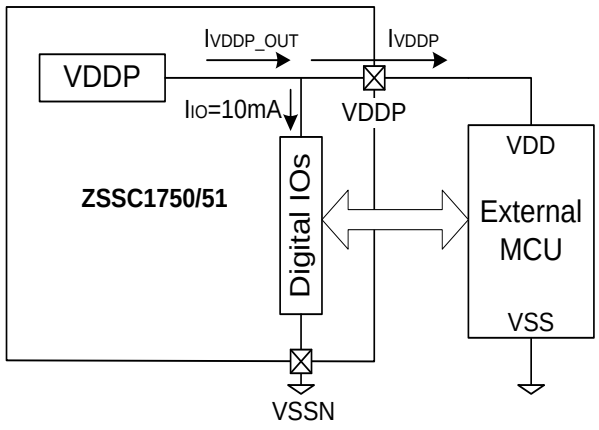
No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Power-on Reset (POR)							
1.3.67.	Power-on reset threshold	V_{PORB}	At V_{DDE}	2.75	3.0	3.6	V
1.3.68.	Power-on-reset hysteresis	$Hyst_{PORB}$	At V_{DDE}		300		mV
1.3.69.	Low-voltage flag	low_voltage	At V_{DDE}	1.8	2.0	2.3	V
1.3.70.	V_{DDP} high [1)] (for VDDP = 3.3V configuration)	vddp_high	At V_{DDE}	3.9	4.05	4.2	V
1.3.71.	V_{DDP} high hysteresis [1)]	$Hyst_{VDDP_high}$	At V_{DDE}		400		mV
Low-Power Voltage Reference							
1.3.72.	Reference bandgap voltage: low-power	V_{BGL}		1.16		1.32	V
1.3.73.	Accuracy (including temperature drift)			-3		3	%
1.3.74.	Temperature coefficient [1)]	TC_{VBGL}			50		ppm/K
Low-Power (LP) Oscillator							
1.3.75.	Frequency	f_{LPO}			125		kHz
1.3.76.	Accuracy (including temperature drift) [1)]			-3		3	%
High-Precision Voltage Reference							
1.3.77.	Reference bandgap voltage: high-precision	V_{BGH}	Uncalibrated	1.16		1.32	V
1.3.78.	Temperature coefficient [1)]	TC_{VBGH}	Calibrated	-20	±5	+20	ppm/K
High-Precision (HP) Oscillator							
1.3.79.	Frequency	f_{HPO}			20		MHz
1.3.80.	Accuracy (including temperature drift) [1)]			-1		1	%
LIN Interface							
1.3.81.	Current limitation for driver dominant state [1)]	I_{BUS_LIM}	*LIN spec 2.1 Param 12*	40		200	mA
1.3.82.	Input leakage current, dominant state, driver off [1)]	$I_{BUS_PAS_dom}$	*LIN spec 2.1 Param 13*	-1			mA
1.3.83.	Input leakage current, recessive state, driver off [1)]	$I_{BUS_PAS_rec}$	*LIN spec 2.1 Param 14*			20	µA

No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
1.3.84.	Control unit disconnected from ground [1)]	$I_{BUS_NO_GND}$	*LIN spec 2.1 Param 15*	-1		1	mA
1.3.85.	V_{BAT} supply disconnected [1)]	$I_{BUS_NO_BAT}$	*LIN spec 2.1 Param 16*			100	µA
1.3.86.	Receiver dominant state, V_{DDE} > 7V [1)]	V_{BUSdom}	*LIN spec 2.1 Param 17*			0.4	V_{DDE}
1.3.87.	Receiver recessive state, V_{DDE} > 7V [1)]	V_{BUSrec}	*LIN spec 2.1 Param 18*	0.6			V_{DDE}
1.3.88.	Center of receiver threshold [1)]	V_{BUS_CNT}	*LIN spec 2.1 Param 19*	0.475	0.5	0.525	V_{DDE}
1.3.89.	Receiver hysteresis voltage [1)]	V_{HYS}	*LIN spec 2.1 Param 20*			0.175	V_{DDE}
1.3.90.	Voltage drop at serial diodes [1)]	$V_{SerDiode}$	*LIN spec 2.1 Param 21*	0.4	0.7	1	V
1.3.91.	Battery shift [1)]	V_{SHIFT_BAT}	*LIN spec 2.1 Param 22*			0.115	V_{BAT}
1.3.92.	Ground shift [1)]	V_{BUS_GND}	*LIN spec 2.1 Param 23*			0.115	V_{BAT}
1.3.93.	Difference between battery shift and ground shift [1)]	$V_{SHIFT_Difference}$	*LIN spec 2.1 Param 24*	0		8	%
1.3.94.	LIN pull-up resistor [1)]	R_{SLAVE}	*LIN spec 2.1 Param 26*	20	30	47	kΩ
1.3.95.	Duty cycle 1 [1)]	D1	*LIN spec 2.1 Param 27*	0.396			
1.3.96.	Duty cycle 2 [1)]	D2	LIN spec 2.1 Param 28			0.581	
1.3.97.	Duty cycle 3 [1)]	D3	LIN spec 2.1 Param 29	0.417			
1.3.98.	Duty cycle 4 [1)]	D4	LIN spec 2.1 Param 30			0.590	
1.3.99.	Receiver propagation delay [1)]	T_{RX_pdr}	LIN spec 2.1 Param 31			6	µs
1.3.100.	Symmetry receiver propagation delay, rising/falling edge [1)]	T_{RX_sym}	LIN spec 2.1 Param 32	-2		2	µs

No.	Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
1.3.101.	Capacitance of slave node [1)]	C_{SLAVE}	LIN spec 2.1 Param 23			250	pF
1.3.102.	LIN pin capacitance [1)]	C_{LIN}		-	-	30	pF

1) Not tested in production test; given by design and/or characterization.
2) Depends on chopping and OSR settings.
3) FSR = 1.2V
4) FSR = Full-scale input range of the ADCs. The input range is given in specification 1.3.26 for current, 1.3.41 for voltage, and 1.3.55 and 1.3.56 for external temperature.

Figure 1.1 Measurement Method for Determining VDDP Pin Current Capability



1.4 Timing Parameters

Table 1.4 Timing Parameters

No	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
	SPI Protocol Timing (See Figure 1.2)						
1.4.1.	SPI operational frequency [1)]	f_{SPI}		-	-	8	MHz
1.4.2.	SCLK clock period for registers read/write [1)]	$t_{SCLKPreg}$		125	-	-	ns
1.4.3.	SCLK clock period for OTP read [1)]	$t_{SCLKPotp}$		200	-	-	ns
1.4.4.	SCLK clock pulse width [1)]	t_{SCLKW}		40	50	60	% t_{SCLKP}
1.4.5.	CSN setup time [1)]	t_{CSU}		50	-	-	ns
1.4.6.	CSN hold time [1)]	t_{CHD}		50	-	-	ns
1.4.7.	CSN high time [1)]	t_{CHI}		300	-	-	ns
1.4.8.	MOSI data setup time [1)]	t_{DSU}		20	-	-	ns
1.4.9.	MOSI data hold time [1)]	t_{DHD}		10	-	-	ns
1.4.10.	MISO data access time [1)]	t_{DACC}		-	-	25	ns
Timer 0 (Sleep Timer)							
1.4.11.	Time interval [1)]	SLPTI1	Programmable	0.1		6553.5	s
1.4.12.	Time interval with post-scaler [1)]	SLPTI2	Programmable			466	h
1.4.13.	Resolution [1)]	$SLPTI1_{res}$			100		ms
Timer 1 (Watchdog Timer WDT)							
1.4.14.	Time interval [1)]	WDTI	Programmable	8µ		6553.5	s
1.4.15.	Resolution [1)]	$WDTI_{res}$	Programmable	0.008		100	ms
Startup Timing (See Figure 1.3)							
1.4.16.	PORB delay until analog blocks settled[1)]	T_{PORB_dly}				1	ms

1) Not tested in production test; given by design and/or characterization.

Figure 1.2 SPI Protocol Timing

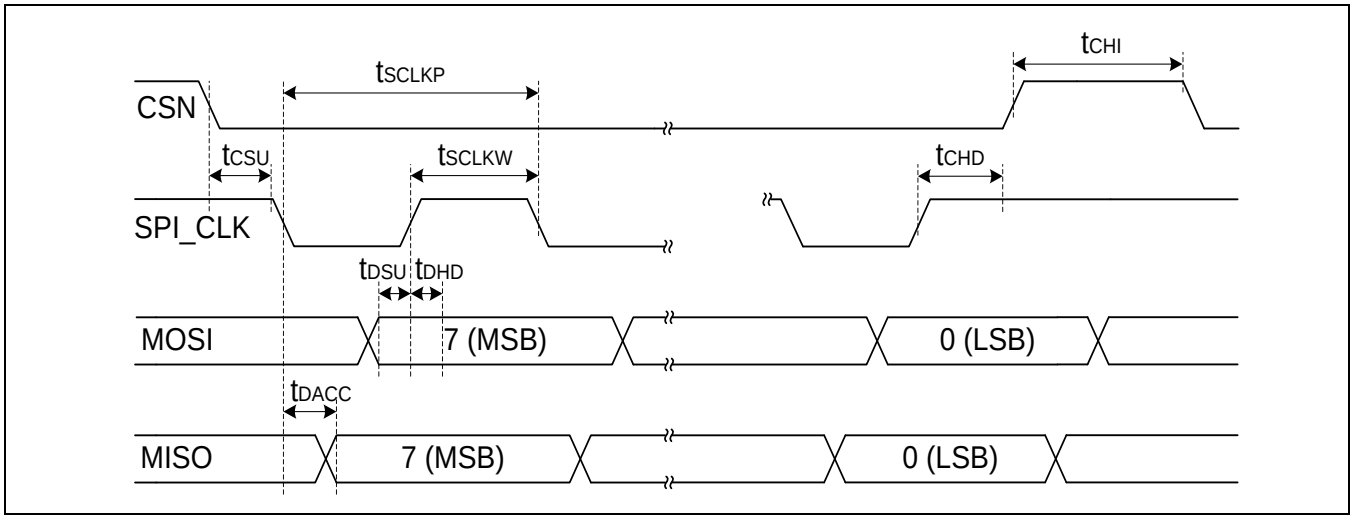
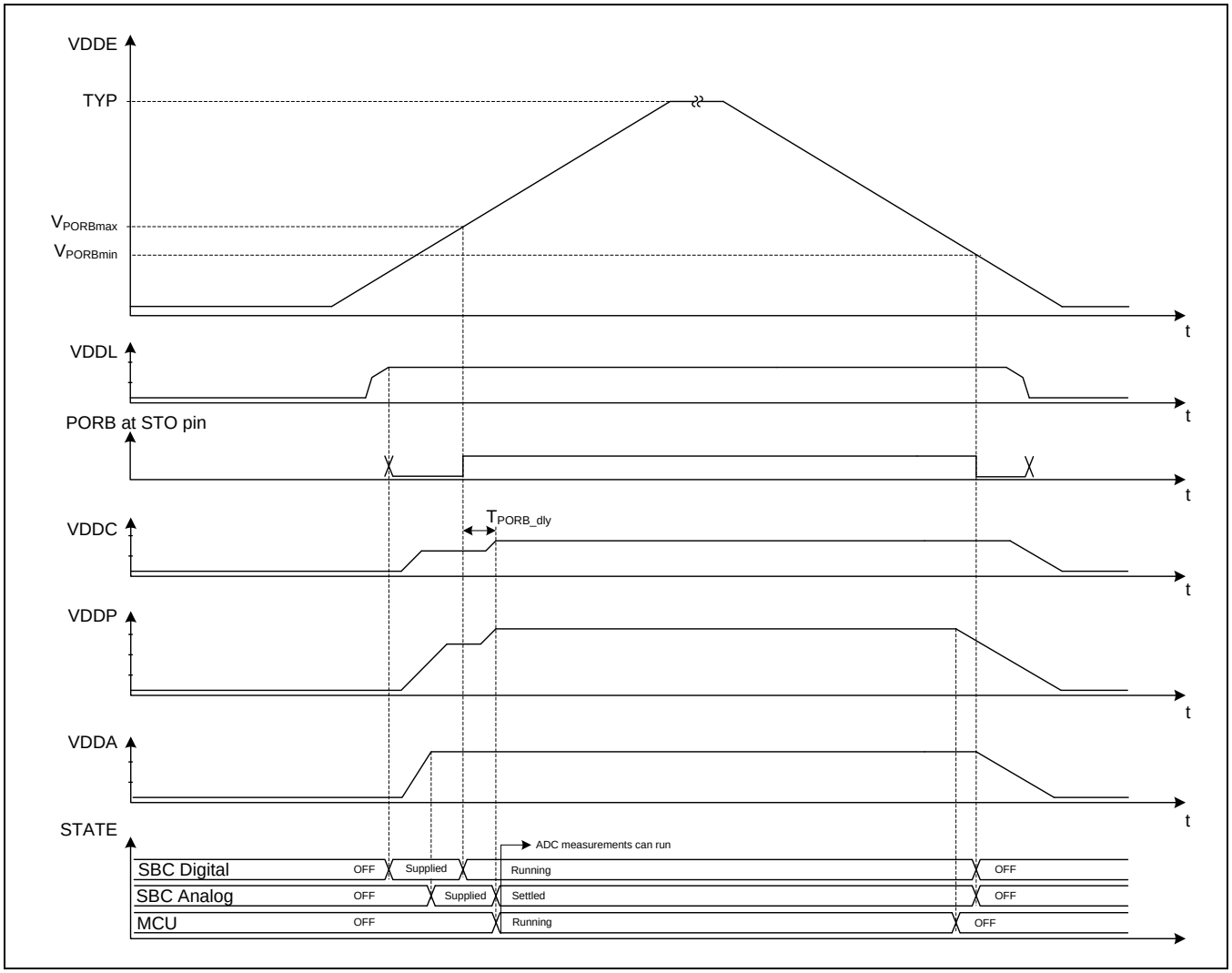


Figure 1.3 ZSSC1750/51 Power-Up and Power-Down Sequence



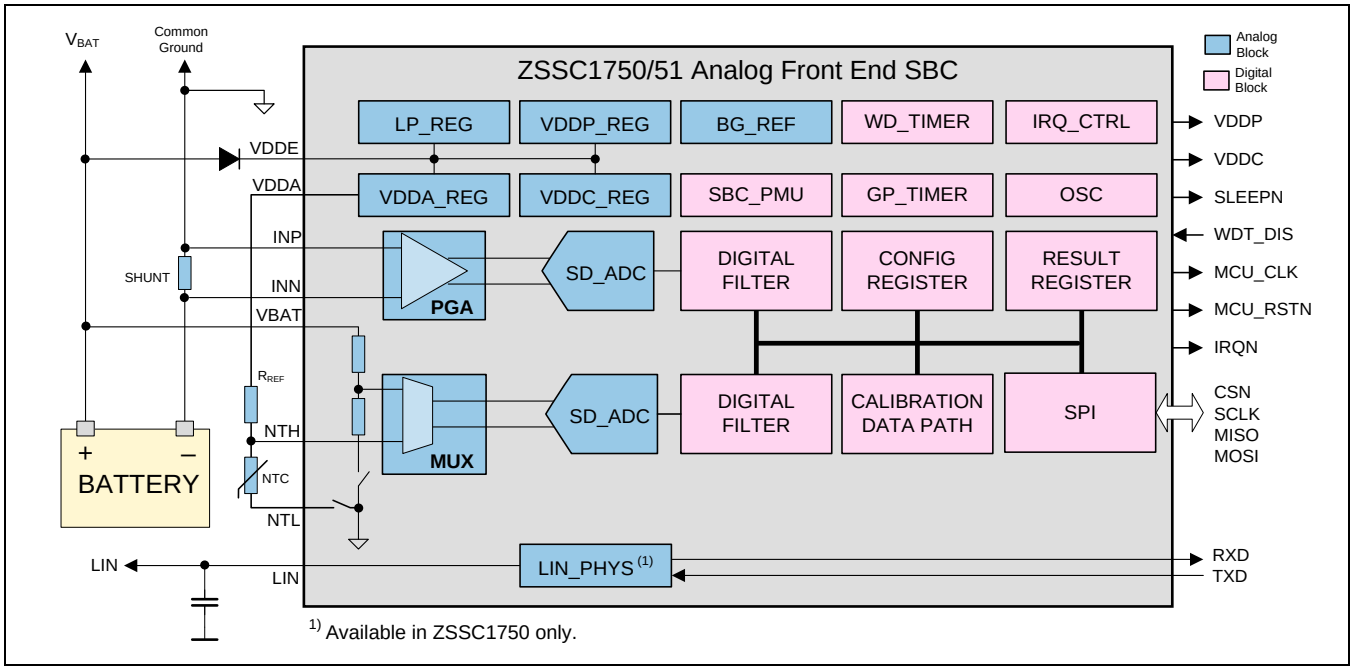
2 Circuit Description

2.1 Overview

The ZSSC1750/51 is a data acquisition System Basis Chip (SBC) assembled in a PQFN36 6x6mm package. It contains a high voltage circuit, analog input stage including peripheral blocks, sigma-delta (ΣΔ) ADCs (SD_ADC), digital filtering, and a LIN transceiver (for ZSSC1750 only). Communication between an external microcontroller and the SBC is handled by a Serial Peripheral Interface (SPI). The functions of the ZSSC1750/51 are controlled by register settings. The circuit starts after power-on with default register and calibration settings that can be overwritten by the user's software.

One input channel measures I_{BAT} via the voltage drop at the external shunt resistor. The second channel measures V_{BAT} and the temperature. By simultaneously measuring V_{BAT} and I_{BAT}, it is possible to dynamically determine Rdi, which is correlated with the state of health (SOH) of the battery. By integrating I_{BAT}, it is possible to determine the state of charge (SOC) of the battery. These are the fundamental parameters for an intelligent battery sensor. The necessary microcontroller and the software for determining these parameters is not part of the ZSSC1750/51.

Figure 2.1 Functional Block Diagram

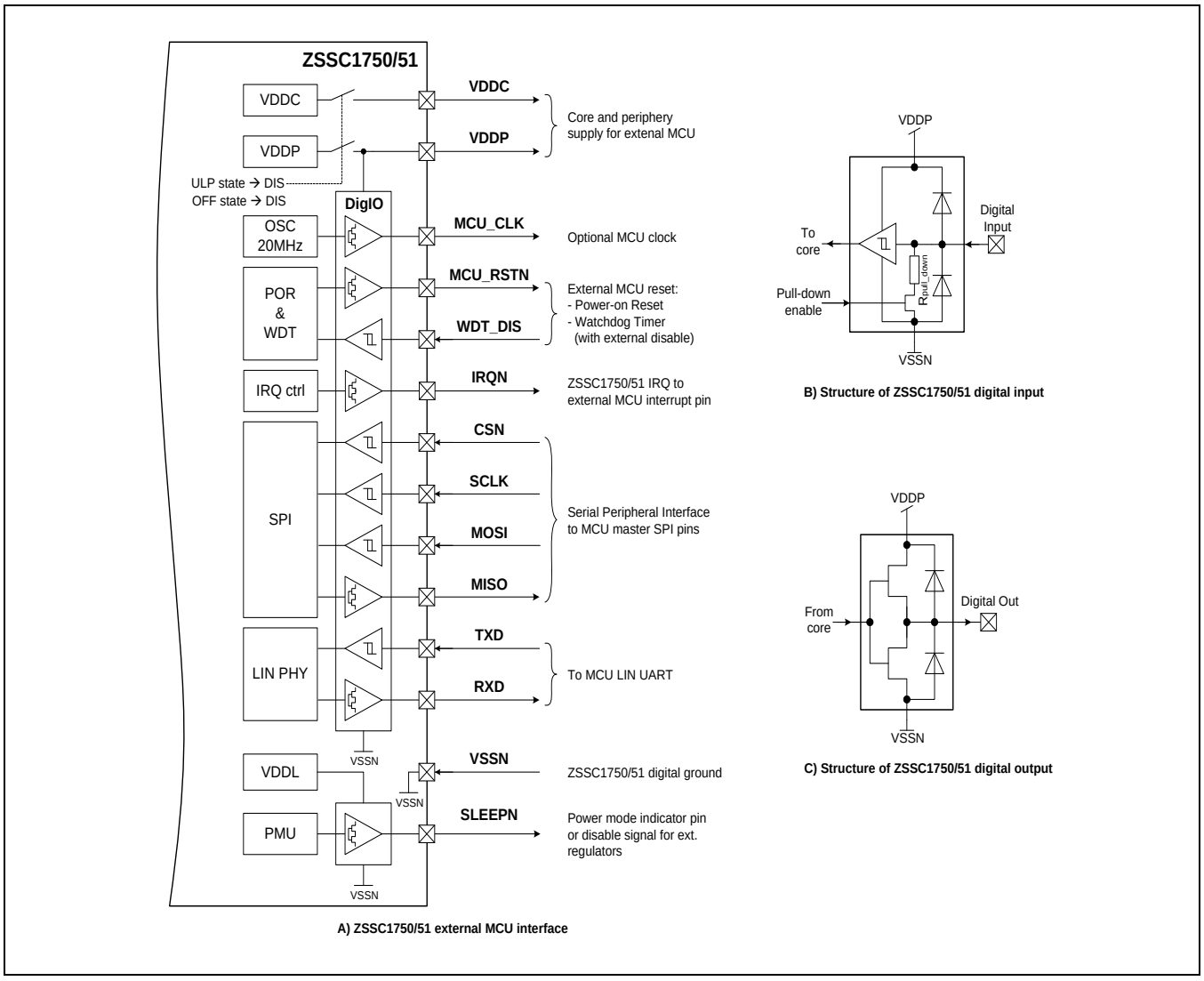


During the Standby Mode and the system's Sleep Mode (e.g., engine is off), the system periodically measures the values to monitor the discharge of the battery (see section 3.7 regarding modes). Measurement cycles are controlled by the user's software and are dependent on the detected events. The ZSSC1750/51 is designed for low current consumption during Sleep Mode in the range of less than 60µA.

2.2 SBC-to-MCU Interface Pins

The ZSSC1750/51 connects to the external microcontroller (MCU) using pins shown in Figure 2.2-A. ZSSC1750/51 pins can be classified in three categories: digital IOs, microcontroller supply pins, and the power state indicator pin.

Figure 2.2 ZSSC1750/51 Digital IO Interface



2.2.1 Digital I/Os

The digital I/O pins include the SPI interface pins, MCU clock, rest and interrupt pins, LIN UART pins (for ZSSC1750 only), and watchdog timer disable pin.

All digital input pins of the ZSSC1750/51 feature a Schmitt trigger (see Figure 2.2-B), as well as configurable pull-down resistors and protection diodes. The pull-down resistors have values specified by parameter 1.3.16. They are enabled after power-on-reset and can be further controlled via the `pullResEna` register (see section 3.11.1.1).

All digital output pins of the ZSSC1750/51 have a push-pull stage and protection diodes connected as shown in Figure 2.2-C.

All digital I/Os are supplied by the VDDP voltage, which is switched off when the ZSSC1750/51 is in the ULP or OFF State (see section 2.3); i.e. the I/Os are also off in this state.

Note: In order to avoid parasitic supply of the digital I/O circuitry when the ZSSC1750/51 is in the ULP or OFF State, the digital outputs of the external microcontroller should be disabled. This is valid when the external micro-controller is not supplied by the ZSSC1750/51.

2.2.2 External Microcontroller (MCU) Supply Pins

The ZSSC1750/51 provides two separate regulators for the external microcontroller supply. The VDDP regulator provides 3.3V, and VDDC provides 1.8V. Both voltages are switched off when the ZSSC1750/51 is in the ULP or OFF State. For more information regarding the VDDP and VDDC regulators, including trimming options, refer to sections 3.12.5 and 3.12.6. The current capability of the VDDP and VDDC pins is specified by parameters 1.3.11 and 1.3.13 respectively.

2.2.3 SLEEPN Power State Indicator Pin

The ZSSC1750/51 features a SLEEPN pin that indicates the power state of the ZSSC1750/51 (see section 2.3). When the ZSSC1750/51 is in the full power (FP) state or low power (LP) state, the SLEEPN pin is HIGH; when the state is ULP or OFF, SLEEPN is LOW. In order to remain powered in these states, the SLEEPN pin circuitry is supplied by the VDDL regulator. When HIGH, the SLEEPN pin has a 1.8V output voltage level; the HIGH and LOW levels are specified with parameters 1.3.20 and 1.3.21.

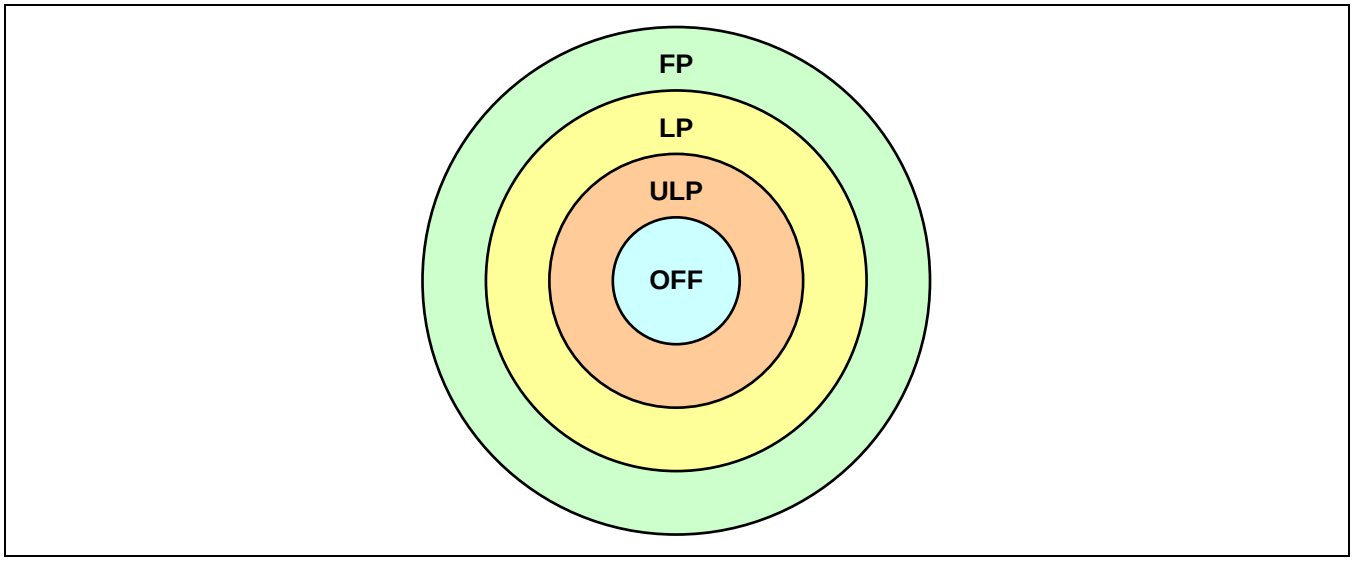
In the application, the SLEEPN pin can be connected to the external microcontroller (if it remains powered in system Sleep Mode), or it can be used for disabling an external circuitry when the ZSSC1750/51 goes into one of the power saving modes. Depending on the application specifics, an external buffer (e.g., a transistor) might be needed for the SLEEPN pin for a proper level or current conditioning.

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2.3 System Power States

There are four different power states implemented in the ZSSC1750/51 as illustrated in Figure 2.3. Full details are given in section 3.7.

Figure 2.3 ZSSC1750/51 Power States



2.3.1 Full Power State (FP)

The ZSSC1750/51 enters the Full Power (FP) State after power-on reset or after wake-up. In this power state, the ZSSC1750/51 is fully operational and the external microcontroller is supplied and running (see section 3.7). In the FP State, the ADCs are fully powered and running on the 4MHz base clock, which is generated from the 20MHz high-precision oscillator.

Of the four power states, the FP State consumes the most power. The MCU software can trigger the power management unit (PMU) inside the ZSSC1750/51 to enter any other power state (see section 3.7).

2.3.2 Low Power State (LP)

The Low Power (LP) State is intended for scenarios where the ZSSC1750/51 will only perform low-power measurements without any operation by the external microcontroller (MCU). For its ADC operations, it uses a 125kHz clock from the low-power oscillator as the base clock. The system can wake up from this power state via any enabled interrupt of the SBC as well as via an MCU reset generated by the watchdog timer.

Note: For any SBC interrupt source that will wake up the system, the corresponding interrupt source must be enabled in the SBC. Note that the SBC rejects the power-down command when an enabled interrupt source inside the SBC is already active.

When the system enters the LP State from the FP State, the microcontroller software must first enable the required interrupt sources for later wake-up in the ZSSC1750/51 SBC and the microcontroller and it must set the `pdState` bit in the `pwrCfgLp` register (see Table 3.19) followed by a gotoPd command (see section 3.7 and Table 3.20). A rising edge on the CSN line triggers the SBC to enter its LP State.

When any of the enabled interrupts becomes active, the system returns to the FP State and continues the software execution.

Note: Do not release the CSN line by software at the end of sending a power-down command to avoid the MCU clock being stopped by the SBC at an intermediate state.

2.3.3 Ultra Low Power State (ULP)

The Ultra-Low Power (ULP) State is similar to the LP State except that the SBC also disables the power for the external microcontroller. This power state is intended for scenarios where the SBC will only perform low-power measurements without any operation running on the microcontroller. For the ZSSC1750/51's ADC operations in this state, it uses a 125kHz clock from the low-power oscillator as the base clock. The system can wake up from this power state by any enabled interrupt of the SBC. The microcontroller is reset upon wake up by the SBC to guarantee correct start up. This means that the microcontroller software starts again from address 0_{HEX} after wake up, not at the position where it was stopped.

Note: For any SBC interrupt source that will wake up the system, the corresponding interrupt source must be enabled in the SBC. Note that the SBC rejects the power-down command when an enabled interrupt source inside the SBC is already active.

When the system enters the ULP State from the FP State, the microcontroller software must first enable the required interrupt sources for later wake-up in the SBC and the microcontroller and it must set the `pdState` bit in `pwrCfgLp` register (see Table 3.19) followed by a gotoPd command (see section 3.7 and Table 3.20). A rising edge on the CSN line triggers the SBC to enter its ULP State. When any of the enabled interrupts becomes active, the system returns to FP State and restarts the microcontroller software execution.

Note: Do not release the CSN line by software at the end of sending a power-down command to avoid the microcontroller clock being stopped by the SBC at an intermediate state.

2.3.4 OFF Power State

The OFF power state has the lowest power consumption: no measurements can be performed as all oscillators are stopped. This power state is intended for scenarios where no measurements will be performed and the system will consume as little power as possible. The system can wake up from this power state only by receiving a wakeup frame over the LIN interface (only for the ZSSC1750) or after a power-on reset (for ZSSC1750/51). The external microcontroller is reset at wake up by the SBC to guarantee correct start up. This means that the microcontroller's software starts again from address 0_{HEX} after wake up, not at the position where it was stopped.

Note: For any SBC interrupt source that will wake up the system, the corresponding interrupt source, e.g. the LIN wakeup interrupt (for the ZSSC1750 only), must be enabled inside the SBC. Note that the SBC rejects the power-down command when an enabled interrupt source in the SBC is already active.

When the system enters the OFF power state from the FP State, the microcontroller software must first enable the required interrupt source in the SBC, e.g. the LIN interrupt (for the ZSSC1750 only), and the microcontroller and must set the `PdState` bit in register `pwrCfgLp` (see Table 3.19) followed by a gotoPD command (see Table 3.20). A rising edge on the CSN line triggers the SBC to enter its OFF State. When any of the enabled interrupts becomes active, the ZSSC1750/51 returns to the FP State and the external microprocessor can restart its software execution.

Note: Do not release the CSN line by software at the end of sending a power-down command to avoid the MCU clock being stopped by the SBC at an intermediate state.

3 ZSSC1750/51 Functional Block Descriptions

3.1 Serial Peripheral Interface (SPI Slave)

The ZSSC1750/51 is fully controllable by an external microcontroller via an integrated four-wire SPI slave. It only operates in a single mode when both the clock polarity and the clock phase are 1 (the clock is high when inactive, data is sent on the falling SPI clock edge, and data is sampled on the rising SPI clock edge). The accessible registers of the SBC as well as the one-time programmable (OTP) memory can be read via the SPI. The internal status information of the SBC is also shifted-out during the address and length bytes of the implemented SPI protocol (see Figure 3.1). Read and write burst accesses of up to 128 bytes are supported.

The SPI chip-select line CSN must be low during any transfer until the complete transfer has finished. This is needed as the CSN input is not only used as an enable signal but also as an asynchronous reset for part of the SPI front-end. The reason for this is to be able to set the SPI back to a defined state via the microcontroller as well as to extract status information without needing to access any register. The CSN input can be kept low between two transfers. The CSN input must only be driven high for execution of the “go-to-power-down” command after the required register settings have been completed.

Note: A high level at CSN resets the internal SPI state machine.

3.1.1 SPI Protocol

The SPI slave module only operates with a clock polarity of 1 (SCLK is high when no transfer is active) and with a clock phase of 1 (data is sent on the falling edge; data is sampled on the rising edge). For any access, the CSN input must be low. At the end of any read access, the CSN input can be kept low. For write accesses that change the power state, the CSN input must be driven high at the end of the write access; it can be kept low for write accesses to other registers. During an SPI access, the CSN input must be kept low.

Important: Driving the CSN input high during a read transfer can cause a loss of data.

In each SPI transfer, 1 to 128 bytes can be read or written in one burst access. All bytes are sent and received with the MSB first. As shown in Figure 3.1, each SPI transfer starts with two bytes sent by the master while the slave sends back status information in parallel. The first of the two bytes sent by the master is the address byte containing the first address to be accessed. When multiple bytes are read or written, the received SPI address is internally incremented for each data byte. The second byte starts with the access type of the transfer (1 = write; 0 = read) followed by the 7-bit length field indicating the number of data bytes that will be read or written. The exception is the length value of 0, which is interpreted by the slave SPI as 128 bytes.

The status information sent back by the slave during the address and length bytes starts with a fixed value of A_{HEX}. This can be used to detect whether the connection is still present. The next bits sent are the slave status word (SSW), which is 12 bits of actual status information.

The 12 SSW bits have the following definitions:

SSW[11]: Value of the low-voltage flag

SSW[10:8]: Reset status

SSW[7]: Watchdog active flag

SSW[6]: Low-power oscillator trimming circuit active

SSW[5]: Voltage/temperature ADC active

SSW[4]: Current ADC active

SSW[3]: LIN short protection active (applicable for ZSSC1750 only)

SSW[2]: LIN TXD timeout protection active (applicable for ZSSC1750 only)

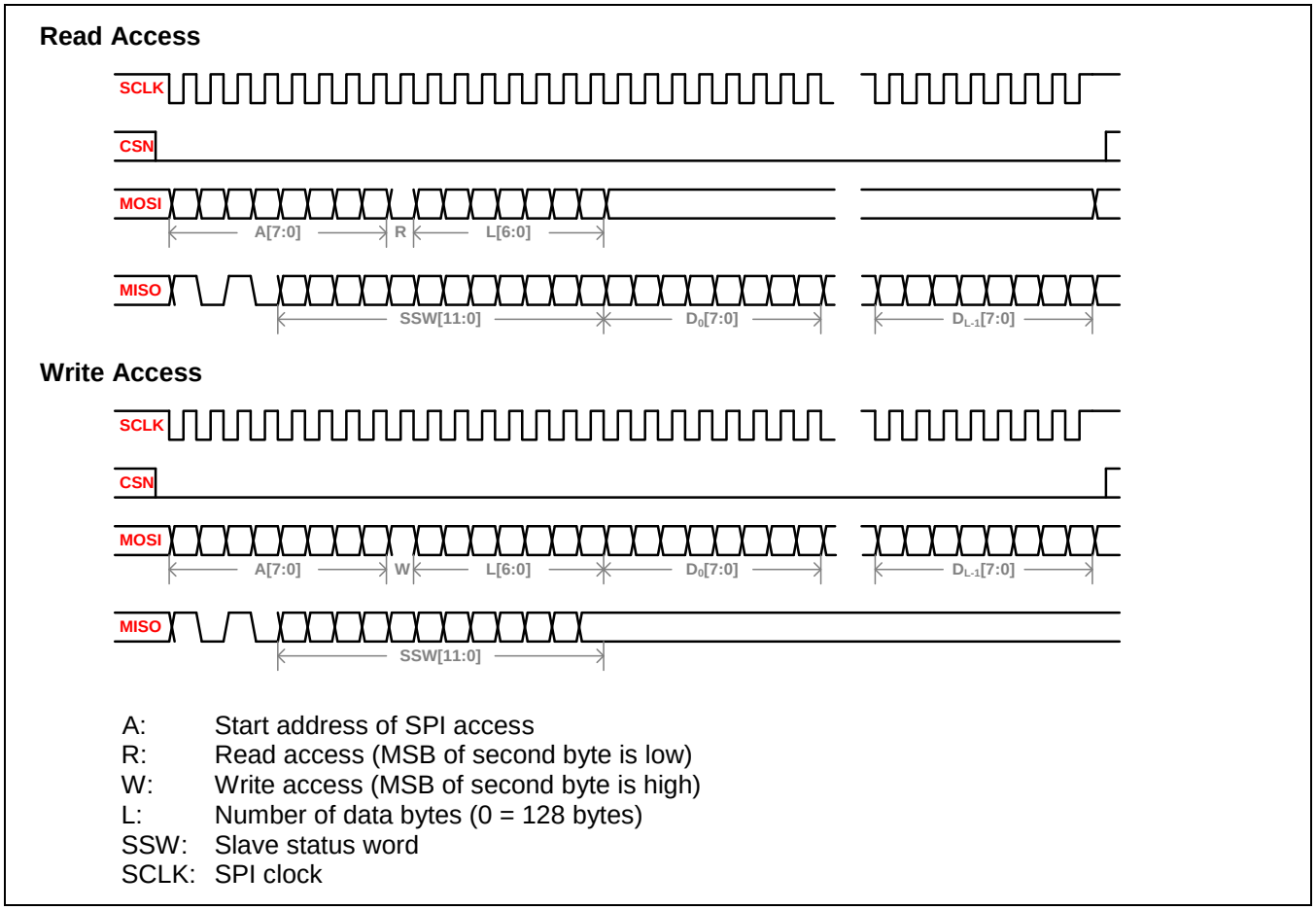
SSW[1]: Readable sleep timer value valid

SSW[0]: OTP download procedure active

Note: After the external microcontroller has been reset, the user's software can read the low-voltage flag and the reset status by a single-byte transfer (important: send only the address byte) to shorten the initialization phase (e.g., when a reset was caused by a wake-up event) without needing to read or write further bytes including the length byte.

After the address byte and length byte are sent by the master, either the master (write transfer) or the slave (read transfer) is transmitting data. The slave ignores all incoming bits while it is sending the requested number of data bytes (read), and the data bytes returned during a write transfer have no meaning. Figure 3.1 shows a read and a write burst access to the SBC.

Figure 3.1 Read and Write Burst Access to the SBC



A: Start address of SPI access
R: Read access (MSB of second byte is low)
W: Write access (MSB of second byte is high)
L: Number of data bytes (0 = 128 bytes)
SSW: Slave status word
SCLK: SPI clock

3.2 SBC Register Map (RESULT REGISTER Block and CONFIG REGISTER Block)

Table 3.1 defines the registers in the SBC. In the "Access" column, the following abbreviations indicate the read/write status of the registers: RC = read-clear; RO = read-only; RW = readable and writable; WO = write-only; W1C = write-one-to-clear, RWS = read-write-set. For more details, see the subsequent sections for the individual registers in section 3.

Important: There is a distinction between "unused" and "reserved" addresses. No problem occurs when writing to unused addresses, but writing 0_{HEX} to unused addresses for future expansions is recommended. Reserved addresses must always be written with the given default value.

Table 3.1 SBC Register Map

Name	Address	Order	Default	Access	Short Description
irqStat	00_{HEX}	LSB	00_{HEX}	RC	Interrupt status register
	01_{HEX}	MSB	00_{HEX}	RC	
adcCdat	02_{HEX}	LSB	00_{HEX}	RO	ADC result register of a single current measurement
	03_{HEX}	---	00_{HEX}	RO	
	04_{HEX}	MSB	00_{HEX}	RO	
adcVdat	05_{HEX}	LSB	00_{HEX}	RO	ADC result register of a single voltage measurement
	06_{HEX}	---	00_{HEX}	RO	
	07_{HEX}	MSB	00_{HEX}	RO	
adcRdat	08_{HEX}	LSB	00_{HEX}	RO	ADC result register of a single temperature measurement by reading a voltage across the reference resistor (external temperature measurement only)
	09_{HEX}	MSB	00_{HEX}	RO	
adcTdat	$0A_{HEX}$	LSB	00_{HEX}	RO	ADC result register of a single temperature measurement by reading a voltage across the NTC resistor (external temperature measurement) or of a differential voltage (VPTAT – VBGH; internal temperature measurement)
	$0B_{HEX}$	MSB	00_{HEX}	RO	
adcCaccu	$0C_{HEX}$	LSB	00_{HEX}	RO	Accumulator register for current measurements
	$0D_{HEX}$	---	00_{HEX}	RO	
	$0E_{HEX}$	---	00_{HEX}	RO	
	$0F_{HEX}$	MSB	00_{HEX}	RO	
adcVaccu	10_{HEX}	LSB	00_{HEX}	RO	Accumulator register for voltage measurements
	11_{HEX}	---	00_{HEX}	RO	
	12_{HEX}	MSB	00_{HEX}	RO	
adcCmax	13_{HEX}	LSB	00_{HEX}	RO	Maximum current value measured in configured measurement sequence
	14_{HEX}	MSB	80_{HEX}	RO	
adcCmin	15_{HEX}	LSB	FF_{HEX}	RO	Minimum current value measured in configured measurement sequence
	16_{HEX}	MSB	$7F_{HEX}$	RO	

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Name	Address	Order	Default	Access	Short Description
adcVmax	17_{HEX}	LSB	00_{HEX}	RO	Maximum voltage value measured in configured measurement sequence
	18_{HEX}	MSB	80_{HEX}	RO	
adcVmin	19_{HEX}	LSB	FF_{HEX}	RO	Minimum voltage value measured in configured measurement sequence
	$1A_{HEX}$	MSB	$7F_{HEX}$	RO	
adcCrcv	$1B_{HEX}$	LSB	00_{HEX}	RO	Counter register containing the number of current measurements
	$1C_{HEX}$	MSB	00_{HEX}	RO	
adcCtcv	$1D_{HEX}$	---	00_{HEX}	RO	Counter register containing the number of current measurements greater than or equal to the threshold
adcVrcv	$1E_{HEX}$	---	00_{HEX}	RO	Counter register containing the number of voltage measurements
Unused	$1F_{HEX}$	---	00_{HEX}	---	---
sleepTCurCnt	20_{HEX}	LSB	00_{HEX}	RO	Current sleep timer value
	21_{HEX}	MSB	00_{HEX}	RO	
Unused	22_{HEX} to $2F_{HEX}$	---	00_{HEX}	---	---
adcCgan	30_{HEX}	LSB	00_{HEX}	RW	Digital gain correction for current channel
	31_{HEX}	---	00_{HEX}	RW	
	32_{HEX}	MSB	80_{HEX}	RW	
adcCoff	33_{HEX}	LSB	00_{HEX}	RW	Digital offset correction for current channel
	34_{HEX}	---	00_{HEX}	RW	
	35_{HEX}	MSB	00_{HEX}	RW	
adcVgan	36_{HEX}	LSB	00_{HEX}	RW	Digital gain correction for voltage channel
	37_{HEX}	---	00_{HEX}	RW	
	38_{HEX}	MSB	80_{HEX}	RW	
adcVoff	39_{HEX}	LSB	00_{HEX}	RW	Digital offset correction for voltage channel
	$3A_{HEX}$	---	00_{HEX}	RW	
	$3B_{HEX}$	MSB	00_{HEX}	RW	
adcTgan	$3C_{HEX}$	LSB	00_{HEX}	RW	Digital gain correction for temperature channel
	$3D_{HEX}$	MSB	80_{HEX}	RW	
adcToff	$3E_{HEX}$	LSB	00_{HEX}	RW	Digital offset correction for temperature channel
	$3F_{HEX}$	MSB	00_{HEX}	RW	
adcCrcl	40_{HEX}	LSB	00_{HEX}	RW	Number of current measurements before the ready strobe is generated
	41_{HEX}	MSB	00_{HEX}	RW	

Name	Address	Order	Default	Access	Short Description
adcCrth	42_{HEX}	LSB	00_{HEX}	RW	Absolute current value is compared to this threshold in Current Threshold Comparator Mode
	43_{HEX}	MSB	00_{HEX}	RW	
adcCtcl	44_{HEX}	---	00_{HEX}	RW	Number of current measurements greater than or equal to the threshold before the set interrupt strobe is generated
adcVrcl	45_{HEX}	---	00_{HEX}	RW	Number of voltage measurements before ready strobe is generated
adcVth	46_{HEX}	LSB	00_{HEX}	RW	Voltage threshold level for Threshold Comparator (unsigned) or Accumulator (signed) Modes
	47_{HEX}	MSB	00_{HEX}	RW	
adcCaccth	48_{HEX}	LSB	00_{HEX}	RW	Accumulator threshold for current channel
	49_{HEX}	---	00_{HEX}	RW	
	$4A_{HEX}$	---	00_{HEX}	RW	
	$4B_{HEX}$	MSB	00_{HEX}	RW	
adcTmax	$4C_{HEX}$	---	00_{HEX}	RW	Upper threshold for temperature measurement
adcTmin	$4D_{HEX}$	---	00_{HEX}	RW	Lower threshold for temperature measurement
adcAcmp	$4E_{HEX}$	LSB	30_{HEX}	RW	ADC function enable register
	$4F_{HEX}$	MSB	00_{HEX}	RW	
adcGomd	50_{HEX}	---	10_{HEX}	RW	Reference voltage and sigma-delta modulator (SDM) configuration (see section 3.8)
adcSamp	51_{HEX}	---	00_{HEX}	RW	Oversampling and filter configuration
adcGain	52_{HEX}	---	00_{HEX}	RW	Gain configuration register for analog amplifiers
pwrCfgFp	53_{HEX}	---	00_{HEX}	RW	Power configuration register for Full Power (FP) State
irqEna	54_{HEX}	LSB	00_{HEX}	RW	Interrupt enable register
	55_{HEX}	MSB	00_{HEX}	RW	
adcCtrl	56_{HEX}	---	00_{HEX}	RW	ADC control register for Full Power State (FP)
adcPoCoGain	57_{HEX}	---	00_{HEX}	RW	Post-correction gain configuration
Unused	58_{HEX} - $5E_{HEX}$	---	00_{HEX}	---	---
discCvtCnt	$5F_{HEX}$	---	00_{HEX}	RW	Configuration register for some power-down states
sleepTAdcCmp	60_{HEX}	LSB	00_{HEX}	RW	Compare value for ADC trigger timer
	61_{HEX}	MSB	00_{HEX}	RW	
sleepTCmp	62_{HEX}	LSB	00_{HEX}	RW	Compare value for sleep timer
	63_{HEX}	MSB	00_{HEX}	RW	
pwrCfgLp	64_{HEX}	---	20_{HEX}	RW	Power configuration register for power-down states

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Name	Address	Order	Default	Access	Short Description
gotoPd	65_{HEX}	---	00_{HEX}	WO	Power-down activation register
Unused	66_{HEX} to 67_{HEX}	---	00_{HEX}	---	---
cmdExe	68_{HEX}	---	02_{HEX}	WO/RW	Command execution register
Unused	69_{HEX} to $6F_{HEX}$	---	00_{HEX}	---	---
wdogCnt	70_{HEX}	LSB	FF_{HEX}	RO	Current watchdog counter value
	71_{HEX}	MSB	FF_{HEX}	RO	
wdogPresetVal	72_{HEX}	LSB	FF_{HEX}	RW	Preset value for watchdog counter
	73_{HEX}	MSB	FF_{HEX}	RW	
wdogCfg	74_{HEX}	---	09_{HEX}	RW	Configuration register for watchdog counter
Unused	75_{HEX} to 77_{HEX}	---	00_{HEX}	---	---
lpOscTrimCnt	78_{HEX}	LSB	00_{HEX}	RO	Result counter of low-power oscillator trim circuit
	79_{HEX}	MSB	00_{HEX}	RO	
irefLpOsc	$7A_{HEX}$	---	52_{HEX}	RW	Trim value for low-power oscillator
lpOscTrim	$7B_{HEX}$	---	04_{HEX}	RW	Configuration register for trim circuit of LP oscillator
Unused	$7C_{HEX}$ to $7F_{HEX}$	---	00_{HEX}	---	---
swRst	80_{HEX}	---	00_{HEX}	WO	Software reset
Unused	81_{HEX} to AF_{HEX}	---	00_{HEX}	---	---
sdmClkCfgLp	$B0_{HEX}$	LSB	18_{HEX}	RW	Clock configuration for SDM clock in power-down state
	$B1_{HEX}$	MSB	00_{HEX}	RW	
sdmClkCfgFp	$B2_{HEX}$	LSB	08_{HEX}	RW	Clock configuration for SDM clock in Full-Power State (FP)
	$B3_{HEX}$	MSB	90_{HEX}	RW	
linCfg	$B4_{HEX}$	---	00_{HEX}	RW/W1C	ZSSC1750: Configuration for LIN control logic
					ZSSC1751: Not used **Important:** Must remain as default for ZSSC1751
linShortFilter	$B5_{HEX}$	---	$0F_{HEX}$	RW	ZSSC1750: Configuration for LIN short de-bounce filter
					ZSSC1751: Not used Important: Must remain as default for ZSSC1751
linShortDelay	$B6_{HEX}$	---	$4F_{HEX}$	RW	ZSSC1750: Configuration for LIN short TX-RX delay
					ZSSC1751: Not used Important: Must remain as default for ZSSC1751

Name	Address	Order	Default	Access	Short Description
linWuDelay	$B7_{HEX}$	---	14_{HEX}	RW	ZSSC1750: Configuration for LIN wake-up time
					ZSSC1751: Not used **Important:** Must remain as default for ZSSC1751
pullResEna	$B8_{HEX}$	---	FF_{HEX}	RW	Configuration register for pull-down resistors
funcDis	$B9_{HEX}$	---	00_{HEX}	RW	Disable bits for dedicated functions
versionCode	BA_{HEX}	LSB	01_{HEX}	RO	Version code
	BB_{HEX}	MSB	03_{HEX}	RO	
Unused	BC_{HEX} ... BF_{HEX}	---	00_{HEX}	---	---
pwrTrim	$C0_{HEX}$	---	$7C_{HEX}$	RW	Trim bits for voltage regulators and bandgap
irefOsc	$C1_{HEX}$	LSB	10_{HEX}	RW	Trim values for high-precision oscillator
	$C2_{HEX}$	MSB	40_{HEX}	RW	
ibiasLinTrim	$C3_{HEX}$	---	10_{HEX}	RW	ZSSC1750: Bias current trim register for LIN block
					ZSSC1751: Not used **Important:** Must remain as default for ZSSC1751
Reserved	$C4_{HEX}$	---	00_{HEX}	RW	---
Reserved	$C5_{HEX}$	---	00_{HEX}	RW	---
Reserved	$C6_{HEX}$	---	00_{HEX}	RW	---
Reserved	$C7_{HEX}$	---	00_{HEX}	RW	---
Reserved	$C8_{HEX}$	---	00_{HEX}	RW	---
Reserved	$C9_{HEX}$	---	00_{HEX}	RW	---
Reserved	CA_{HEX}	---	08_{HEX}	RW	---
Reserved	CB_{HEX}	---	00_{HEX}	RW	---
Reserved	CC_{HEX}	---	00_{HEX}	RW	---
Reserved	CD_{HEX}	---	00_{HEX}	RW	---
Reserved	CE_{HEX}	---	00_{HEX}	RW	---
Reserved	CF_{HEX}	---	00_{HEX}	RW	---
adcChan	$D0_{HEX}$	---	00_{HEX}	RW	Analog multiplexer configuration during test/ diagnosis
adcDiag	$D1_{HEX}$	---	80_{HEX}	RW	Enable register for test/diagnosis
currentSrcEna	$D2_{HEX}$	---	00_{HEX}	RW	Enable register for current sources
Reserved	$D3_{HEX}$	---	00_{HEX}	RW	---
Reserved	$D4_{HEX}$	---	00_{HEX}	RW	---
Reserved	$D5_{HEX}$	---	00_{HEX}	RW	---

Name	Address	Order	Default	Access	Short Description
Reserved	$D6_{HEX}$	---	00_{HEX}	RW	---
Reserved	$D7_{HEX}$	---	00_{HEX}	RW	---
Reserved	$D8_{HEX}$	---	00_{HEX}	RW	---
Reserved	$D9_{HEX}$	---	00_{HEX}	RW	---
Reserved	DA_{HEX}	---	$B8_{HEX}$	RW	---
Reserved	DB_{HEX}	---	00_{HEX}	RW	---
Reserved	DC_{HEX}	---	00_{HEX}	RW	---
Reserved	DD_{HEX}	---	00_{HEX}	RW	---
Reserved	DE_{HEX}	---	00_{HEX}	RW	---
Reserved	DF_{HEX}	---	00_{HEX}	RW	---
OTP	$E0_{HEX}$ to FF_{HEX}	---	---	RO	OTP raw data (see section 3.10.)

3.3 ZSSC1750/51 Clock and Reset Logic

3.3.1 Clock Sources

The ZSSC1750/51 SBC contains two different oscillators, a low-power oscillator (LP oscillator) providing a clock of 125kHz (typical) with an accuracy of ±3% and a high-precision oscillator (HP oscillator) providing a clock of 20MHz (typical) with an accuracy of ±1%. The low-power oscillator is always active except in the OFF State while the high-precision oscillator is only active in Full-Power State (FP). The clock from the high-precision oscillator is routed to the external microcontroller via the MCU_CLK pin.

There are three different internal clocks generated from the two clocks from the oscillators for the digital core of the SBC:

- **Low-power clock (lpClk):** This clock is directly driven by the low-power oscillator and has a frequency of 125kHz. It is used for the watchdog timer, the sleep timer, and the power management unit.
- **Divided clock (divClk):** This clock is derived from the high-precision oscillator and has a frequency of 4MHz. It is used for the register file, the low-power oscillator trimming circuit, the LIN support logic (ZSSC7150 only), and the OTP controller.
- **Multiplexed clock (muxClk):** This clock is identical to the divClk in the Full-Power State (FP) and identical to lpClk in the LP and ULP States. It is used for the ADC controller unit and the interrupt controller.

Both oscillators are trimmed during the production test, and the trim values are stored in the OTP memory (`IREF_OSC_0, IREF_OSC_1, IREF_OSC_2, IREF_OSC_3, IREF_LP_OSC;` see Table 3.67). The high precision oscillator is routed to the MCU_CLK pin, which can be used as a clock source for the external microcontroller or other digital devices, so it is important that the clock from the high-precision oscillator has the correct frequency. Therefore, the two trimming values for the high-precision oscillator are protected by redundancy inside the OTP. Software can check the validity of the trim values and the redundancy bits by reading the OTP raw data directly from the OTP via the SPI.

Note: The trimming values for both oscillators should also be stored by the user's external microcontroller so that the user's software is able to check the validity of the trimming values. On detection of errors inside the OTP, the user's software can write the correct values via SPI.

3.3.2 Trimming the Low-Power Oscillator

Because the clock from the low-power oscillator is less accurate than the clock from the high-precision oscillator, a trimming circuit is implemented that trims the low-power oscillator using the divided clock divClk. There are two options for trimming the low-power oscillator. One option is to allow the hardware to update the trim value for the low-power oscillator automatically so that no user interference is necessary. For this, the user only needs to set the `lpOscTrimEna` and `lpOscTrimUpd` bits in register `lpOscTrim` to 1 as well as setting the `lpOscTrimCfg` field as needed (see Table 3.4). The latter configuration value defines how many low-power clock periods are used for frequency calculation. While the trimming circuit is faster when fewer periods are used, the result of the frequency calculation is more accurate when more periods are used. In the first part of the trimming loop, the circuit determines the frequency of the low-power oscillator. When the measured frequency is too low, the hardware increments the trim value by 1; if it is too high, the hardware decrements the trim value by 1. Otherwise, the trim value remains unchanged. After changing the trim value, the hardware measures the (new) frequency. This algorithm is only stopped when the user's software clears the `lpOscTrimEna` bit (trimming logic stops after a final update) or when any low-power state is entered.

The second option is to use the trim circuit only to measure the frequency but to update the trim value via the user's software. This can be preferable when the target frequency is not equal to 125kHz. For this, the user only needs to set the `lpOscTrimEna` bit to 1 and set the `lpOscTrimUpd` bit to 0 as well as setting the `lpOscTrimCfg` field as needed. Next, the user must clear the `lpOscTrimEna` bit without changing the other values in the register and must wait until the hardware has finished to calculate the frequency (wait until `SSW[6]` is 0). By reading the `lpOscTrimCnt` register, the user can calculate the actual frequency of the low-power oscillator using the following formula:

$$f_{LP} = \frac{f_{HP}}{lpOscTrimCnt + 1} \cdot 2^{lpOscTrimCfg+2} \qquad f_{HP} = 4\,MHz \tag{1}$$

After determining the actual frequency, the user can change the trim value for the low-power oscillator `lpOscTrimVal` as required (see Table 3.3) and re-enable the trimming circuit to check the new frequency.

Note: The trimming circuit can be kept active when going to any low-power state. The PMU interrupts the trimming circuit on transition to the low-power state and restarts it after wakeup. This is needed as divClk is stopped in any low-power state.

3.3.3 Clock Trimming and Configuration Registers

3.3.3.1 Register "irefOsc" – Trim Values for the High-Precision Oscillator

Table 3.2 Register `irefOsc`

Name	Address	Bits	Default	Access	Description
irefTcOscTrim	$C1_{HEX}$	[4:0]	10000_{BIN}	RW	Trim value to minimize the temperature coefficient of the high-precision oscillator. **Note:** This value is automatically updated by the OTP controller after an SBC reset.
Unused		[6:5]	00_{BIN}	RO	Unused; always write as 0.
irefOscTrim[0]		[7]	0_{BIN}	RW	Trim value for the high-precision oscillator. The frequency of the high-precision oscillator increases (decreases) when this value is incremented (decremented). **Note:** This value is automatically updated by the OTP controller after an SBC reset.
irefOscTrim[8:1]	$C2_{HEX}$	[7:0]	40_{HEX}	RW	

3.3.3.2 Register "irefLpOsc" – Trim Value for the Low-Power Oscillator

Table 3.3 Register `irefLpOsc`

Name	Address	Bits	Default	Access	Description
lpOscTrimVal	$7A_{HEX}$	[6:0]	1010010_{BIN}	RW	Trim value for the low-power oscillator. The frequency of the low-power oscillator increases (decreases) when this value is incremented (decremented). **Note:** This value is automatically updated by the OTP controller after SBC reset.
Unused		[7]	0_{BIN}	RO	Unused; always write as 0.

3.3.3.3 Register "lpOscTrim" – Configuration Register for the Low-Power Oscillator Trimming Circuit

Table 3.4 Register lpOscTrim

Name	Address	Bits	Default	Access	Description
lpOscTrimEna	$7B_{HEX}$	[0]	0_{BIN}	RW	If set to 1, enables the low-power oscillator trimming circuit. **Note:** When the user disables the trimming feature, the trimming logic continues its operation until it has finished the current calculation and then stops. The user can check that the trimming circuit has stopped by evaluating SSW[6], which is 0 when the trimming circuit is inactive.
lpOscTrimUpd		[1]	0_{BIN}	RW	Update bit for the low-power oscillator trimming circuit. When set to 1, the trimming circuit is allowed to update `lpOscTrimVal` in register `irefLpOsc`. When set to 0, no hardware update is performed. **Note:** Do not change while trimming circuit is active.
lpOscTrimCfg		[3:2]	01_{BIN}	RW	This value selects the number of clock periods of the low-power oscillator to be used to determine the frequency. 0 – 4 clock periods 1 – 8 clock periods 2 – 16 clock periods 3 – 32 clock periods **Note:** Do not change while trimming circuit is active.
Unused		[7:3]	00000_{BIN}	RO	Unused; always write as 0.

3.3.3.4 Register "lpOscTrimCnt" – Result Counter of the Low-Power Oscillator Trimming Circuit

Table 3.5 Register `lpOscTrimCnt`

Name	Address	Bits	Default	Access	Description
lpOscTrimCnt[7:0]	78_{HEX}	[7:0]	00_{HEX}	RO	Result counter of the low-power oscillator trimming circuit. This value will only be read when the trimming circuit is inactive (SSW[6] == 0).
lpOscTrimCnt[10:8]	79_{HEX}	[2:0]	000_{BIN}	RO	
Unused		[7:3]	00000_{BIN}	RO	Unused; always write as 0

3.3.4 Resets

The main reset source is the integrated power-on-reset circuit, which resets the complete digital core of the SBC when VDDE drops below 3.0V (typical). There are three other reset sources that reset the complete digital core of the SBC except the watchdog timer and its configuration registers.

These additional reset sources are

- **Watchdog reset:** This reset occurs when the active watchdog timer expires without being handled by the user's software.
- **Software reset:** This reset can be generated by the user by writing the value $A9_{HEX}$ to register `swRst`.
- **PMU error reset:** This reset occurs if the power management unit (PMU) goes into an invalid state (e.g., due to cosmic radiation).

If any of these four resets occurs, the power-on procedure is executed, which powers up the required analog blocks and starts the download procedure for the OTP. This download procedure transfers the OTP contents into the appropriate registers if the OTP content is valid. The MCU_RSTN pin is driven low, which can be used to reset the connected external microcontroller. The microcontroller reset is released after the power-up procedure has finished.

The MCU_RSTN pin is also driven low when the system goes to OFF or ULP State because the power supplies to the microcontroller (VDDP, VDDC) are disabled in these power-down states. In this case, the MCU_RSTN low state is released after a wake-up event has occurred and the power supplies to the external microcontroller have stabilized.

Another possible reset source for the external microcontroller is VddpReset, which is also generated by the power-on-reset circuit when VDDE drops below 4.05V (typical). In this case, it cannot be guaranteed that VDDP, which is needed for correct operation of the external microcontroller, is still valid if VDDP is trimmed to the higher level of 3.3V (see section 3.12.5).

The digital core of the SBC observes the input from the power-on-reset block and generates the MCU_RSTN signal only when all of the following conditions are true:

- VDDP is trimmed to 3.3V (bit `vddpTrim` of register `pwrTrim` is set to 1).
- The ZSSC1750/51 system is in the Full-Power State (FP).
- VDDP reset is not disabled (bit `disVddpRst` of register `funcDis` is set to 0; see Table 3.8).

3.3.4.1 The Reset Status

The external microcontroller can easily check the reason for being reset by a single-byte transfer to the SBC (SPI address byte only) and evaluating `SSW[10:8]`, which contains the reason for the last reset (reset status). This value can be evaluated by the user's software for different actions after reset:

Reset status 0: In this case, the reset was generated by the power-on-reset cell. The SBC was reset, and a MCU_RSTN signal was generated to reset the external microcontroller.

Reset status 1: The watchdog timer was not handled and has expired (see section 3.4). The SBC logic (except the watchdog timer and its configuration registers) was reset and a MCU_RSTN signal was generated to reset the external microcontroller

Reset status 2: Only a MCU_RSTN signal was generated to reset the external microcontroller due to a wakeup from the ULP or OFF State.

Reset status 3: The user's software has forced a reset. The SBC logic (except the watchdog timer and its configuration registers) was reset and a MCU_RSTN signal was generated to reset the external microcontroller.

Reset status 4: VDDP has dropped below 3.3V, and the external microcontroller was active. Only a MCU_RSTN signal was generated to reset the external microcontroller.

Reset status 5: The PMU is in an illegal state. The SBC logic was reset (except the watchdog timer and its configuration registers) and a MCU_RSTN signal was generated to reset the external microcontroller.

3.3.4.2 The Low-Voltage Flag

The low-voltage flag is part of the analog block. The low-voltage flag is at low-level state after power-on-reset. It can be set by the user's software by writing the value '1' to bit `lvfSet` in register `cmdExe`. It is cleared by the power-on-reset cell when VDDE drops below 1.9V (typical). When VDDE drops below this threshold, it cannot be guaranteed that the VDDL voltage is high enough to provide a reliable SBC digital supply. The low-voltage flag is mapped to SPI `SSW[11]` where the user's software can read its value.

3.3.4.3 Register "swRst" – Software Reset

Table 3.6 Register `swRst`

Name	Address	Bits	Default	Access	Description
swRst	80_{HEX}	[7:0]	00_{HEX}	WO	Writing $A9_{HEX}$ to this register forces a software reset, which generates a MCU_RSTN signal to reset the external microcontroller as well as the SBC digital core except the watchdog timer and its configuration registers. Always reads as 0.

3.3.4.4 Register "cmdExe" – Triggering Command Execution by Software

Table 3.7 Register `cmdExe`

Name	Address	Bits	Default	Access	Description
wdogClr	68_{HEX}	[0]	0_{BIN}	RW	Writing 1 to this bit clears the watchdog timer. This bit is cleared by hardware after the watchdog is cleared. As long as the clear procedure is active, any further writes to this bit are rejected.
otpDownload		[1]	1_{BIN}	WO	Strobe register; write 1 to start the download procedure from the OTP; always reads as 0.
lvfSet		[2]	0_{BIN}	WO	Strobe register; write 1 to set the low-voltage flag; always reads as 0.
Unused		[7:3]	00000_{BIN}	RO	Unused; always write as 0.

3.3.4.5 Register "funcDis" – Disabling VDDP Reset and STO Output Pin

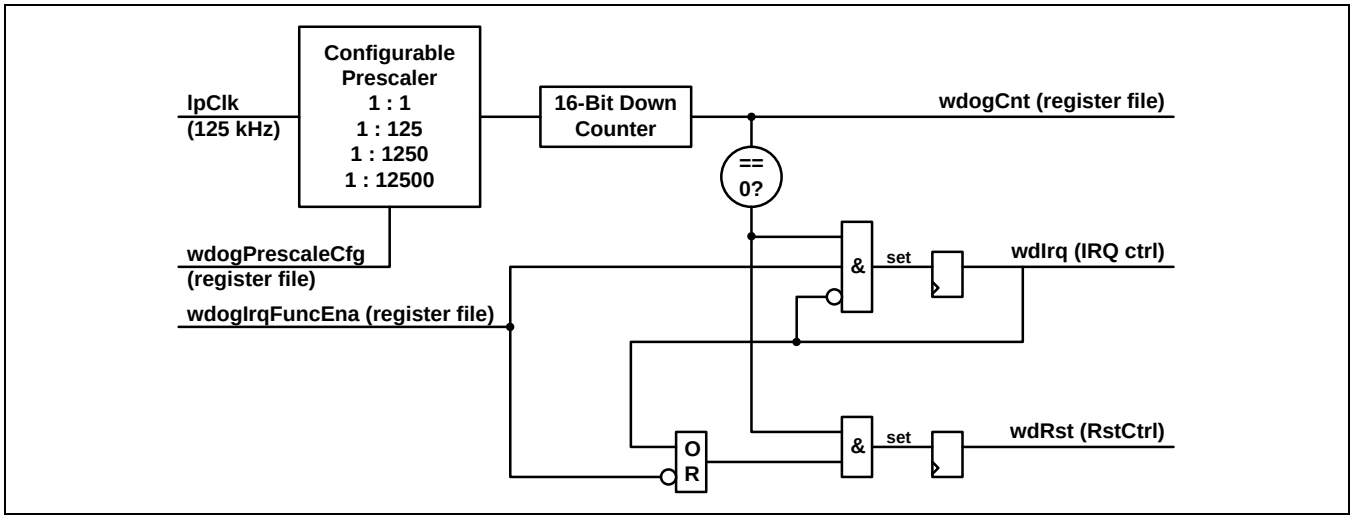
Table 3.8 Register `funcDis`

Name	Address	Bits	Default	Access	Description
disVddpRst	$B9_{HEX}$	[0]	0_{BIN}	RW	When set to 1, VddpReset does not generate a MCU_RSTN signal to reset the external microcontroller.
disStoOut		[1]	0_{BIN}	RW	When set to 1, the output driver of the STO pin is disabled.
Unused		[7:2]	000000_{BIN}	RO	Unused; always write as 0.

3.4 SBC Watchdog Timer (WD_TIMER Block)

The SBC contains a configurable watchdog timer (down counter) for the ZSSC1750/51 when it is running using the clock from the low-power oscillator. It is used to recover from an invalid software or hardware state. To avoid a reset of the system, the watchdog must be periodically serviced. The only part of the system that will not be reset by the watchdog reset is the watchdog itself and its configuration registers.

Figure 3.2 Structure of the Watchdog Timer



By default, the watchdog timer is active starting with a counter value of $FFFF_{HEX}$ and a prescaler of 125. This is done to guarantee that the boot code of the external microcontroller has enough time to finish. During the initialization phase of the system, the user's software can disable, reconfigure, and restart the watchdog. Disabling the watchdog before configuration is required as all write accesses to the register `wdogPresetVal` and the register `wdogCfg` except the bits `wdogLock` and `wdogEna` (see Table 3.12) are blocked when the watchdog is active. As it takes multiple low-power clock cycles until the enable signal is evaluated inside the watchdog clock domain, the `SSW[7]` bit (`wdActive`) must be checked to determine if write accesses are possible. To avoid any malfunction during reconfiguration, the prescaler registers are set to 0 and the counter register is set to $FFFF_{HEX}$ at disable.

When the watchdog is disabled, configuration is possible. The register wdogPresetVal contains the value that will be copied into the down counter in the first enable cycle or when the watchdog timer is serviced via the wdogClr bit in register cmdExe. The field wdogPrescaleCfg in register wdogCfg configures the prescaler. The resolution and maximum timeout for the watchdog depend on the configuration as shown in Table 3.9.

Table 3.9 Resolution and Maximum Timeout for Prescaler Configurations

wdogPrescaleCfg Setting	Prescaler Configuration	Resolution	Maximum Timeout
0	1:1	8µs	524 ms
1	1:125	1ms	65.5 s
2	1:1250	10ms	655.3 s
3	1:12500	100ms	6553.5 s

As the maximum timeout value might still be too small for some applications, the user can use the wdogPmDis bit in register wdogCfg to select whether the watchdog timer will be halted during any power-down state (bit set to 1) or not (bit set to 0).

It is also possible to use the watchdog timer (WDT) as a wake-up source. When the wdogIrqFuncEna bit in register wdogCfg is set to 1 and the down counter reaches 0, an interrupt is generated (instead of a reset that would wake up the system) and the down counter reloads the preset value and continues its operation. When the watchdog timer expires for a second time without service, the watchdog reset is generated. If the wdogIrqFuncEna bit is set to 0, the reset is already generated when the timer expires for the first time.

After reconfiguration, the watchdog timer is re-enabled. To avoid further (accidental) changes to the watchdog timer configuration registers, the user can set the wdogLock bit inside the register wdogCfg to 1. If this bit is set, all write accesses are blocked. The wdogLock bit will only be cleared by a power-on reset.

The WDT can also be disabled by driving the WDT_DIS pin HIGH. In this case it is halted, but still can be cleared via the wdogClr bit in register cmdExe (see Table 3.7). This functionality is useful in the external microcontroller's in-circuit programming mode to disable a reset generated by the watchdog timer.

To perform the required period servicing of the watchdog timer, the user must write the value 1 to the wdogClr bit in register cmdExe. To avoid any malfunction if the watchdog is serviced too often, any consecutive write accesses to the wdogClr bit are blocked until the first clear process has finished.

Important: The preset value programmed to the wdogPresetVal register must never be 0_{HEX} as this would immediately cause a reset forcing the system into a dead lock. It is strongly recommended that the user's software checks the programmed reload value before re-enabling the watchdog.

Important: The preset value must not be too small. The user must take into account critical system timings including power-up times and flash programming/erasing times.

Note: The reconfiguration of the registers wdogPresetVal and wdogCfg, including bits wdogEna and wdogLock, can be done in a single SPI burst write access.

3.4.1 Watchdog Registers

3.4.1.1 Register "wdogPresetVal" – Preset Value for the Watchdog Timer

Table 3.10 Register wdogPresetVal

Important: The preset value programmed to this register must never be 0_{HEX} (see section 3.4 above).

Name	Address	Bits	Default	Access	Description
wdogPresetVal[7:0]	72_{HEX}	[7:0]	FF_{HEX}	RW	Lower byte of the preset value of the watchdog timer. This value is loaded into the lower byte of the watchdog counter when the watchdog is enabled or when the watchdog is cleared. **Note:** This bit can only be written when the watchdog is not locked (`wdogLock` == 0) and when the watchdog is inactive (`SSW[7]` == 0).
wdogPresetVal[15:8]	73_{HEX}	[7:0]	FF_{HEX}	RW	Upper byte of the preset value of the watchdog timer. This value is loaded into the upper byte of the watchdog counter when the watchdog is enabled or when the watchdog is cleared. **Note:** This bit can only be written when the watchdog is not locked (`wdogLock` == 0) and when the watchdog is inactive (`SSW[7]` == 0).

3.4.1.2 Register "wdogCnt" – Current Value of Watchdog Timer

Table 3.11 Register wdogCnt

Name	Address	Bits	Default	Access	Description
wdogCnt[7:0]	70_{HEX}	[7:0]	00_{HEX}	RO	Lower byte of current watchdog timer value
wdogCnt[15:8]	71_{HEX}	[7:0]	00_{HEX}	RO	Upper byte of current watchdog timer value

3.4.1.3 Register “wdogCfg” – Watchdog Timer Configuration Register

Table 3.12 Register wdogCfg

Name	Address	Bits	Default	Access	Description
wdogEna	74_{HEX}	[0]	1_{BIN}	RW	Global enable bit for the watchdog timer. **Note:** This bit can only be written when the watchdog is not locked (`wdogLock` == 0).
wdogPmDis		[1]	0_{BIN}	RW	When this bit is set to 1, PMU stops the watchdog during any power-down state. **Note:** This bit can only be written when the watchdog is not locked (`wdogLock` == 0).
wdogIrqFuncEna		[2]	0_{BIN}	RW	When this bit is set to 1, the watchdog reloads the preset value when expiring for the first time and generates an interrupt instead of a reset. A reset will always be generated when the watchdog timer expires for the second time. **Note:** This bit can only be written when the watchdog is not locked (`wdogLock` == 0) and when the watchdog is inactive (`SSW[7]` == 0)
wdogPrescaleCfg		[4:3]	01_{BIN}	RW	Prescaler configuration: 0 – No prescaler active 1 – Prescaler of 125 is active 2 – Prescaler of 1250 is active 3 – Prescaler of 12500 is active **Note:** This bit can only be written when the watchdog is not locked (`wdogLock` == 0) and when the watchdog is inactive (`SSW[7]` == 0)
Unused		[6:5]	00_{BIN}	RO	Unused; always write as 0.
wdogLock		7	0_{BIN}	RWS	When this bit is set to 1, all write accesses to the other bits of this register as well as to the `wdogPresetVal` registers are ignored. This bit can only be written to 1 and is only cleared by a power-on reset.

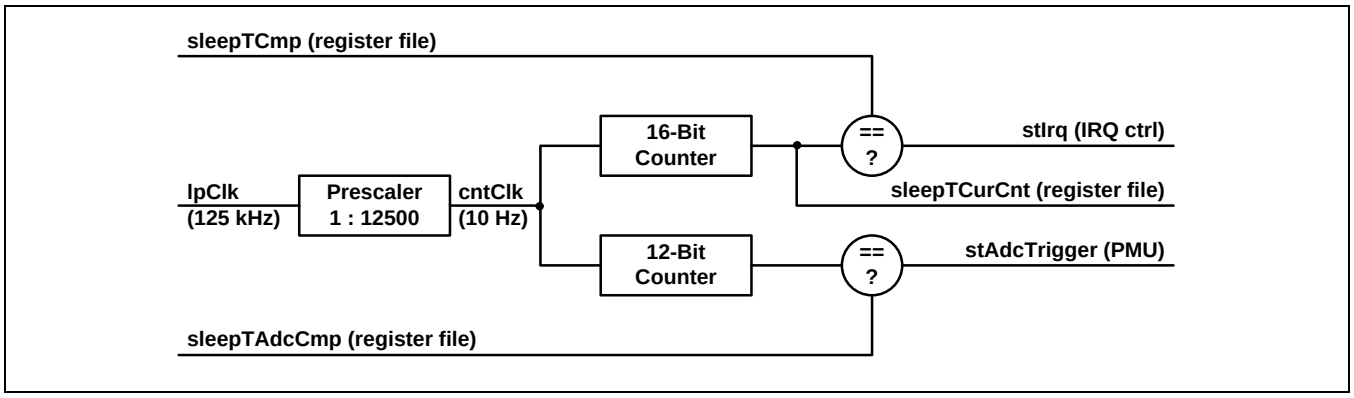
3.5 SBC Sleep Timer (GP_TIMER Block)

The integrated sleep timer (up counter) in the GP_TIMER (general-purpose timer) block is only active when the system is in any low-power state and it is running with the 125kHz clock from the low-power oscillator.

The sleep timer consists of three blocks:

- A fixed prescaler that divides the incoming 125kHz clock from the low-power oscillator by 12500 to get a timer resolution of 10 Hz.
- A 16-bit counter that generates an interrupt (signal: stIrq) when the timer reaches the programmed compare value in the `sleepTCmp` register (see Table 3.14).
- A 12-bit counter that triggers the PMU (with signal stAdcTrigger) when the timer reaches the programmed compare value in the `sleepTAdcCmp` register (see Table 3.13) to power-up the ADC blocks and to perform measurements if one of the discrete measurement scenarios are configured.

Figure 3.3 Structure of the Sleep Timer



When the system goes from the Full-Power (FP) State to any power-down state on request by the user, the prescaler and both counters are cleared and the 16-bit counter is enabled. Every 100ms, triggered by the prescaler, the 16-bit counter is incremented until it reaches the programmed compare value `sleepTCmp`. When the compare value is reached, the timer stops and the interrupt controller is triggered to set the corresponding status flag (see section 3.6.1.1). The sleep timer is also stopped when the system returns to the FP State. The user can determine the sleep duration by reading the register `sleepTCurCnt`, which returns the value of the 16-bit counter (see Table 3.15).

Note: Although the timer stops and the interrupt status bit is set when the compare value is reached, the system remains in the power-down state if the corresponding interrupt is not enabled to drive the interrupt line IRQN (bit 1 in the `irqEna` register; see Table 3.17).

Equation (2) can be used to determine the correct sleep time to be programmed. The sleep timer expires after 100ms for a compare value of 0, after 200ms for a compare value of 1, and so on.

$$\text{Sleep Time} = 100\text{ms} * (\text{sleepTCmp} + 1) \quad (2)$$

The 12-bit counter that triggers the PMU is only enabled during any power-down state when any discrete measurement scenario is configured. In this case, the counter is incremented each 100ms triggered by the prescaler. When the counter reaches the programmed compare value `sleepTAdcCmp`, a strobe for the PMU is generated and the 12-bit counter is reset to 0. Then it continues its operation. This counter is only stopped when the system returns to the FP State, but it continues to operate when the sleep timer has expired if it was not enabled to wake up the system.

Equation (3) can be used to determine the correct ADC trigger time to be programmed. The ADC trigger timer expires after 100ms for a compare value of 0, after 200ms for a compare value of 1, and so on.

In general

$$\text{ADC Trigger Time} = 100\text{ms} * (\text{sleepTAdcCmp} + 1) \quad (3)$$

Important: When both the sleep timer for wake-up and the ADC trigger timer for discrete measurements are used, special care must be taken when programming the compare values because when the sleep timer expires, the wake-up condition has higher priority over an active ADC measurement or an ADC trigger strobe.

3.5.1 Sleep Timer Registers

3.5.1.1 Register "sleepTAdcCmp" – Compare Value for ADC Trigger Timer

Table 3.13 Register `sleepTAdcCmp`

Name	Addr	Bits	Default	Access	Description
sleepTAdcCmp[7:0]	60_{HEX}	[7:0]	00_{HEX}	RW	Lower byte of compare value for the ADC trigger timer; the ADC trigger timer is only active if the system is in LP or ULP State and any discrete measurement scenario is configured generating periodic strobes for the PMU. ADC trigger time = 100 ms ∗ (`sleepTAdcCmp` + 1)
sleepTAdcCmp[15:8]	61_{HEX}	[7:0]	00_{HEX}	RW	Upper byte of compare value for ADC trigger timer; ADC trigger timer is only active when the system is in LP or ULP State and any discrete measurement scenario is configured generating periodic strobes for the PMU. ADC trigger time = 100 ms ∗ (`sleepTAdcCmp` + 1)

3.5.1.2 Register "sleepTCmp" – Compare Value for Sleep Timer

Table 3.14 Register `sleepTCmp`

Name	Addr	Bits	Default	Access	Description
sleepTCmp[7:0]	62_{HEX}	[7:0]	00_{HEX}	RW	Lower byte of compare value for sleep timer; sleep timer is only active if the system is in LP or ULP State. Sleep time = 100 ms ∗ (`sleepTCmp` + 1)
sleepTCmp[15:8]	63_{HEX}	[7:0]	00_{HEX}	RW	Upper byte of compare value for sleep timer; sleep timer is only active when the system is in LP or ULP State. Sleep time = 100 ms ∗ (`sleepTCmp` + 1)

3.5.1.3 Register "sleepTCurCnt" – Current Value of Sleep Timer

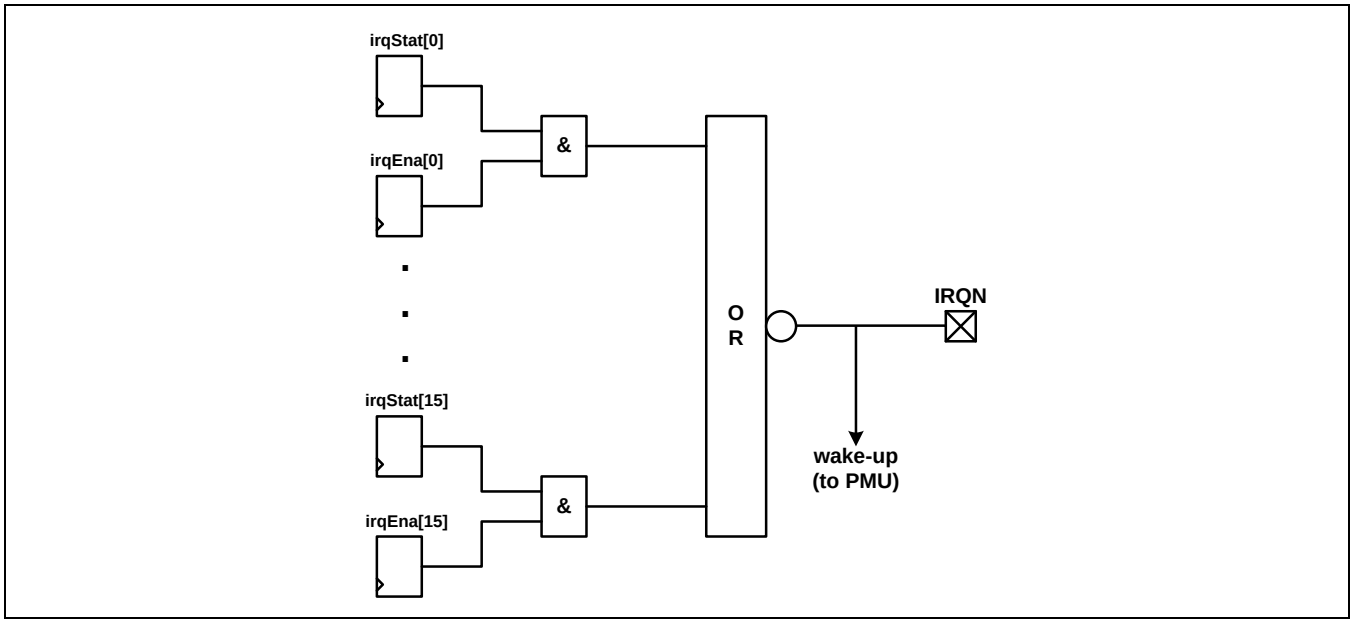
Table 3.15 Register `sleepTCurCnt`

Name	Addr	Bits	Default	Access	Description
sleepTCurCnt[7:0]	20_{HEX}	[7:0]	00_{HEX}	RO	Lower byte of the current sleep timer value. Since the timer is stopped in FP State, the duration of the last power-down state can be determined: Sleep time = 100ms ∗ (`sleepTCurCnt` + 1) **Note:** Value is only valid when `SSW[1]` (sleep timer valid stValid) is set.
sleepTCurCnt[15:8]	21_{HEX}	[7:0]	00_{HEX}	RO	Upper byte of the current sleep timer value. Since the timer is stopped in FP State, the duration of the last power-down state can be determined: Sleep time = 100ms ∗ (`sleepTCurCnt` + 1) **Note:** Value is only valid when `SSW[1]` (stValid) is set.

3.6 SBC Interrupt Controller (IRQ_CTRL Block)

There are 16 different interrupt sources in the SBC system, each having a dedicated interrupt status bit in the `irqStat` register (see Table 3.16) and a dedicated interrupt enable bit in the `irqEna` register (see Table 3.17). The interrupt controller captures each interrupt source in the interrupt status register independently of the interrupt enable settings. The interrupt controller combines all enabled interrupt status bits into the low-active interrupt signal that is used to drive the interrupt pin IRQN of the SBC and to wake up the system by the PMU. This means that interrupt status bits, which can always be set even when disabled, can only generate a wake-up event and drive the interrupt pin IRQN when they are enabled.

Figure 3.4 Generation of Interrupt and Wake-up



The user can determine the interrupt reason by reading the interrupt status register `irqStat`. The interrupt status register is cleared on each read access. Therefore the user's software must ensure that it stores the read interrupt status value if needed to avoid loss of information.

3.6.1.1 Interrupt Sources

The bit mapping is the same for the interrupt enable register `irqEna` (see Table 3.17) and the interrupt status register `irqStat` (see Table 3.16):

Bit 0: **Watchdog Timer Interrupt**; status is set by the watchdog timer when the interrupt functionality of the watchdog timer is enabled and the watchdog timer expires for the first time.

Bit 1: **Sleep Timer Interrupt**; status is set by the sleep timer when the sleep timer reaches the programmed compare value.

Bit 2: **LIN TXD Timeout Interrupt (for ZSSC1750 only)**; status is set by the LIN support logic when the TXD input from the external microcontroller is low for more than 10.24ms.

Bit 3: **LIN Short Interrupt (for ZSSC1750 only)**; status is set by the LIN support logic when a short is detected in the LIN PHY.

Bit 4: **LIN Wakeup Interrupt (for ZSSC1750 only)**; status is set by the LIN support logic when a wake-up frame is detected on the LIN bus.

Bit 5: **Current Conversion Result Ready Interrupt**; status is set by the ADC unit when a single current measurement (register `adcCrcl` == 0) or multiple current measurements defined by `adcCrcl` (register `adcCrcl` ≠ 0) have been completed and the result is available.

Bit 6: **Voltage Conversion Result Ready Interrupt**; status is set by the ADC unit when a single voltage measurement (register `adcVrcl` == 0) or multiple voltage measurements defined by the `adcVrcl` (register `adcVrcl` ≠ 0) have been completed and the result is available.

Bit 7: **Temperature Conversion Result Ready Interrupt**; status is set by the ADC unit when a single temperature measurement has been completed and the result is available.

Bit 8: **Current Comparator Interrupt**; status is set by the ADC unit when the Current Threshold Counter Mode is enabled (register `adcAcmp[2:1]` ≠ 00) and the absolute value of multiple current measurements (defined by register `adcCtcl`) exceeds the programmed current threshold (register `adcCrth`).

Note: If the threshold counter mode is enabled but `adcCtcl` is 0, this bit is always set independently of the threshold.

Bit 9: **Voltage Comparator Interrupt**; status is set by the ADC unit if the `VThWuEna` bit (`adcAcmp[8]`) is set to 1 and a single measured voltage or the accumulated voltage measurements (depends on configured mode) drop below the programmed (register `adcVTh`) voltage threshold.

Bit 10: **Temperature Threshold Interrupt**; status is set by the ADC unit when the `TWuEna` bit (`adcAcmp[10]`) is set to 1 and a temperature measurement is outside the specified temperature interval defined by registers `adcTmin` and `adcTmax`.

Bit 11: **Current Accumulator Threshold Interrupt**; status is set by the ADC unit when the `CAccuThEna` bit (`adcAcmp[3]`) is set to 1 and the accumulated current values rise above the programmed threshold value (register `adcCaccTh`) for a positive threshold value or fall below the programmed threshold value for the negative threshold value.

Bit 12: **Current Overflow Interrupt**; status is set by the ADC unit when the `COvrEna` bit (`adcAcmp[4]`) is set to 1 and the compensated value of a current measurement is outside of the representable range.

Bit 13: **Voltage/Temperature Overflow Interrupt**; status is set by the ADC unit when the `VTOvrEna` bit (`adcAcmp[5]`) is set to 1 and the compensated value of a voltage or temperature measurement is outside of the representable range.

Bit 14: **Current Over-Range Interrupt**; status is set by the ADC unit when the `COvrEna` bit (`adcAcmp[4]`) is set to 1 and the input from the current ADC is overdriven.

Bit 15: **Voltage/Temperature Over-Range Interrupt**; status is set by the ADC unit when the `VTOvrEna` bit (`adcAcmp[5]`) is set to 1 and the input from the voltage/temperature ADC is overdriven.

3.6.1.2 Register “irqStat” – Interrupt Status Register

Table 3.16 Register `irqStat`

Name	Address	Bits	Default	Access	Description
irqStat[7:0]	00_{HEX}	[7:0]	00_{HEX}	RC	Lower byte of the interrupt status register as defined in section 3.6.1.1; each bit is set by hardware and cleared on read access.
irqStat[15:8]	01_{HEX}	[7:0]	00_{HEX}	RC	Upper byte of interrupt status register as defined in section 3.6.1.1; each bit is set by hardware and cleared on read access.

Note: To avoid loss of information, the hardware set condition has a higher priority than the read clear condition.

3.6.1.3 Register “irqEna” – Interrupt Enable Register

Table 3.17 Register `irqEna`

Name	Address	Bits	Default	Access	Description
irqEna[7:0]	54_{HEX}	[7:0]	00_{HEX}	RW	Lower byte of the interrupt enable register as defined in section 3.6.1.1; only enabled interrupts can drive the interrupt line and wake up the system; the bit mapping is the same as for the interrupt status register.
irqEna[15:8]	55_{HEX}	[7:0]	00_{HEX}	RW	Upper byte of the interrupt enable register as defined in section 3.6.1.1; only enabled interrupts can drive the interrupt line and wake up the system; the bit mapping is the same as for the interrupt status register.

Note: The interrupt enable bit for the LIN wake-up interrupt (`irqEna[4]`) is also used as the enable for the LIN wake-up (for ZSSC1750 only) frame detector within the PMU.

3.7 SBC Power Management Unit (SBC_PMU Block)

The power management unit (PMU) controls placing the SBC into the selected power down state, controlling the power down signals for the different analog blocks, and controlling the clocks for the digital logic. It also controls the other digital modules during the power-down state.

The system provides four different power states:

FP (Full-Power State)	In this state, all blocks are powered except the ADCs if the user's software has not enabled them. All internal clocks are active (divClk and muxClk are 4MHz) and the external microcontroller is also powered and clocked through pins VDDP, VDDC, and MCU_CLK. When powered and enabled by software, the ADC clocks are generated from the clock from the high-precision oscillator.
LP (Low-Power State)	In this state, the high-precision oscillator and the LIN transmitter (ZSSC1750 only) are powered down. The clock for the external microcontroller (MCU_CLK) is stopped, but the microcontroller remains powered through VDDP and/or VDDC. Depending on the selected measurement scenario, the ADCs are also powered down during times of inactivity. Otherwise the ADC clocks are generated from the low-power oscillator.
ULP (Ultra-Low-Power State)	In this state, the high-precision oscillator and the LIN transmitter (ZSSC1750 only) are powered down. The optional external microcontroller clock MCU_CLK is stopped and the supply voltages for the external microcontroller (VDDP, VDDC) are powered down. Depending on the selected measurement scenario, the ADCs are also powered down during times of inactivity. Otherwise, the ADC clocks are generated from the clock from the low-power oscillator.
OFF (Off State)	In this state, all analog blocks except the digital power supply for the SBC and the RX part of the LIN PHY (ZSSC1750 only) are powered down. The external microcontroller clock MCU_CLK is stopped, and the supply voltages for the external microcontroller (VDDP, VDDC) are powered down.

For the ZSSC1750/51 to enter any of the power-down states (LP, ULP, or OFF), the user's software must first set the `pdState` field of register `pwrCfgLp` to select the state (see Table 3.19) and enable the interrupts needed as the wakeup source before writing $A9_{HEX}$ to register `gotoPd` (see Table 3.20). Immediately after $A9_{HEX}$ is written to the `gotoPd` register, the CSN line must be driven high. Although for all other register accesses, the CSN line can be kept low and the next SPI transfer can follow immediately, it is mandatory to drive CSN high for the power-down command. Otherwise, the PMU remains in the FP State.

Important: If no interrupt is enabled, the system can only be awakened by power-on-reset!

Note: The CSN line must be driven high to go to power-down after writing the value $A9_{HEX}$ to register `gotoPd`.

The following tasks are always performed on transition to any power-down state by the PMU:

- Both ADCs are stopped. Any active measurement is interrupted. ADC control is transferred to the PMU.
- Those configuration values that can be configured independently for the Full-Power State and power-down states are switched to the power-down settings.
- The sleep timer is cleared and enabled.
- The clock on the MCU_CLK pin is stopped.
- The high-precision oscillator is powered down.
- The TX part of the LIN PHY is powered down (ZSSC1750 only).
- The source for the muxClk changes from divClk to lpClk.

If any of the enabled interrupts occurs and the interrupt pin IRQN is driven low, the system wakes up immediately; any ADC measurement that is active during the power-down state is stopped. All mandatory blocks are powered up, and the system waits for stabilization before re-enabling the clock output MCU_CLK for the external microcontroller.

If any of the enabled interrupts is already active on reception of the power-down command or becomes active on transition to the requested power-down state, the system rejects the power-down command or re-enables those blocks that are already powered down. Depending on the time when the power-down procedure was interrupted, it is possible that the sleep timer was not cleared. In this case, the sleep timer valid flag is cleared, signaling that the sleep timer value in register `sleepTCurCnt` is not valid. This flag is mapped to `SSW[1]`.

3.7.1 FP State

After the initial power-on reset when the OTP contents are downloaded into the registers and all blocks have stabilized, the system enters the FP State. In this state, all voltage regulators, both oscillators and the LIN PHY (ZSSC1750 only) are powered but the ADCs are still powered down.

Important: Both ADCs are powered down after power-on reset.

To be able to use the ADCs, the user must first power up the required ADCs by programming register `pwrCfgFp`, bits `pwrAdcI` and/or `pwrAdcV` (see Table 3.18). The first bit enables the current ADC and the second bit enables the voltage/temperature ADC. In this register are three other bits that can be set by the user, but they should be handled with care as the system consumes less power when any of these bits is set but the accuracy of the measurement results is reduced:

- `lpEnaFp` if set to 1, the bias current for analog blocks is reduced to 10%
- `ulpEnaFp` if set to 1, the bias current for analog blocks is reduced to 5%
- `pdRefbufOcFp` if set to 1, the offset cancellation circuit inside the reference buffer is powered down

Note: If both `lpEnaFp` and `ulpEnaFP` are set to 1, the bias current for analog blocks is reduced to 15%.

Important: These settings are only used in FP State. For configuration for the power-down states, the `pwrCfgLp` register must be used.

The settings in register `pwrCfgFp` are preserved when entering any power-down state by executing the power-down command. The PMU overrides these settings or switches to the settings made in register `pwrCfgLp` on transition to the power-down state. When the system wakes up and returns to the FP State, the PMU restores the settings as configured in `pwrCfgFp` regardless of whether any ADC was powered in power-down state or not.

3.7.2 LP and ULP States

The LP and ULP power-down states are used to save power while doing measurements with lower accuracy. In both states, the TX part of the LIN PHY and the high-precision oscillator are powered down and the external microcontroller clock is stopped. The internal clock muxClk is driven by the low-power oscillator with a frequency of 125kHz while the internal clock divClk is stopped. In ULP State, the two voltage regulators VDDP (IO voltage for SBC and external microcontroller) and VDDC (optional core voltage for external microcontroller) are powered down. In this case, the SLEEPN pin is driven low to indicate this state. The state of the ADCs and the other analog blocks needed for measurements depends on the configured measurement setup for the power-down state (see following subsections). The blocks are powered when they are needed for measurement and powered down when they are not needed for measurement. This is controlled by the PMU as well as the control signals (*start, stop, mode*) for the digital ADC unit.

The main configuration register for the power-down behavior is register `pwrCfgLp` (see Table 3.19). The field `pdState` is used to select the power-down state to be entered on reception of the power-down command, and the field `pdMeas` is used to define the measurement setup to be used during the power-down state.

There are three other bits to configure the power-down behavior:

- `lpEnaLp` if set to 1, the bias current for analog blocks is reduced to 10%
- `ulpEnaLp` if set to 1, the bias current for analog blocks is reduced to 5%
- `pwrRefbufOcLp` if set to 1, the offset cancellation circuit in the reference buffer is powered up

Note: If both `lpEnaLp` and `ulpEnaLp` are set to 1, the bias current for analog blocks is reduced to 15%.

For the corresponding bits for the FP State, `lpEnaFp` and `ulpEnaFp` in register `pwrCfgFp` (see Table 3.18), the meaning is the same, but the default settings are different. While there is no bias current reduction during FP State (default setting for both bits is 0), the default bias current for the LP and ULP States is reduced to 10%. The meaning of the control bit for the offset cancellation differs: the FP State control bit is a power-down signal; the LP/ULP State control bit is a power-up bit. While the offset cancellation is enabled by default during the FP State (`pdRefbufOcFp` == 0), the offset cancellation is disabled by default during the LP or ULP State (`pdRefbufOcLp` == 0). Both bits are configurable by the user.

On transition to the LP or ULP State, the sleep timer and the ADC trigger timer are cleared. While the sleep timer is always enabled during power-down states, the ADC trigger timer is only enabled when performing discrete measurements. If the sleep timer interrupt is enabled, the system wakes up when the sleep timer expires. If the sleep timer interrupt is not enabled, the sleep timer stops when it expires, but the ADC trigger timer, if enabled due to the measurement configuration, continues its operation. For wake-up, other interrupts must be enabled; e.g., LIN wakeup (for ZSSC1750 only).

Note: The sleep timer is always active during the LP and ULP States.

Note: When reading the sleep timer value after wake-up by another enabled interrupt, the sleep timer is only valid when it has not reached its compare value although the valid flag says valid. Whether the sleep timer is valid can be determined by the sleep timer status bit.

When the system wakes up and returns to FP State, the sleep timer is stopped. The user's software can read the sleep timer value to determine the duration of the power-down state.

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3.7.2.1 Performing No Measurements during LP/ULP State

When the LP or ULP State has been entered, all analog blocks related to ADCs are powered down. If the system goes to power down without performing any measurements, only three different wake-up sources are possible: the watchdog timer interrupt, the sleep timer interrupt, and the LIN wakeup interrupt (for ZSSC1750 only).

Important: At least one of these interrupts must be enabled, as otherwise the system can only wake up via power-on reset. If no interrupt is enabled, the system cannot wake up.

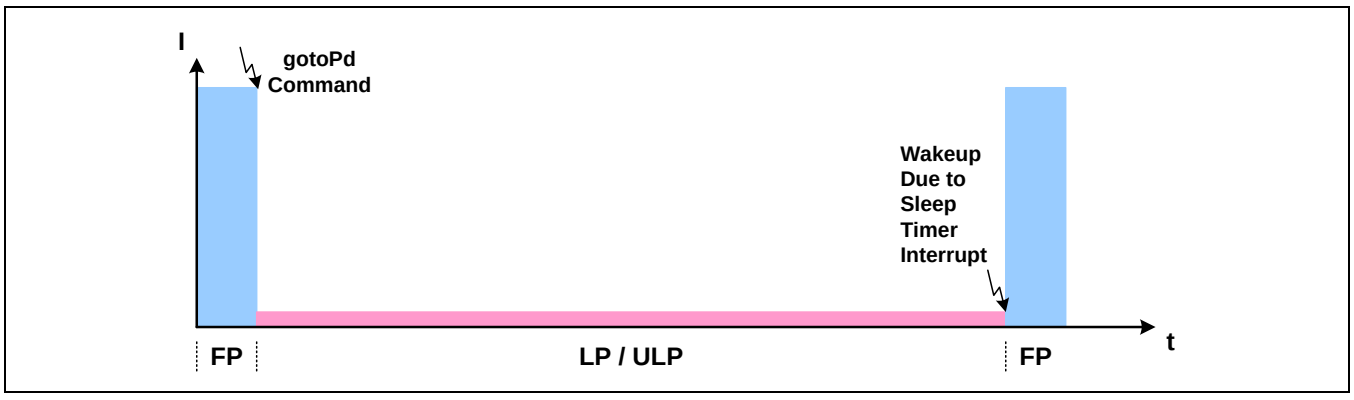
To go to LP or ULP State without performing measurements, the following tasks must be done:

- Enable at least one of the following interrupts:
  - Set `irqEna[0]` to 1 to enable the watchdog interrupt to wake up the system.
  - Set `irqEna[1]` to 1 to enable the sleep timer to wake up the system.
  - Set `irqEna[4]` to 1 to enable the LIN wake-up detector and to enable the system to wake up due to a LIN wakeup frame (for ZSSC1750 only).
- Set up the sleep timer compare value (register `sleepTCmp`) if needed.
- Configure the `pwrCfgLp` register as follows:
  - Set `pdState` to 0 or 1 to configure the LP State or to 2 to configure the ULP State.
  - Set `pdMeas` to 0 to configure the system to perform no measurements.
  - Set `lpEnaLp, ulpEnaLp` and `pwrRefbufOcLp` as needed.
- Write $A9_{HEX}$ to register `gotoPd` and then drive the CSN line high.

When an enabled interrupt occurs, the system wakes up and the settings from register `pwrCfgFp` are restored. When all blocks have stabilized, the external microcontroller clock MCU_CLK is re-enabled, and if coming out of the ULP State, the microcontroller reset MCU_RST is released.

Figure 3.5 LP/ULP State without any Measurements

Note: the sleep timer is used as the wake-up source in this example, but it could also be the watchdog timer interrupt or the LIN wakeup interrupt.



3.7.2.2 Performing Discrete Measurements of Current during LP/ULP State

The system can be configured to periodically enable the current ADC and to measure the current during the LP or ULP State. The current ADC can be configured to perform several current measurements during each measurement phase (green boxes in Figure 3.6).

Upon entering the LP/ULP State and between the measurements, the current ADC is powered down. The voltage/temperature ADC is powered down for the entire power-down period. The PMU powers up the current ADC when triggered by the ADC trigger timer. Possible wake-up sources during this scenario are the watchdog timer interrupt, the sleep timer interrupt, the LIN wakeup interrupt (for ZSSC1750 only), or any of the ADC interrupts related to current.

Important: When no interrupt is enabled, the system cannot wake up.

To go to LP or ULP State and perform discrete current measurements, the following tasks must be done:

- Enable at least one of the following interrupts:
  - Set `irqEna[0]` to 1 to enable the watchdog interrupt to wake up the system.
  - Set `irqEna[1]` to 1 to enable the sleep timer to wake up the system.
  - Set `irqEna[4]` to 1 to enable the LIN wake-up detector and to enable the system to wake up due to a LIN wakeup frame (for ZSSC1750 only).
  - Enable any ADC interrupt related to current (see section 3.6.1.1).
- Set up the sleep timer compare value (register `sleepTCmp`) if needed.
- Set up the ADC trigger timer compare value (register `sleepTAdcCmp`) as needed.
- Configure the `pwrCfgLp` register as follows:
  - Set `pdState` to 0 or 1 to configure LP State or to 2 to configure ULP State.
  - Set `pdMeas` to 1 to configure the system to perform discrete current measurements.
  - Set `lpEnaLp`, `ulpEnaLp` and `pwrRefbufOcLp` as needed.
- Write $A9_{HEX}$ to register `gotoPd` and then drive the CSN line high.

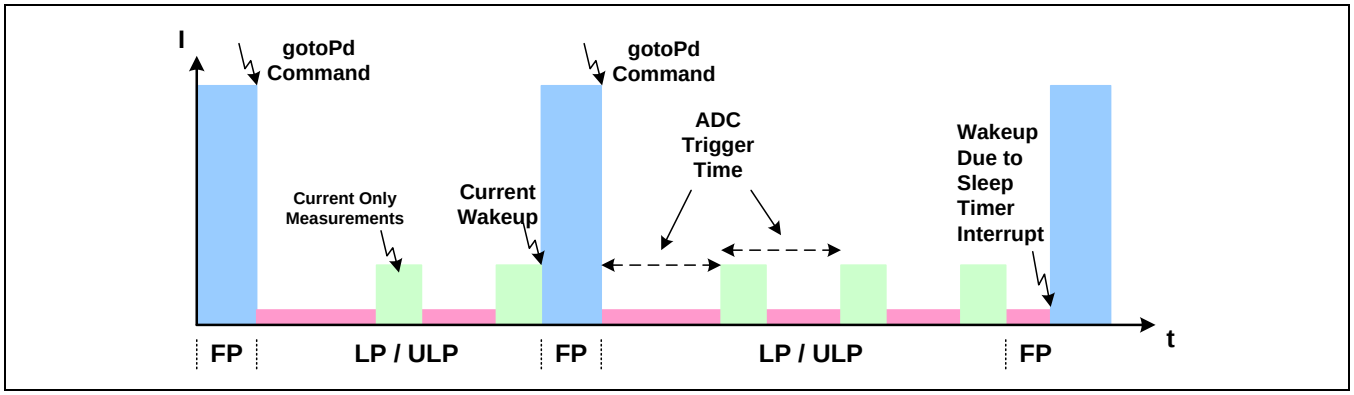
When an enabled interrupt occurs, the system wakes up and the settings from register `pwrCfgFp` are restored. When all blocks have stabilized, the external microcontroller clock is re-enabled and, if coming out of ULP State, the microcontroller reset is released.

Important: If any measurement is active while an enabled interrupt occurs (e.g., the sleep timer expires), the measurement is interrupted and the system returns to FP State.

In the example shown in Figure 3.6, the first wakeup is by the ADC and the second wake-up is by the sleep timer; however, the wakeups could be other combinations of the watchdog timer interrupt, sleep timer interrupt, and/or LIN wakeup interrupt (ZSSC1750 only).

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Figure 3.6 LP/ULP State Performing Only Current Measurements



3.7.2.3 Performing Discrete Measurements of Current, Voltage, and Internal Temperature during LP/ULP State

During the LP or ULP State, the system can be configured to periodically enable both ADCs and measure current, voltage, and internal or external temperature (see section 3.7.2.4 for external temperature). The sequence can be selected in the `pdMeas` bit field [4:2] in register `pwrCfgLp`, which also selects whether internal or external temperature is measured. The period between each measurement is determined by the ADC trigger timer (`sleepTAdcCmp`).

The current ADC can be configured to perform multiple current measurements during each measurement window (green and orange boxes in Figure 3.7 to Figure 3.9) while the voltage/temperature ADC can be configured to perform multiple voltage or internal temperature measurements (orange boxes in Figure 3.7 to Figure 3.9). After performing the configured number of voltage measurements, the PMU changes the configuration for the voltage/temperature ADC and performs a single measurement of the internal temperature. Voltage and temperature are not measured in each sample period if the ADCs are configured for measuring only current in a specified number of initial loops. The user can configure register `discCvtCnt` (see Table 3.21) so that in the first `discCvtCnt` samples, only current is measured before voltage and temperature are measured in the next sample.

Upon entering the LP/ULP State and between the measurements, both ADCs are powered down. The PMU powers up the current ADC when triggered by the ADC trigger timer. The voltage/temperature ADC is only powered up after `discCvtCnt` current-only measurements have been performed. Possible wake-up sources in this setup are all interrupts except LIN short and LIN TXD timeout interrupts (ZSSC1750 only).

Important: When no interrupt is enabled, the system cannot wake up.

To go to the LP or ULP State and perform measurements of discrete current, voltage, and internal temperature, the following tasks must be done:

- Enable at least one of the following interrupts:
  - Set `irqEna[0]` to 1 to enable the watchdog interrupt to wake up the system.
  - Set `irqEna[1]` to 1 to enable the sleep timer to wake up the system.
  - Set `irqEna[4]` to 1 to enable LIN wake-up detector and to enable the system to wake up due to a LIN wakeup frame (for ZSSC1750).
  - Enable any ADC interrupt (see section 3.6.1.1).
- Configure the sleep timer compare value (register `sleepTCmp`) if needed.
- Set up the ADC trigger timer compare value (register `sleepTAdcCmp`) as needed.
- Configure the `pwrCfgLp` register as follows:
  - Set `pdState` to 0 or 1 to configure the LP State or to 2 to configure the ULP State.
  - Set `pdMeas` to 2 to configure the system to perform discrete current, voltage, and internal temperature measurements.
  - Set `lpEnaLp`, `ulpEnaLp` and `pwrRefbufOcLp` as needed.
- Set `discCvtCnt` as needed. This register defines the number of current-only measurement loops before performing measurements of all three parameters.
- Write $A9_{HEX}$ to register `gotoPd` and then drive the CSN line high.

When an enabled interrupt occurs, the system wakes up and the settings from register `pwrCfgFp` are restored. When all blocks have stabilized, the external microcontroller clock is re-enabled and if coming out of the ULP State, the microcontroller reset is released.

Important: If any measurement is active while an enabled interrupt occurs (e.g., the sleep timer expires) the measurement is interrupted and the system returns to the FP State.

Note: If register `discCvtCnt` is set to 0, voltage and temperature are measured in each loop (default setting).

Figure 3.7 LP/ULP State Performing Current, Voltage, and Temperature Measurements with `discCvtCnt` == 2

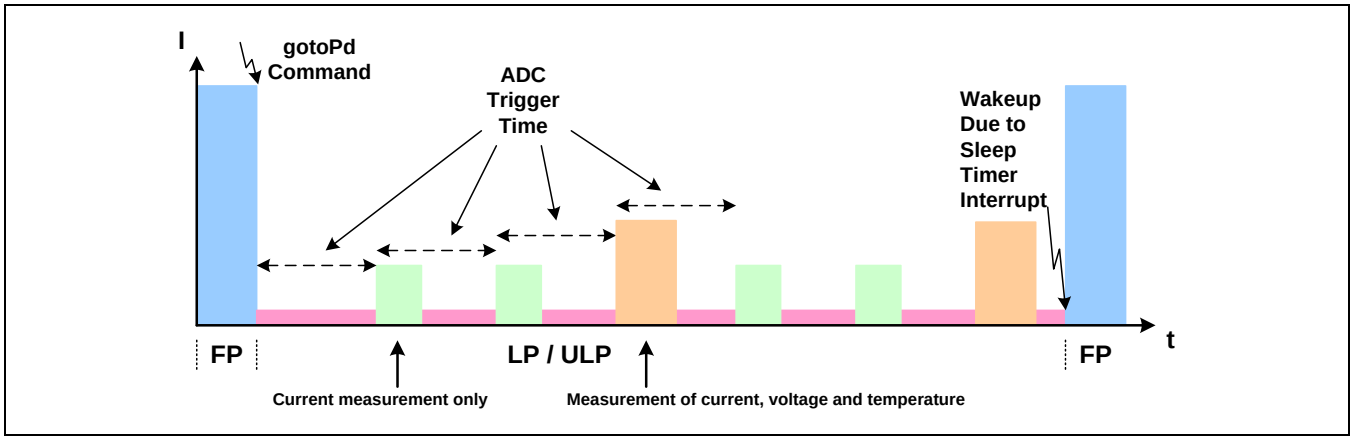


Figure 3.8 LP/ULP State Performing Current, Voltage, and Temperature Measurements with `discCvtCnt` == 5

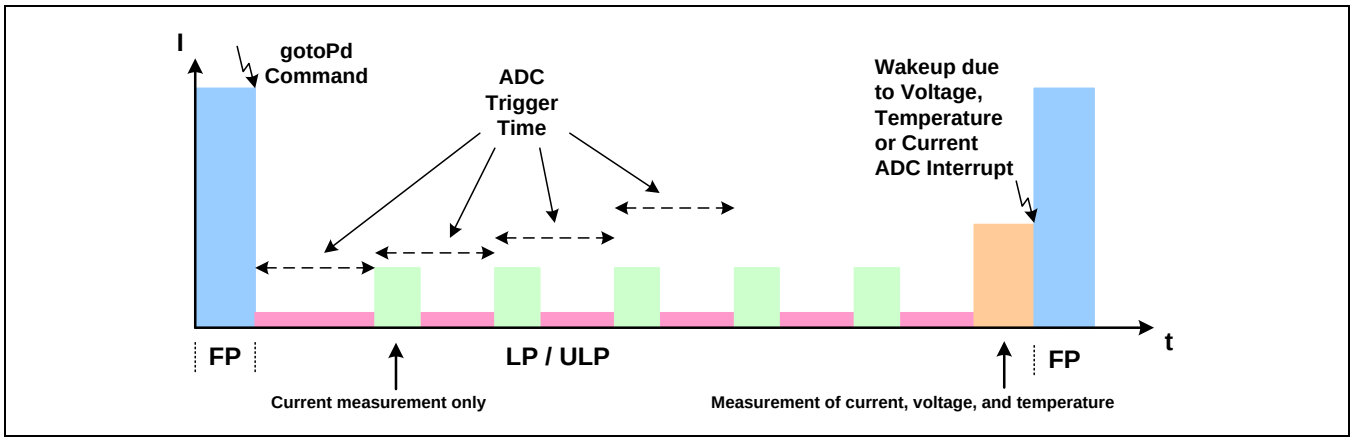
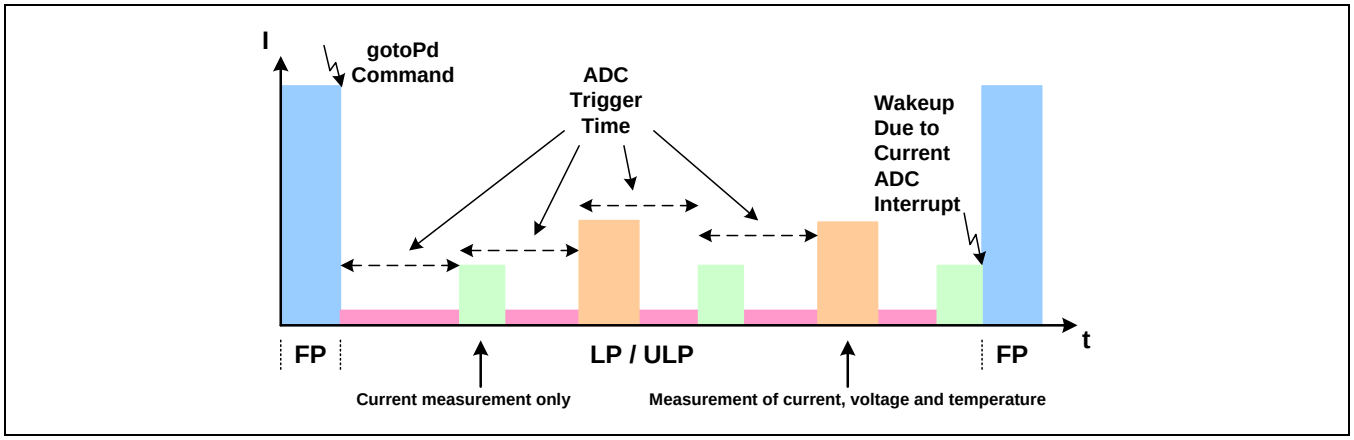


Figure 3.9 LP/ULP State Performing Current, Voltage, and Temperature Measurements with `discCvtCnt` == 1



3.7.2.4 Performing Discrete Measurements of Current, Voltage, and External Temperature during LP/ULP State

During the LP or ULP State, the system can be configured to periodically enable both ADCs and measure current, voltage, and external temperature. This setup is the same as the configuration described in the previous section, except that the external instead of the internal temperature is measured. To use this option, `pdMeas` must be set to 3.

3.7.2.5 Performing Continuous Measurements of Current during LP/ULP State

The system can be configured to perform continuous current measurements during the LP or ULP State. While the current ADC is powered up during the entire power-down state, the voltage/temperature ADC is powered down.

The current ADC is powered up on entering the LP/ULP State if it was not already powered up during the FP State. The ADC trigger timer is not enabled as the measurement is continuous. Possible wake-up sources during this scenario are the watchdog timer interrupt, the sleep timer interrupt, the LIN wakeup interrupt (for ZSSC1750 only), or any of the ADC interrupts related to current.

Important: If no interrupt is enabled, the system cannot wake up.

To go to the LP or ULP State with continuous current measurements, the following tasks must be done:

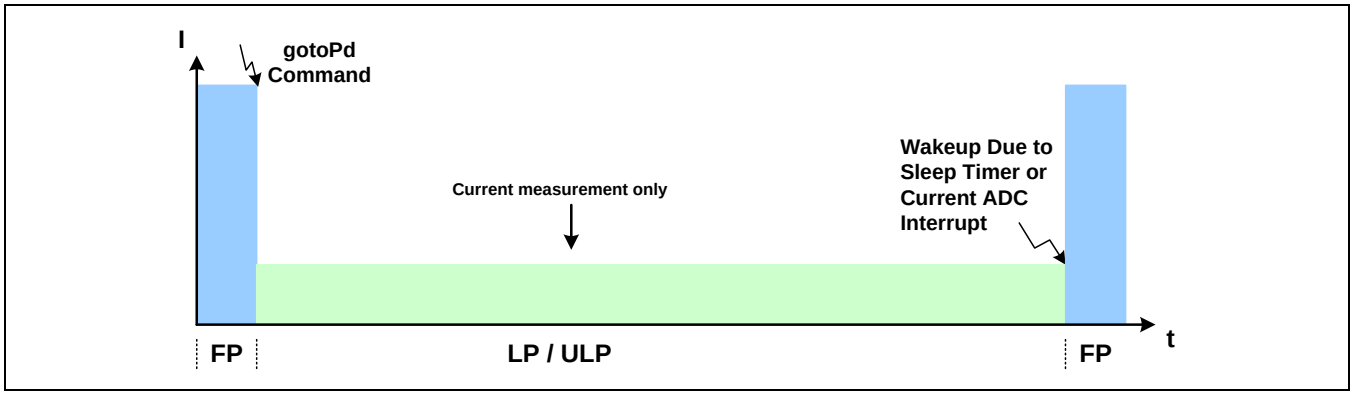
- Enable at least one of the following interrupts:
  - Set `irqEna[0]` to 1 to enable the watchdog interrupt to wake up the system.
  - Set `irqEna[1]` to 1 to enable the sleep timer to wake up the system.
  - Set `irqEna[4]` to 1 to enable the LIN wake-up detector and to enable the system to wake up due to a LIN wakeup frame (for ZSSC1750 only).
  - Enable any ADC interrupt related to current (see section 3.6.1.1).
- Setup the sleep timer compare value (register `sleepTCmp`) if needed.
- Configure the `pwrCfgLp` register as follows:
  - Set `pdState` to 0 or 1 to configure LP State or to 2 to configure ULP State.
  - Set `pdMeas` to 4 to configure the system to perform continuous current measurements.
  - Set `lpEnaLp`, `ulpEnaLp`, and `pwrRefbufOcLp` as needed.
- Write $A9_{HEX}$ to register `gotoPd` and then drive the CSN line high.

When an enabled interrupt occurs, the system wakes up and the settings from register `pwrCfgFp` are restored. When all blocks have stabilized, the external microcontroller clock is re-enabled and if coming out of ULP State, the microcontroller reset is released.

Important: If any measurement is active while an enabled interrupt occurs (e.g., the sleep timer expires), the measurement is interrupted and the system returns to FP State.

Figure 3.10 LP/ULP State Performing Continuous Current-Only Measurements

Note: The sleep timer interrupt or an ADC interrupt related to current is used as the wake-up source in this example, but it could also be the watchdog timer interrupt or the LIN wakeup interrupt (ZSSC1750 only).



3.7.2.6 Performing Continuous Current and Voltage Measurements during LP/ULP State

The system can be configured to perform continuous current and voltage measurements during the LP or ULP State. Both ADCs are powered up during the entire power-down state. The ADCs are powered up on entering the LP/ULP State if they were not already powered up during the FP State. The ADC trigger timer is not enabled as the measurement is continuous. Possible wake-up sources during this scenario are the watchdog timer interrupt, the sleep timer interrupt, the LIN wakeup interrupt (for ZSSC1750 only), or any of the ADC interrupts related to current or voltage.

Important: If no interrupt is enabled, the system cannot wake up.

To go to LP or ULP State and perform continuous current and voltage measurements, follow these steps:

- Enable at least one of the following interrupts:
  - Set `irqEna[0]` to 1 to enable the watchdog interrupt to wake up the system.
  - Set `irqEna[1]` to 1 to enable the sleep timer to wake up the system.
  - Set `irqEna[4]` to 1 to enable the LIN wake-up detector and to enable the system to wake up due to a LIN wakeup frame (for ZSSC1750 only).
  - Enable any ADC interrupt related to current.
- Set up the sleep timer compare value (register `sleepTCmp`) if needed.
- Configure the `pwrCfgLp` register as follows:
  - Set `pdState` to 0 or 1 to configure the LP State or to 2 to configure the ULP State.
  - Set `pdMeas` to 5 to configure the system to perform continuous current and voltage measurements.
  - Set `lpEnaLp`, `ulpEnaLp`, and `pwrRefbufOcLp` as needed.
- Write $A9_{HEX}$ to register `gotoPd` and then drive the CSN line high.

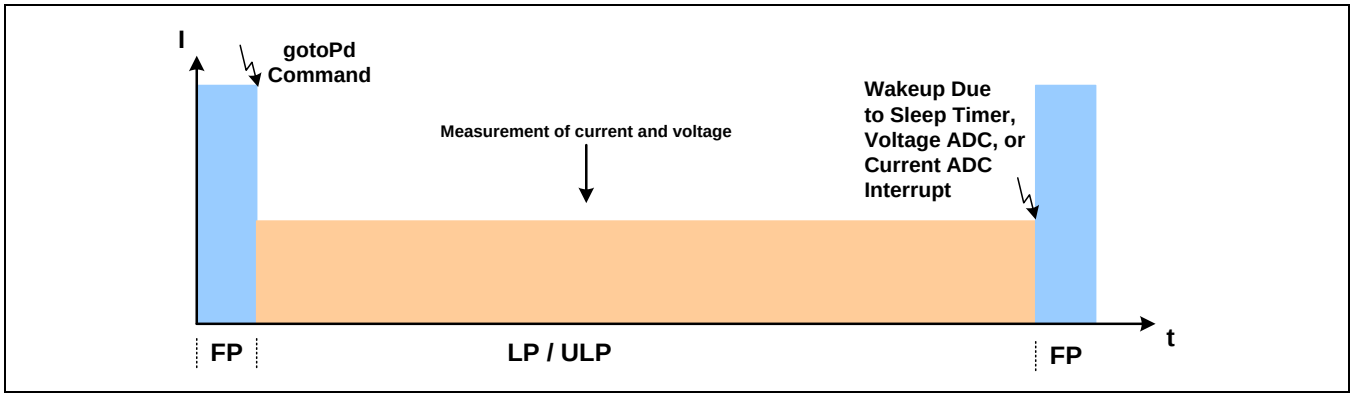
When an enabled interrupt occurs, the system wakes up and the settings from register `pwrCfgFp` are restored. When all blocks have stabilized, the external microcontroller clock MCU_CLK is re-enabled and if coming out of ULP State, the microcontroller reset MCU_RST is released.

Important: If any measurement is active while an enabled interrupt occurs (e.g., the sleep timer expires), the measurement is interrupted and the system returns to the FP State.

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Figure 3.11 Performing Continuous Current and Voltage Measurements during LP/ULP State

Note: The sleep timer interrupt or an ADC interrupt related to voltage or current is used as the wake-up source in this example, but it could also be the watchdog timer interrupt or the LIN wakeup interrupt (for ZSSC1750 only).



3.7.2.7 Performing Continuous Measurements of Current and Internal Temperature during LP/ULP State

This setup is the same as the configuration described in the previous section, except that the internal temperature instead of the voltage is measured. To use this option, `pdMeas` must be set to 6. Possible wake-up sources during this scenario are the watchdog timer interrupt, the sleep timer interrupt, the LIN wakeup interrupt (for ZSSC1750 only), or any of the ADC interrupts related to current or temperature.

3.7.2.8 Performing Continuous Measurements of Current and External Temperature during LP/ULP State

This setup is the same as the configuration described in the previous section, except that the external temperature instead of the internal temperature is measured. To use this option, `pdMeas` must be set to 7. Possible wake-up sources during this scenario are the watchdog timer interrupt, the sleep timer interrupt, the LIN wakeup interrupt (for ZSSC1750 only), or any of the ADC interrupts related to current or temperature.

3.7.3 OFF State

The OFF State is the power-down state with the lowest current consumption, and no ADC measurements are possible. It is intended for long periods of inactivity; e.g., when a car is shipped around the world. During this state, all oscillators and clocks are turned off, the external microcontroller is not powered, and most of the analog blocks are powered down. Only the SBC's digital core and the RX part of the LIN PHY remain powered. The system can only wake up at the detection of a LIN wakeup frame (for ZSSC1750 only) or after power-on reset (for ZSSC1750/51). To go to the OFF State, the following tasks must be done:

- Set `irqEna[4]` to 1 to enable the LIN wake-up detector and to enable the system to wake up due to a LIN wakeup frame (for ZSSC1750 only).
- Set `pdState` to 3 to configure the OFF State as the power-down state to be entered.
- Write $A9_{HEX}$ to register `gotoPd` and drive the CSN line high.

For the ZSSC1750 only, when the LIN RXD line goes low during the OFF State, the low-power oscillator is re-enabled and the digital logic checks if the LIN RXD line is low for a time equal or more than 150µs. If this is true, the complete system returns to the FP State and the external microcontroller is powered up, reset, and clocked again. If the LIN RXD line was low for less than 150µs, the low-power oscillator is powered down again and the system remains in OFF State.

Important: If the LIN wakeup interrupt is not enabled, the system only can only wake up by a power-on reset.

3.7.4 Registers for Power Configuration and the Discreet Current Measurement Count

3.7.4.1 Register "pwrCfgFp" – Power Configuration Register for the FP State

Table 3.18 Register `pwrCfgFp`

Name	Address	Bits	Default	Access	Description
pwrAdcI	53_{HEX}	[0]	0_{BIN}	RW	When set to 1, the current ADC is powered.
pwrAdcV		[1]	0_{BIN}	RW	When set to 1, the voltage/temperature ADC is powered.
Reserved		[2]	0_{BIN}	RW	Reserved; always write as 0.
lpEnaFp		[3]	0_{BIN}	RW	When set to 1, the bias current of the analog blocks is reduced to 10% in the FP State. **Note:** if `ulpEnaFp` is also set to 1, the bias current of the analog blocks is reduced to 15%.
ulpEnaFp		[4]	0_{BIN}	RW	When set to 1, the bias current of the analog blocks is reduced to 5% in the FP State. **Note:** if `lpEnaFp` is also set to 1, the bias current of the analog blocks is reduced to 15%.
pdRefbufOcFp		[5]	0_{BIN}	RW	When set to 1, the offset cancellation of the reference buffer is powered down.
Unused		[7:6]	00_{BIN}	RO	Unused; always write as 0.

3.7.4.2 Register "pwrCfgLp" – Power Configuration Register for Power-Down States

Table 3.19 Register pwrCfgLp

<table>
<tr><th>Name</th><th>Address</th><th>Bits</th><th>Default</th><th>Access</th><th>Description</th></tr>
<tr><td>pdState</td><td rowspan="6">64_{HEX}</td><td>[1:0]</td><td>00_{BIN}</td><td>RW</td><td>Select the power-down state to be entered:<table><tr><td>0 or 1</td><td>LP State</td></tr><tr><td>2</td><td>ULP State</td></tr><tr><td>3</td><td>OFF State</td></tr></table></td></tr>
<tr><td>pdMeas</td><td>[4:2]</td><td>000_{BIN}</td><td>RW</td><td>Type of measurements to be performed during the LP or ULP State:<table><tr><td>0</td><td>No measurements</td></tr><tr><td>1</td><td>Discrete measurements of current</td></tr><tr><td>2</td><td>Discrete measurements of current, voltage, and internal temperature</td></tr><tr><td>3</td><td>Discrete measurements of current, voltage, and external temperature</td></tr><tr><td>4</td><td>Continuous measurements of current</td></tr><tr><td>5</td><td>Continuous measurements of current and voltage</td></tr><tr><td>6</td><td>Continuous measurements of current and internal temperature</td></tr><tr><td>7</td><td>Continuous measurements of current and external temperature</td></tr></table></td></tr>
<tr><td>lpEnaLp</td><td>[5]</td><td>1_{BIN}</td><td>RW</td><td>When set to 1, the bias current of the analog blocks is reduced to 10% in the LP/ULP State.
Note: if <code>ulpEnaLp</code> is also set to 1, the bias current of the analog blocks is reduced to 15%.</td></tr>
<tr><td>ulpEnaLp</td><td>[6]</td><td>0_{BIN}</td><td>RW</td><td>When set to 1, the bias current of the analog blocks is reduced to 5% in the LP/ULP State.
Note: If <code>lpEnaLp</code> is also set to 1, the bias current of the analog blocks is just reduced to 15%.</td></tr>
<tr><td>pwrRefbufOcLp</td><td>[7]</td><td>0_{BIN}</td><td>RW</td><td>When set to 1, the offset cancellation of the reference buffer is powered in LP/ULP State while performing measurements.</td></tr>
</table>

3.7.4.3 Register “gotoPd” – Enter Power-Down State

Table 3.20 Register `gotoPd`

Name	Address	Bits	Default	Access	Description
gotoPd	65_{HEX}	[7:0]	00_{HEX}	WO	Writing $A9_{HEX}$ to this register triggers the PMU to enter the configured power-down state when the CSN line is driven high.

3.7.4.4 Register “discCvtCnt” – Configuration Register for Discrete Measurements

Table 3.21 Register `discCvtCnt`

Name	Address	Bits	Default	Access	Description
discCvtCnt	$5F_{HEX}$	[7:0]	00_{HEX}	RW	Defines the number of "current only" measurements before performing one measurement of current, voltage, and temperature when `pdMeas` is 2 or 3.

3.8 ZSSC1750/51 ADC Unit

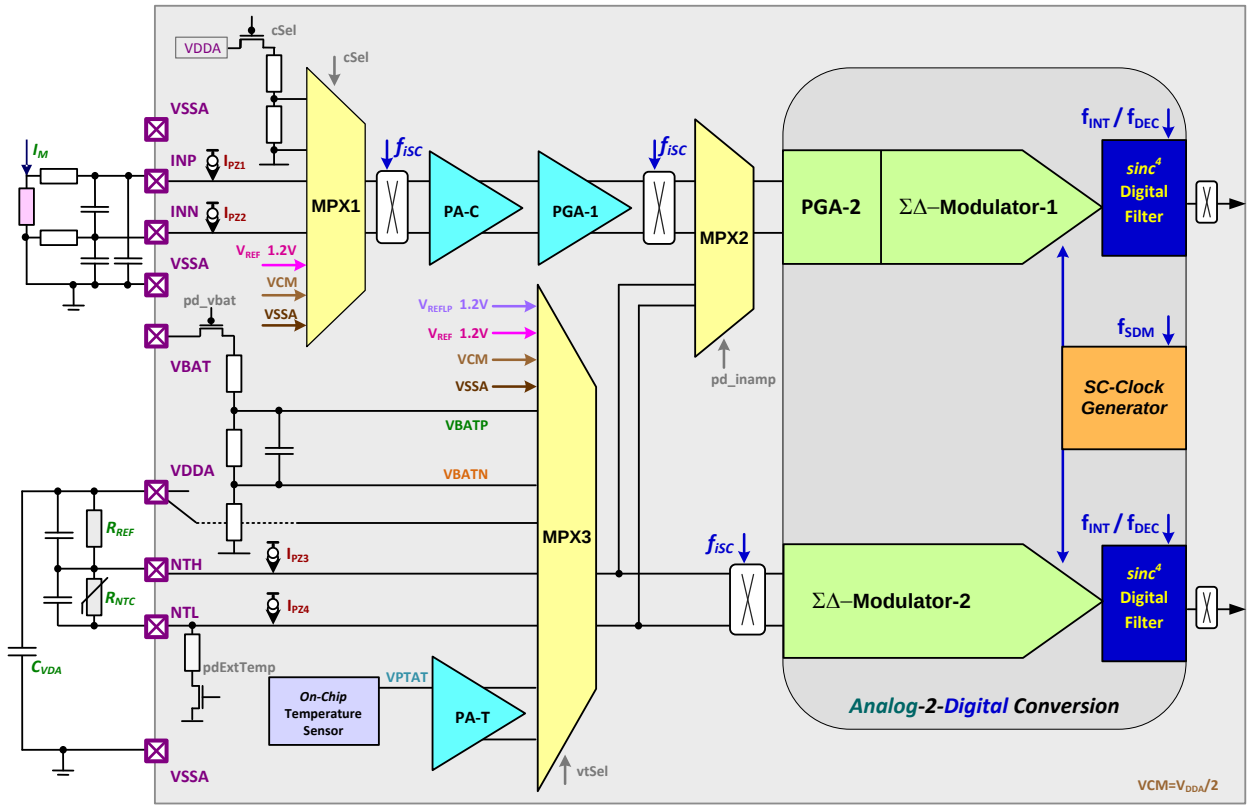
The measurement subsystem incorporates two independent and synchronized high-resolution ADCs for monitoring two channels (SD_ADC blocks). The conversion scheme is based on the sigma-delta modulation (SDM) principle. One channel (ADC-I) is exclusively used for current measurement and includes a pre-amplifier with offset cancellation circuitry. The second channel (ADC-V/T) can be programmed for measuring either voltage or temperature (internal or external).

The raw conversion data can be post-processed by calibration data to achieve a minimum offset and gain error (gain and offset correction). The conversion results are stored in the register file from which they can be read via the SPI digital communication interface. A completed conversion is flagged by a “data ready” signal that can be used as an interrupt source for the external microcontroller. A functional block diagram of the analog circuitry is shown in Figure 3.12.

The purpose of this analog architecture is to achieve a maximum level of diagnostic capability and flexibility as well as best accuracy.

The digital ADC unit consists of the data processing unit and control logic. The control logic generates the clocks and control signals for the analog SD-ADCs as well as control signals for the data processing part of the ADC unit.

Figure 3.12 Functional Block Diagram of the Analog Measurement Subsystem



PA-C = Preamplifier Current; PA-T = Preamplifier Temperature; MPX = Multiplexer; PGA = Programmable Gain Amplifier

3.8.1 ADC Clocks

Two clocks are generated in the digital part of the ADC unit and are driven to the analog part. The SDM clock is used for both SD-ADCs. The chop clock is used for the chopping operation within the SD-ADCs. The base for both clocks is the multiplexed clock muxClk, which is a 4MHz clock in FP State and a 125kHz clock in LP/ULP State.

3.8.1.1 ADC Clocks in FP State

In the FP State, the SDM clock is generated from the 4MHz clock by dividing it by two times the value programmed into bit field `sdmClkDivFp` in register `sdmClkCfgFp` (see Table 3.24):

$$f_{SDM} = \frac{f_{HP}}{2 * \texttt{sdmClkDivFp}} \qquad f_{HP} = 4\,MHz \tag{4}$$

Important: When `sdmClkDivFp` is set to 0, the frequency of SDM clock is 2MHz.

The chop clock is generated from the SDM clock by further dividing it by 2, 4, 8, or 16 depending on the setting of the sdmChopClkDiv field in register adcGomd (see Table 3.55):

$$f_{CHOP} = f_{SDM} * 2^{-(sdmClkChopDiv+1)} \quad (5)$$

Although the clock bases used to generate the SDM and the chop clock have a frequency of 4MHz, the position of the clock edges used for the clock generation can be shifted relative to the 4MHz clock used for the digital logic to obtain optimal noise behavior for the analog section. The 4MHz clock used to generate the SDM clock ($CLK_{SDMBASE}$) is delayed relative to the 4MHz clock used for the digital logic (CLK_{MUXCLK}) by one to four 20MHz clock cycles (CLK_{HPOSC}) depending on the settings of the field sdmPos in register sdmClkCfgFp (Table 3.24). The 4MHz clock used to generate the chop clock ($CLK_{CHOPBASE}$) is delayed relative to the 4MHz clock used for the digital logic ($CLK_{SDMBASE}$) by zero to four 20MHz clock cycles depending on the settings of field sdmPos2 and field sdmPos in register sdmClkCfgFp. The delay in the number of 20MHz clock cycles of the chop clock relative to the SDM clock can be calculated using the following formula:

$$delay = (sdmPos2 - sdmPos) \bmod 5 \quad (6)$$

Important: The delay programmed into field sdmPos2 is related to CLK_{MUXCLK}, not to $CLK_{SDMBASE}$. Table 3.22 shows the value that must be programmed into field sdmPos2 depending on the field sdmPos and the desired delay.

Table 3.22 Value for sdmPos2 Depending on sdmPos and Desired Clock Delay from SDM to Chop Clock

Delay	sdmPos2			
	sdmPos =0	sdmPos =1	sdmPos=2	sdmPos=3
0	0	1	2	3
1	1	2	3	4
2	2	3	4	0
3	3	4	0	1
4	4	0	1	2

Figure 3.13 FP ADC Clocking Scheme for `sdmPos` = `sdmPos2` = 2; `sdmClkDivFp` = 1; `sdmChopClkDiv` = 0

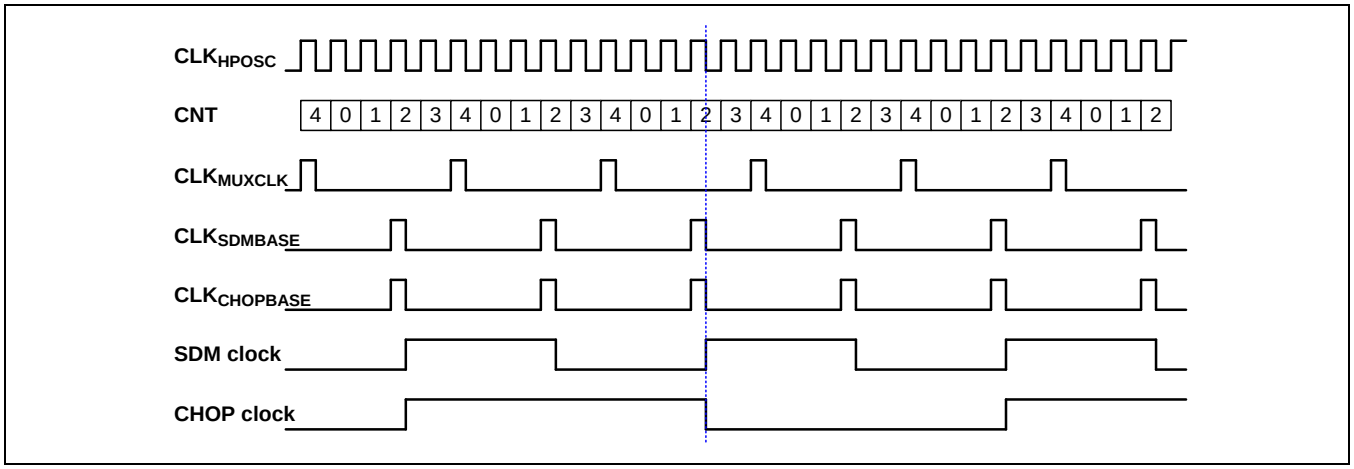


Figure 3.14 FP ADC Clocking for `sdmPos` = 1 and `sdmPos2` = 4; `sdmClkDivFp` = 1; `sdmChopClkDiv` = 0

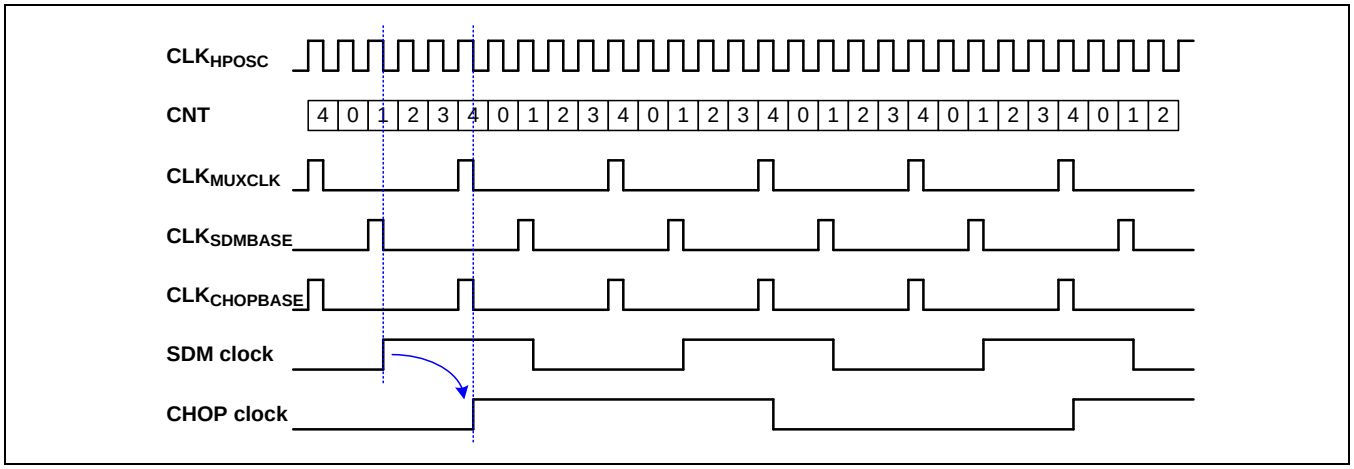


Figure 3.15 FP ADC Clocking for sdmPos = 3 and sdmPos2 = 0; sdmClkDivFp = 1; sdmChopClkDiv = 0

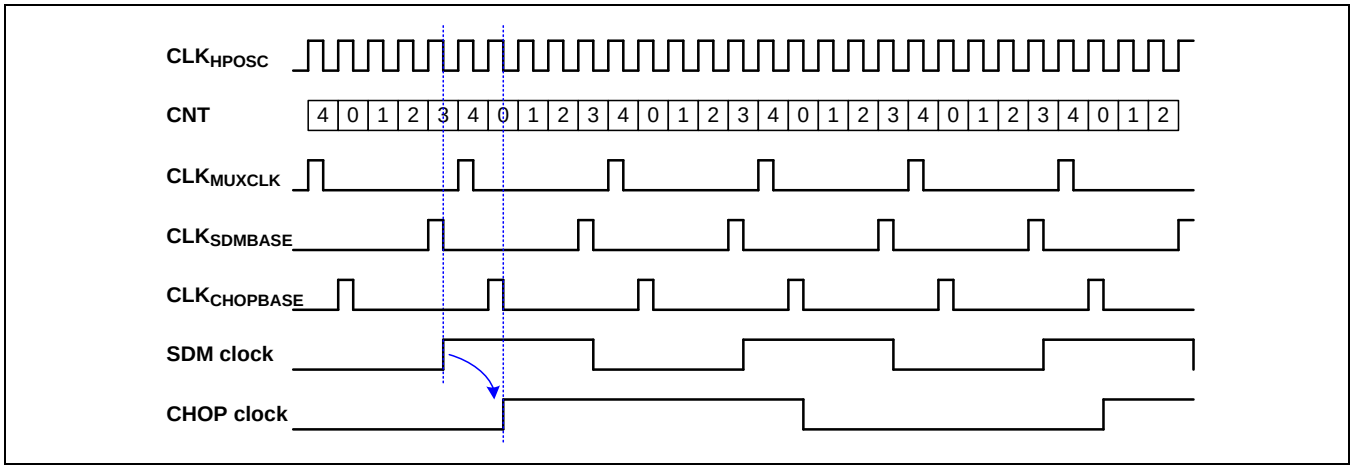
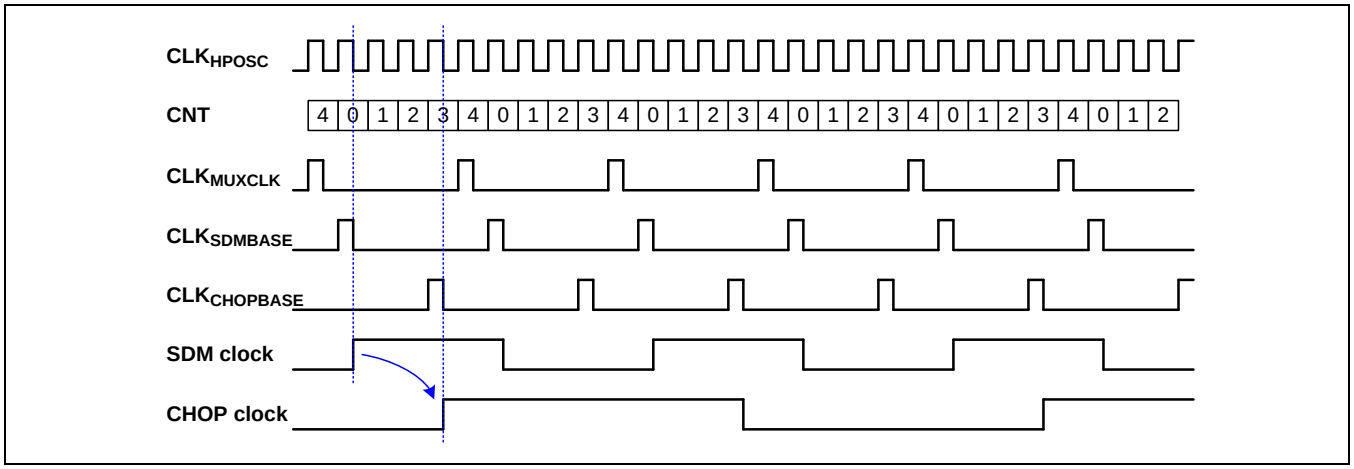


Figure 3.16 FP ADC Clocking for sdmPos = 0 and sdmPos2 = 3; sdmClkDivFp = 1; sdmChopClkDiv = 0



3.8.1.2 ADC Clocks in the LP/ULP State

In the LP or ULP State, the SDM clock is generated from the 125 kHz clock (CLK_{LPOSC}) by dividing it by two times the value programmed into register `sdmClkDivLp` (see Table 3.23):

$$f_{SDM} = \frac{f_{LP}}{2 * sdmClkDivLp}; \quad f_{LP} = 125\,kHz \tag{7}$$

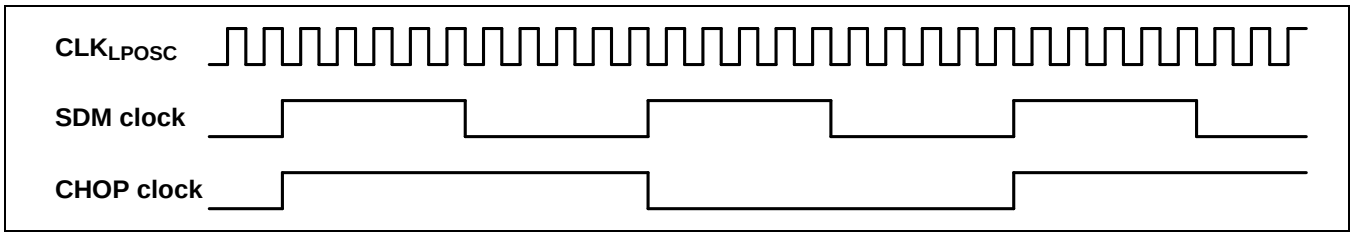
Important: When `sdmClkDivLp` is set to 0, the frequency of the SDM clock is 62.5 kHz.

The chop clock is generated from the SDM clock by further dividing it by 2, 4, 8, or 16 depending on the setting of the `sdmChopClkDiv` field in register `adcGomd`:

$$f_{CHOP} = f_{SDM} * 2^{-(sdmChopClkDiv+1)} \quad (8)$$

Both the SMD and chop clocks are generated from the same 125kHz clock that is used for the digital logic. Shifting of the clocks used to generate the SDM and chop clock is not possible and not needed as the analog clocks are generated on the falling clock edge where the digital logic is already stable and will not influence the analog section.

Figure 3.17 LP/ULP ADC Clocking Scheme; `sdmClkDivLp` = 5; `sdmChopClkDiv` = 0



3.8.1.3 Register "sdmClkCfgLp" – Configuration Register for the SDM Clocks in the LP/ULP State

Table 3.23 Register `sdmClkCfgLp`

Name	Address	Bits	Default	Access	Description
sdmClkDivLp[7:0]	$B0_{HEX}$	[7:0]	18_{HEX}	RW	Clock divider value for the SDM clock in the LP and ULP States related to the 125KHz base clock. With sdmClkDivLP = 0, the divider value is 2.
sdmClkDivLp[9:8]	$B1_{HEX}$	[1:0]	00_{BIN}	RW	
Unused		[7:2]	$00\ 0000_{BIN}$	RO	Unused; always write as 0.

3.8.1.4 Register "sdmClkCfgFp" – Configuration Register for the SDM Clocks in the FP State

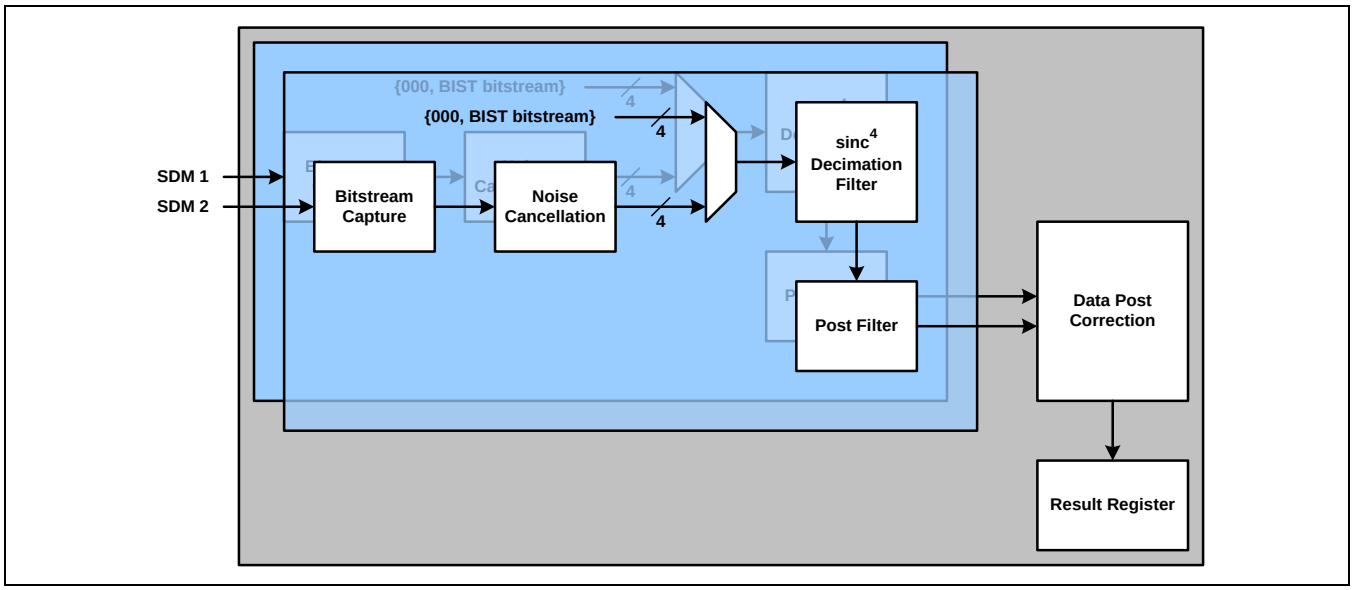
Table 3.24 Register `sdmClkCfgFp`

Name	Address	Bits	Default	Access	Description
sdmClkDivFp[7:0]	$B2_{HEX}$	[7:0]	08_{HEX}	RW	Clock divider value for the SDM clock in the FP State related to the 4MHz base clock $f_{HP.}$ If 0, then the SDM clock is 2MHz.
sdmClkDivFp[9:8]	$B3_{HEX}$	[1:0]	00_{BIN}	RW	
Unused		[2]	0_{BIN}	RO	Unused; always write as 0
sdmPos2		[5:3]	010_{BIN}	RW	Position of the chop clock ($CLK_{CHOPBASE}$) relative to the base clock CLK_{MUXCLK} (possible values = 0 to 4)
sdmPos		[7:6]	10_{BIN}	RW	Position of the SDM clock ($CLK_{SDMBASE}$) relative to the base clock CLK_{MUXCLK}

3.8.2 ADC Data Path

The incoming 2nd and 3rd order bit streams from the analog part of the SD-ADCs are first captured and then driven through a 3rd order noise shaping filter as illustrated in Figure 3.18. The digital conversion is accomplished by a 4th order low-pass filter (sinc4 decimation filter). The bit stream capturing and the noise shaping filter cannot be directly changed by the user (no configuration registers), but the selected oversampling rate (`adcSamp` register field `osr`) affects the sinc4 decimation filter (one output value per N input values).

Figure 3.18 Functional Block Diagram of the Digital ADC Data Path



A simple post filter (moving average filter) is placed behind the sinc4 decimation filter. The user can select the averaging function (no averaging; 2-stage averaging; or 3-stage averaging) via the `avgFiltCfg` bit field in the `adcSamp` register (see Table 3.56) when chopping is disabled (see section 3.8.4.4). When chopping is enabled, the 2-stage averaging is used independently of the filter configuration.

The function of the 2-stage averaging filter is

$$x_{out}(t) = \frac{x_{in}(t) + x_{in}(t-1)}{2} \quad (9)$$

The function of the 3-stage averaging filter is

$$x_{out}(t) = \frac{x_{in}(t) + 2 * x_{in}(t-1) + x_{in}(t-2)}{4} \quad (10)$$

Where t = current sample

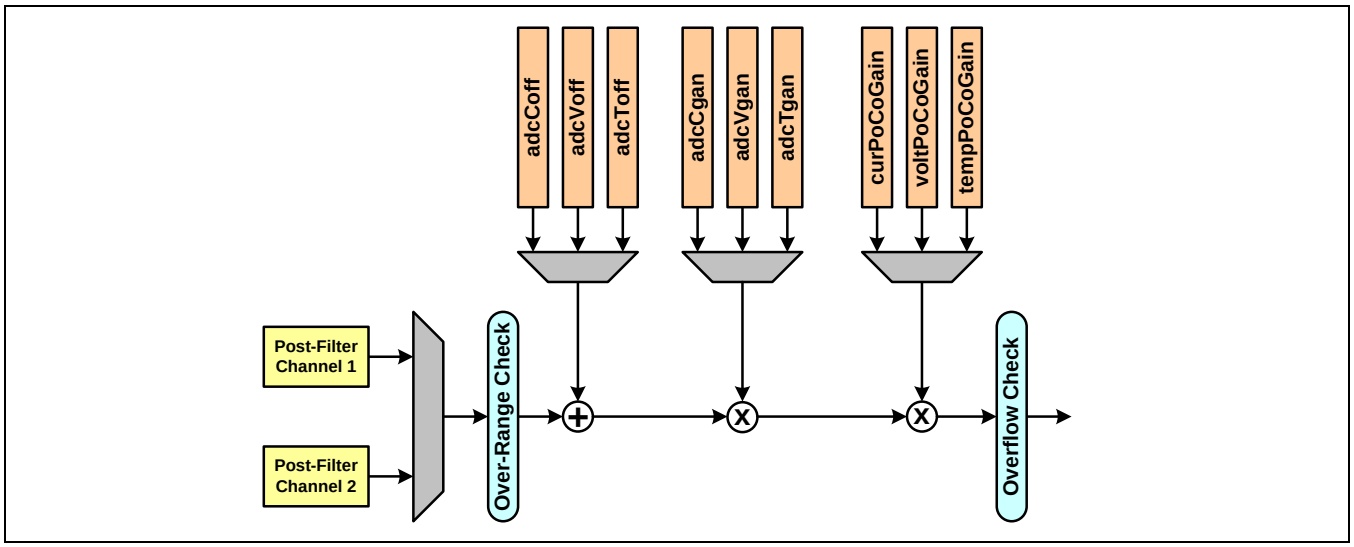
t-1 = previous sample

t-2 = sample before previous sample, etc.

3.8.2.1 Data Post-Correction Block

The data post-correction block performs the offset and gain correction of the post-filtered conversion data as well as the over-range and the overflow detection.

Figure 3.19 Data Post Correction



First, an over-range check is performed on the incoming data. Values that are outside the interval [-0.75; 0.75) are always mapped to the corresponding interval boundary. This is done for better results as the ADC accuracy decreases for large input values. The user can enable a “set interrupt” strobe for each of the two channels by setting the `adcAcmp` register bits `COvrEna` and `VTOvrEna` to 1 (see Table 3.54).

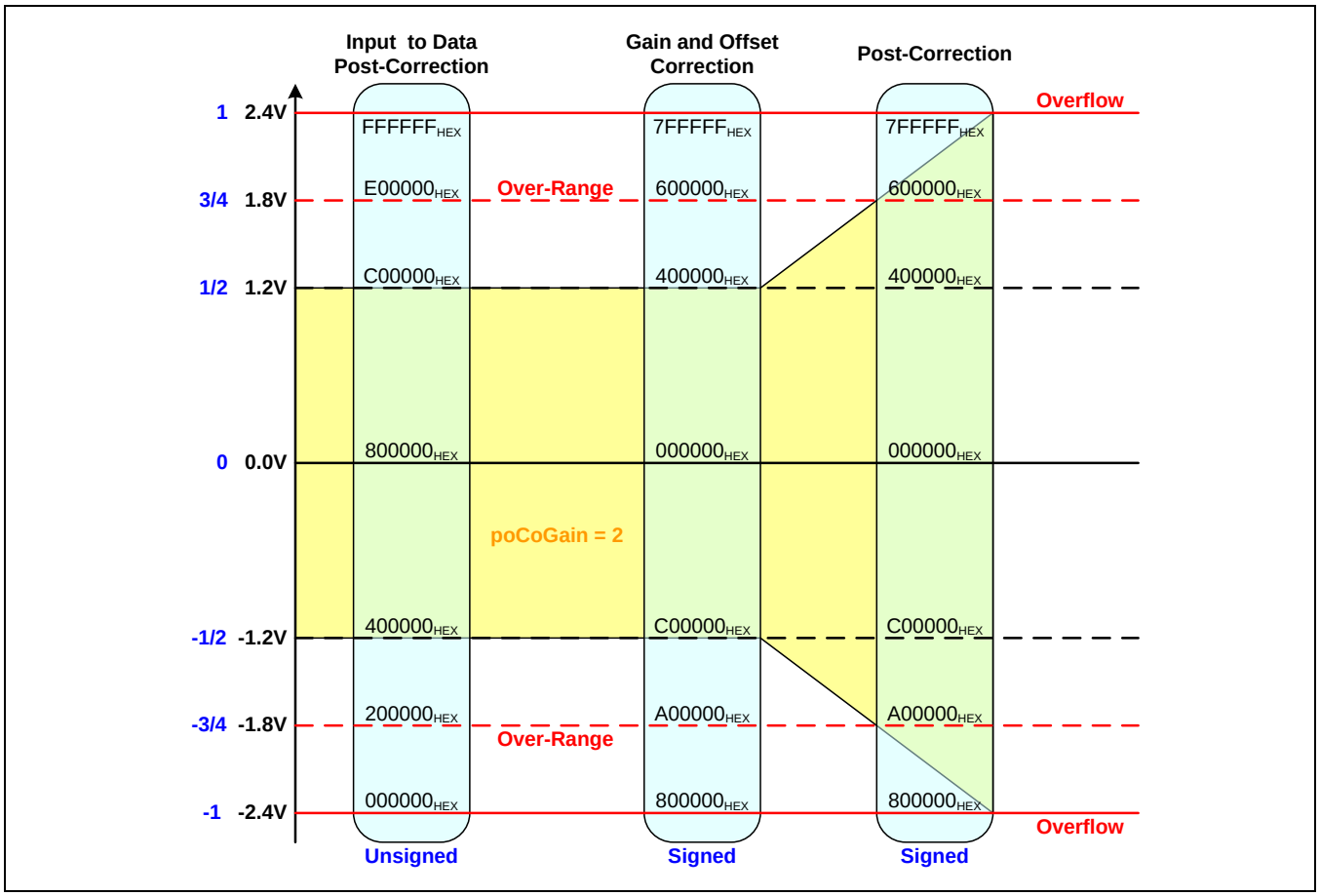
Note: The “set interrupt” strobes go to the interrupt controller. They have a different meaning than the corresponding “interrupt enable” bits (interrupt bits [15:14] in the `irqEna` register). The “set interrupt” bits are used to select whether the interrupt status bits will be set or not; the “interrupt enable” bits select whether the interrupt status bits will drive the interrupt line or not.

After the over-range check, a programmable offset, interpreted as a number in the range [-1.0; 1.0), is added to the data. Three registers allow setting different offsets for current, voltage, and temperature: `adcCoff`, `adcVoff`, and `adcToff` (see Table 3.25, Table 3.27, and Table 3.29 respectively).

The offset correction is followed by two multiplication stages. In the first multiplication stage, individual gain factors for current (`adcCgan`), voltage (`adcVgan`), or temperature (`adcTgan`), interpreted as numbers in the range [0.0; 2.0), are multiplied by the offset corrected data (see Table 3.26, Table 3.28, and Table 3.30 respectively). The second multiplication stage is used to shift the significant data into the most significant bits of the result register. The data is multiplied by 1, 2, 4, or 8, which can be individually selected for current, voltage, and temperature via the `curPoCoGain`, `voltPoCoGain`, and `tempPoCoGain` fields in the `adcPoCoGain` register (see Table 3.31).

Figure 3.20 Data Representation through Data Post Correction including Over-Range and Overflow Levels

Note: the yellow area represents the usable data space to avoid overflow when the post correction gain is 2.

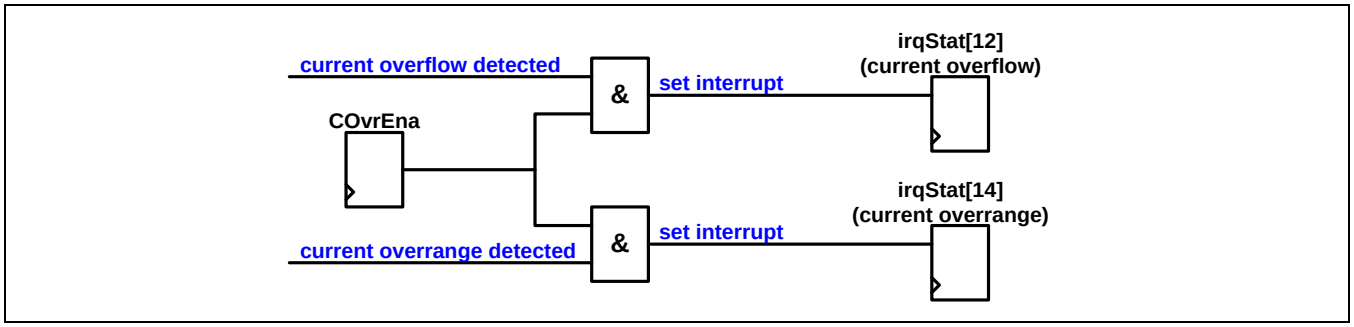


An overflow check is performed on the output of the second multiplication stage as the result might be out of the representable range of [-1.0; 1.0). The user can also enable a “set interrupt” strobe for each of the two channels by setting the `adcAcmp` register bits `COvrEna` and/or `VTOvrEna` to 1 (same bits as for the over-range check).

Note: Although the same “set interrupt strobe enable” bit is used for over-range and overflow, independent interrupt status bits can be individually enabled or disabled.

Figure 3.21 illustrates the common enable `CovrEna` for the interrupt strobes for current over-range and overflow. The function of `VTOvrEna` as the common enable for the interrupt strobes for voltage/temperature over-range and overflow conditions is similar.

Figure 3.21 Common Enable for the "set overrange" and "set overflow" Interrupt Strobes for Current



3.8.2.2 Register "adcCoff" – Offset Correction Value for Current Channel

Table 3.25 Register `adcCoff`

Name	Address	Bits	Default	Access	Description
adcCoff[7:0]	33_{HEX}	[7:0]	00_{HEX}	RW	Offset value for current value; interpreted as a number in the range [-1.0; 1.0) formatted in 2's complement representation. Programmable offset range = +/- 2 V_{REF}; V_{REF}= full-scale range ADC. **Note:** The initial value is loaded from OTP after reset.
adcCoff[15:8]	34_{HEX}	[7:0]	00_{HEX}	RW	
adcCoff[23:16]	35_{HEX}	[7:0]	00_{HEX}	RW	

3.8.2.3 Register "adcCgan" – Gain Correction Value for Current Channel

Table 3.26 Register `adcCgan`

Name	Address	Bits	Default	Access	Description
adcCgan[7:0]	30_{HEX}	[7:0]	00_{HEX}	RW	Gain value for current value; interpreted as a number in the range [0.0; 2.0). **Note:** The initial value is loaded from OTP after reset.
adcCgan[15:8]	31_{HEX}	[7:0]	00_{HEX}	RW	
adcCgan[23:16]	32_{HEX}	[7:0]	80_{HEX}	RW	

3.8.2.4 Register "adcVoff" – Offset Correction Value for Voltage Channel

Table 3.27 Register `adcVoff`

Name	Address	Bits	Default	Access	Description
adcVoff[7:0]	39_{HEX}	[7:0]	00_{HEX}	RW	Offset value for voltage value; interpreted as a number in the range [-1.0; 1.0) formatted in 2's complement representation. Programmable offset range = +/- 2 V_{REF}; V_{REF}= full-scale range ADC. **Note:** The initial value is loaded from OTP after reset.
adcVoff[15:8]	$3A_{HEX}$	[7:0]	00_{HEX}	RW	
adcVoff[23:16]	$3B_{HEX}$	[7:0]	00_{HEX}	RW	

3.8.2.5 Register "adcVgan" – Gain Correction Value for Voltage Channel

Table 3.28 Register adcVgan

Name	Address	Bits	Default	Access	Description
adcVgan[7:0]	36_{HEX}	[7:0]	00_{HEX}	RW	Gain value for voltage value; interpreted as a number in the range [0.0; 2.0) **Note:** The initial value is loaded from OTP after reset.
adcVgan[15:8]	37_{HEX}	[7:0]	00_{HEX}	RW	
adcVgan[23:16]	38_{HEX}	[7:0]	80_{HEX}	RW	

3.8.2.6 Register "adcToff" – Offset Correction Value for Temperature Channel

Table 3.29 Register adcToff

Name	Address	Bits	Default	Access	Description
adcToff[7:0]	$3E_{HEX}$	[7:0]	00_{HEX}	RW	Offset value for temperature value; interpreted as a number in the range [-1.0; 1.0) **Note:** The initial value is loaded from OTP after reset.
adcToff[15:8]	$3F_{HEX}$	[7:0]	00_{HEX}	RW	

3.8.2.7 Register "adcTgan" – Gain Correction Value for Temperature Channel

Table 3.30 Register adcTgan

Name	Address	Bits	Default	Access	Description
adcTgan[7:0]	$3C_{HEX}$	[7:0]	00_{HEX}	RW	Gain value for temperature value; interpreted as a number in the range [0.0; 2.0) **Note:** The initial value is loaded from OTP after reset.
adcTgan[15:8]	$3D_{HEX}$	[7:0]	80_{HEX}	RW	

3.8.2.8 Register "adcPoCoGain" – Post Correction Gain Configuration

Table 3.31 Register adcPoCoGain

Name	Address	Bits	Default	Access	Description
curPoCoGain	57_{HEX}	[1:0]	00_{BIN}	RW	Post correction gain for the current channel: 0 – Gain factor is 1 1 – Gain factor is 2 2 – Gain factor is 4 3 – Gain factor is 8
voltPoCoGain		[3:2]	00_{BIN}	RW	Post correction gain for the voltage channel: 0 – Gain factor is 1 1 – Gain factor is 2 2 – Gain factor is 4 3 – Gain factor is 8
tempPoCoGain		[5:4]	00_{BIN}	RW	Post correction gain for the temperature channel: 0 – Gain factor is 1 1 – Gain factor is 2 2 – Gain factor is 4 3 – Gain factor is 8
Unused		[7:6]	00_{BIN}	RO	Unused; always write as 0.

3.8.3 ADC Operating Modes and Result Registers

3.8.3.1 Single Measurement Results

Each value coming from the data post-correction block is the result of a single measurement. These values are signed and stored in the corresponding result registers `adcCdat`, `adcVdat`, `adcTdat`, or `adcRdat` (see Table 3.32 through Table 3.35).The following formulas can be used to calculate the battery current and the battery voltage from the result register values:

$$I_{BAT} = \frac{adcCdat * 2 * V_{REF}}{R_{SHUNT} * 2^{23} * G_{ANA} * G_{POCO}} \quad (11)$$

$$V_{BAT} = \frac{adcVdat * 24 * 2 * V_{REF}}{2^{23} * G_{POCO}} \quad (12)$$

Where:

I_{BAT}	Battery current
V_{BAT}	Battery voltage
G_{ANA}	Analog gain in current path (`pgaIfc` $*$ `pga1` $*$ `pga2`; see Table 3.36)
G_{POCO}	Digital gain in post-correction stage (second multiplication; see Table 3.31)
R_{SHUNT}	Shunt resistance
V_{REF}	Reference voltage
`adcCdat`	Register value for current
`adcVdat`	Register value for voltage

3.8.3.2 Register "adcCdat" – Single Current Measurement Value

Table 3.32 Register adcCdat

Name	Address	Bits	Default	Access	Description
adcCdat[7:0]	02_{HEX}	[7:0]	00HEX	RO	Conversion result of a single current measurement (signed value)
adcCdat[15:8]	03_{HEX}	[7:0]	00HEX	RO	
adcCdat[23:16]	04_{HEX}	[7:0]	00HEX	RO	

3.8.3.3 Register "adcVdat" – Single Voltage Measurement Value

Table 3.33 Register adcVdat

Name	Address	Bits	Default	Access	Description
adcVdat[7:0]	05_{HEX}	[7:0]	00HEX	RO	Conversion result of a single voltage measurement (signed value)
adcVdat[15:8]	06_{HEX}	[7:0]	00HEX	RO	
adcVdat[23:16]	07_{HEX}	[7:0]	00HEX	RO	

3.8.3.4 Registers "adcTdat" and "adcRdat" – Single Temperature Measurement Values

Table 3.34 Register adcTdat

Name	Address	Bits	Default	Access	Description
adcTdat[7:0]	$0A_{HEX}$	[7:0]	00HEX	RO	Conversion result of a single temperature value (signed value; inverted); this value is either the internally measured temperature or the NTC value of an external temperature measurement. **Important:** This value is sign-inverted.
adcTdat[15:8]	$0B_{HEX}$	[7:0]	00HEX	RO	

Table 3.35 Register adcRdat

Name	Address	Bits	Default	Access	Description
adcRdat[7:0]	08_{HEX}	[7:0]	00HEX	RO	Conversion result of a single temperature measurement by reading a voltage across the reference resistor (external temperature measurement only).
adcRdat[15:8]	09_{HEX}	[7:0]	00HEX	RO	

3.8.3.5 Register “adcGain” – Analog Gain Configuration in the Current Path

Table 3.36 Register `adcGain`

Name	Address	Bits	Default	Access	Description
pgaIfc	52_{HEX}	[1:0]	00_{BIN}	RW	Sets the gain of the PA-C preamplifier in the analog current path: 0 Gain factor is 1 1 Gain factor is 2 2 Gain factor is 4 3 Gain factor is 8
pga1		[3:2]	00_{BIN}	RW	Sets the gain of the PGA-1 programmable gain amplifier in the analog current path: 0 Gain factor is 1 1 Gain factor is 2 2 Gain factor is 4 3 Gain factor is 8
pga2		[4]	0_{BIN}	RW	Sets the gain of PGA-2 programmable gain amplifier in the analog current path: 0 Gain factor is 4 1 Gain factor is 8
Unused		[7:5]	000_{BIN}	RO	Unused; always write as 0.

3.8.3.6 Result Counter Functionality and Conversion Ready Strobes

Three status bits are available in the interrupt status (`irqStat[7:5]`) that signal that the conversion of current, voltage, or temperature has been completed. The “set interrupt” strobe is generated for each completed temperature measurement. For the voltage and current measurements, the user can independently select whether the corresponding “set interrupt” strobe will be generated after each single measurement (SRCS – single result count sequence) or after N measurements (MRCS – multi-result count sequence).

The register `adcCrcl` configures the number of current measurements before the current conversion ready strobe is generated; the maximum number is 65535 (see Table 3.37). Setting this register to 0 disables the result count functionality, which means that SRCS is configured. The present result counter value can always be read from the register `adcCrcv` (see Table 3.38). The result counter is reset when the bit field `startAdcC` in register `adcCtrl` is set (rising edge) in the FP State (see Table 3.58) or at the start of the first measurement in LP/ULP State. It is set to 1 at the end of the first measurement after the limit defined in `adcCrcl` has been reached.

The register `adcVrcl` configures the number of measurements before the voltage conversion ready strobe is generated, the maximum number is 15 (see Table 3.39). Setting this register to 0 disables the result count functionality, which means that SRCS is configured. The present result counter value can always be read from the register `adcVrcv` (see Table 3.40). The result counter is reset when `startAdcV` in register `adcCtrl` is set (rising edge) in the FP State or at the start of the first measurement in the LP/ULP State. It is set to 1 at the end of the first measurement after the limit defined in `adcVrcl` was reached.

Note: Setting register `adcCrcl` or `adcVrcl` to 1 also leads to SRCS in the corresponding channel.

3.8.3.7 Register "adcCrcl" – Current Result Count Limit

Table 3.37 Register adcCrcl

Name	Address	Bits	Default	Access	Description
adcCrcl[7:0]	40_{HEX}	[7:0]	00_{HEX}	RW	Number of current measurements before the current conversion ready strobe is generated. **Note:** Setting this bit to 0 disables this functionality, and the strobe is generated after each current measurement.
adcCrcl[15:8]	41_{HEX}	[7:0]	00_{HEX}	RW	

3.8.3.8 Register "adcCrcv" – Current Result Count Value

Table 3.38 Register adcCrcv

Name	Address	Bits	Default	Access	Description
adcCrcv[7:0]	$1B_{HEX}$	[7:0]	00_{HEX}	RO	Present value of the current result counter.
adcCrcv[15:8]	$1C_{HEX}$	[7:0]	00_{HEX}	RO	

3.8.3.9 Register "adcVrcl" – Voltage Result Count Limit

Table 3.39 Register adcVrcl

Name	Address	Bits	Default	Access	Description
adcVrcl	45_{HEX}	[3:0]	0000_{BIN}	RW	Number of voltage measurements before the voltage conversion ready strobe is generated. **Note:** Setting this bit to 0 disables this functionality, and the strobe is generated after each voltage measurement.
Unused		[7:4]	0000_{BIN}	RO	Unused; always write as 0.

3.8.3.10 Register "adcVrcv" – Voltage Result Count Value

Table 3.40 Register adcVrcv

Name	Address	Bits	Default	Access	Description
adcVrcv	$1E_{HEX}$	[3:0]	0000_{BIN}	RO	Present value of the voltage result counter.
Unused		[7:4]	0000_{BIN}	RO	Unused; always write as 0.

3.8.3.11 Current Threshold Comparator Functionality

The current threshold comparator functionality is used to monitor the current level and to generate an interrupt (`irqStat[8]`) if the absolute current value exceeds a programmable limit for a configurable number of conversion results. This functionality is enabled if the field `ctcvMode` in register `adcAcmp` is set to a non-zero value (see Table 3.54Table 3.58). If enabled, this function is always triggered when a new current value is measured. The absolute value of the most significant 17 bits of the measured current value is compared to the expanded programmable threshold register `adcCrth` (see Table 3.41):

$$\mathrm{abs}(\mathtt{adcCdat}\ [23:7]) \geq \{0, \mathtt{adcCrth}\} \tag{13}$$

When the current threshold comparator functionality is enabled, the current threshold counter is used to count the number of conversions where the absolute current value is above the threshold. If the absolute current value is greater than or equal to the programmed threshold (above formula is true), the internal current threshold counter is incremented (until it reaches its maximum value FF_{HEX}). Otherwise the counter is either decremented (if `ctcvMode` field in register `adcAcmp` set to 1) or reset (if `ctcvMode` set to 2), or it remains unchanged (if `ctcvMode` set to 3). The present value of the current threshold counter can be read from the register `adcCtcv` (see Table 3.43).

Note: When bit field `ctcvMode` in register `adcAcmp` is set to 00_{BIN}, the current threshold comparator functionality is disabled and register `adcCrtv` is always 0.

Note: When `ctcvMode` is set to 01_{BIN}, the current threshold counter is not decremented when the counter is 0.

After each comparison of the absolute current value versus the current threshold level and after the current threshold counter has been updated, the internal current threshold counter is compared to the current threshold counter limit (register `adcCtcl`; see Table 3.42). Whenever the current threshold counter is greater than or equal to the programmable limit, a “set interrupt” strobe is generated.

Note: When the current threshold counter has reached its limit and it is configured to keep its value if the limit is not reached, a “set interrupt” strobe is generated for each new measurement even if the new value is below threshold.

The current threshold counter is reset to 0 for the following conditions:

- If `ctcvMode` is set to 2 and the absolute current value is below the programmed threshold `adcCrth`
- On assertion of `startAdcC` (rising edge) in the FP State
- At the start of the first conversion in the LP or ULP State
- Each time the result counter is reset (if the result counter is enabled) and the current threshold counter reset mode bit (bit `ctcvRstMode` in register `adcAcmp`) is set to 1

3.8.3.12 Register "adcCrth" – Absolute Current Threshold

Table 3.41 Register `adcCrth`

Name	Address	Bits	Default	Access	Description
adcCrth[7:0]	42_{HEX}	[7:0]	00_{HEX}	RW	Absolute current threshold (unsigned value). When using current comparator threshold functionality, the absolute current value is compared to {0, adcCrth}.
adcCrth[15:8]	43_{HEX}	[7:0]	00_{HEX}	RW	

3.8.3.13 Register "adcCtcl" – Current Threshold Counter Limit

Table 3.42 Register `adcCtcl`

Name	Address	Bits	Default	Access	Description
adcCtcl	44_{HEX}	[7:0]	00_{HEX}	RW	Current threshold counter limit. This register defines the number of current measurements that must be greater than or equal to the threshold `adcCrth` before the interrupt is set.

3.8.3.14 Register "adcCtcv" – Current Threshold Counter Value

Table 3.43 Register `adcCtcv`

Name	Address	Bits	Default	Access	Description
adcCtcv	$1D_{HEX}$	[7:0]	00_{HEX}	RO	Present current threshold counter value.

3.8.3.15 Current Accumulator Functionality

The current accumulator functionality is used to sum up all current conversion results. The present accumulator value can be read from the register `adcCaccu` (signed value; see Table 3.45). Positive conversion results increment the accumulator register, negative conversion results decrement it. The accumulator register saturates at its minimum and maximum value.

The current accumulator is reset to 0 under these conditions:

- On assertion of `startAdcC` (rising edge) in the FP State
- At the start of the first conversion in the LP or ULP State
- Each time the result counter is reset (if the result counter is enabled) and the current accumulator reset mode bit (bit `accuRstMode` in register `adcAcmp`) is set to 1

Note: The current accumulator functionality can be used to calculate the mean value of the current.

The current accumulator is also compared to a programmable signed accumulator threshold value (register adcCaccTh). This comparison can be used to generate a “set interrupt” strobe for irqStat[11]; however, to enable the generation of the “set interrupt” strobe, bit CAccuThEna in register adcAcmp must be set to 1 (see Table 3.54). The “set interrupt” strobe is always generated on update of the accumulator register when

- adcCaccTh is greater than 0 and adcCaccu is greater than adcCaccTh
- adcCaccTh is lower than 0 and adcCaccu is lower than adcCaccTh
- adcCaccTh is equal to 0 and adcCaccu is not equal to 0

3.8.3.16 Register “adcCaccTh” – Current Accumulator Threshold Value

Table 3.44 Register adcCaccTh

Name	Address	Bits	Default	Access	Description
adcCaccTh[7:0]	48_{HEX}	[7:0]	00_{HEX}	RW	Signed threshold value for current accumulator mode
adcCaccTh[15:8]	49_{HEX}	[7:0]	00_{HEX}	RW	
adcCaccTh[23:16]	$4A_{HEX}$	[7:0]	00_{HEX}	RW	
adcCaccTh[31:24]	$4B_{HEX}$	[7:0]	00_{HEX}	RW	

3.8.3.17 Register “adcCaccu” – Current Accumulator Value

Table 3.45 Register adcCaccu

Name	Address	Bits	Default	Access	Description
adcCaccu[7:0]	$0C_{HEX}$	[7:0]	00_{HEX}	RO	Present current accumulator value
adcCaccu[15:8]	$0D_{HEX}$	[7:0]	00_{HEX}	RO	
adcCaccu[23:16]	$0E_{HEX}$	[7:0]	00_{HEX}	RO	
adcCaccu[31:24]	$0F_{HEX}$	[7:0]	00_{HEX}	RO	

3.8.3.18 Voltage Threshold Comparator and Voltage Accumulator Functionality

The ZSSC1750/51 also provides a threshold comparator as well as an accumulator comparator for the battery voltage channel but with reduced functionality.

If the VThSel bit in register adcAcmp is set to 0, the absolute value of the most significant 17 bits of a single voltage measurement (register adcVdat) is compared to the programmable voltage threshold (register adcVTh; see Table 3.46). In this case, register adcVTh is interpreted as an unsigned value. There is also no counter functionality. Whenever the absolute voltage value is below the programmed threshold, a “set interrupt” strobe for irqStat[9] is generated if the strobe generation is enabled (the field VThWuEna in register adcAcmp is set to 1).

$$\mathrm{abs}(\mathrm{adcVdat}\ [23:7]) < \{0, \mathrm{adcVTh}\} \tag{14}$$

When bit VThSel in register adcAcmp is set to 1, the voltage accumulator functionality is enabled. The voltage result counter functionality must also be enabled (register adcVrcl > 0). The voltage accumulator functionality is used to sum up all voltage conversion results. In contrast to the current channel, only the upper 20 bits of the voltage conversion results are accumulated. The present accumulator value can be read from the register adcVaccu (signed value; see Table 3.47). Positive conversion results increment the accumulator register; negative conversion results decrement it. The accumulator register saturates at its minimum and maximum value.

The voltage accumulator is reset to 0 under these conditions:

- On assertion of `startAdcV` (rising edge) in the FP State
- At start of the first conversion in the LP or ULP State
- Each time the result counter is reset (if the result counter is enabled)

Note: The voltage accumulator functionality can be used to calculate the mean value of the voltage.

After the last accumulation within an MRCS, the upper 16 bits of the voltage accumulator are compared to the voltage threshold `adcVTh`, which is interpreted as a signed value in this case. This comparison can be used to generate a "set interrupt" strobe for `irqStat[9]`; however, to enable the generation of the "set interrupt" strobe, bit `VThWuEna` in register `adcAcmp` must be set to 1.

The "set interrupt" strobe is generated when

- `adcVTh` is greater than 0 and `adcVaccu` is less than or equal to `adcVTh`
- `adcVTh` is lower than 0 and `adcVaccu` is greater than or equal to `adcVTh`
- `adcVTh` is equal to 0 and `adcVaccu` is equal to 0

Important: The threshold `adcVTh` is either interpreted as an unsigned or signed value depending on the operation mode (`VThSel`).

Note: The voltage comparators compare only on the MSBs of the conversion result, so it might be beneficial to use the post-correction gain functionality to shift left the results to increase the accuracy of the comparison.

3.8.3.19 Register "adcVTh" – Voltage Threshold Value

Table 3.46 Register adcVTh

Name	Address	Bits	Default	Access	Description
adcVTh[7:0]	46_{HEX}	[7:0]	00_{HEX}	RW	Voltage threshold. If `VThSel` == 0, then `adcVTh` is interpreted as an unsigned value and it is compared to the absolute value of a single voltage conversion. If `VThSel` == 1, then `adcVTh` is interpreted as a signed value and it is compared to the accumulated voltage conversion results at the end of an MRCS.
adcVTh[15:8]	47_{HEX}	[7:0]	00_{HEX}	RW	

3.8.3.20 Register "adcVaccu" – Voltage Accumulator Value

Table 3.47 Register adcVaccu

Name	Address	Bits	Default	Access	Description
adcVaccu[7:0]	10_{HEX}	[7:0]	00_{HEX}	RO	Present voltage accumulator value
adcVaccu[15:8]	11_{HEX}	[7:0]	00_{HEX}	RO	
adcVaccu[23:16]	12_{HEX}	[7:0]	00_{HEX}	RO	

3.8.3.21 Minimum and Maximum Values of Current and Voltage

For current and voltage measurements, the minimum and maximum values are determined on the upper 16 bits of the corresponding conversion results. These values can be read from registers `adcCmax`, `adcCmin`, `adcVmax`, and `adcVmin`. These registers are reset in the same manner as the corresponding accumulator registers. These values are only provided for statistical reasons and can be used to assess the accumulated current or voltage values when used for mean value calculation.

Note: As the minimum and maximum values are only determined on the 16 MSBs of the corresponding conversion results, it might be beneficial to use the post correction gain functionality to shift left the results to increase the accuracy of the comparison.

3.8.3.22 Register "adcCmax" – Maximum Current Value

Table 3.48 Register `adcCmax`

Name	Address	Bits	Default	Access	Description
adcCmax[7:0]	13_{HEX}	[7:0]	00_{HEX}	RO	Upper 16 bits of the maximum measured current value (signed value)
adcCmax[15:8]	14_{HEX}	[7:0]	80_{HEX}	RO	

3.8.3.23 Register "adcCmin" – Minimum Current Value

Table 3.49 Register `adcCmin`

Name	Address	Bits	Default	Access	Description
adcCmin[7:0]	15_{HEX}	[7:0]	FF_{HEX}	RO	Upper 16 bits of the minimum measured current value (signed value)
adcCmin[15:8]	16_{HEX}	[7:0]	$7F_{HEX}$	RO	

3.8.3.24 Register "adcVmax" – Maximum Voltage Value

Table 3.50 Register `adcVmax`

Name	Address	Bits	Default	Access	Description
adcVmax[7:0]	17_{HEX}	[7:0]	00_{HEX}	RO	Upper 16 bits of the maximum measured voltage value (signed value)
adcVmax[15:8]	18_{HEX}	[7:0]	80_{HEX}	RO	

3.8.3.25 Register "adcVmin" – Minimum Voltage Value

Table 3.51 Register `adcVmin`

Name	Address	Bits	Default	Access	Description
adcVmin[7:0]	19_{HEX}	[7:0]	FF_{HEX}	RO	Upper 16 bits of the minimum measured voltage value (signed value)
adcVmin[15:8]	$1A_{HEX}$	[7:0]	$7F_{HEX}$	RO	

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3.8.3.26 Temperature Limits

The user can define an upper (register `adcTmax`) and a lower (register `adcTmin`) limit for the external and internal temperature measurement. On each update of register `adcTdat` (see Table 3.34), the upper 8 bits are compared to the signed limit values. This can be used to generate a "set interrupt" strobe for `irqStat[10]` if the value for `adcTdat` is outside the interval [`adcTmin`; `adcTmax`] and the `TWuEna` bit in register `adcAcmp` is set to 1 (see Table 3.54).

Note: The minimum and maximum values are only compared to the 8 MSBs of the conversion result, so it might be beneficial to use the post correction gain functionality to shift left the results to increase the accuracy of the comparison.

Important: The value stored in register `adcTdat` is inverted: the value given in register `adcTmax` is the value for the lower temperature interrupt threshold and the value given in register `adcTmin` is the value for the higher temperature interrupt threshold.

3.8.3.27 Register "adcTmax" – Upper Boundary for Temperature Interval

Table 3.52 Register `adcTmax`

Name	Address	Bits	Default	Access	Description
adcTmax	$4C_{HEX}$	[7:0]	00_{HEX}	RW	Lower boundary for the temperature interval compared to the upper bits of `adcTdat`.

3.8.3.28 Register "adcTmin" – Lower Boundary for Temperature Interval

Table 3.53 Register `adcTmin`

Name	Address	Bits	Default	Access	Description
adcTmin	$4D_{HEX}$	[7:0]	00_{HEX}	RW	Upper boundary for the temperature interval compared to the upper bits of `adcTdat`.

3.8.3.29 Miscellaneous Registers

The registers defined in the next three sections provide settings that enable interrupts or control various functions related to the ADCs.

3.8.3.30 Register "adcAcmp" – ADC Function Enable Register

Table 3.54 Register adcAcmp

Name	Address	Bits	Default	Access	Description
anaGndSw	$4E_{HEX}$	[0]	0_{BIN}	RW	If set to 1, the signal `pdExtTemp` (see Figure 3.12), which is normally controlled by the PMU, is forced to 1. In this case, the transistor shown in Figure 3.12 is not conducting.
ctcvMode		[2:1]	00_{BIN}	RW	Current threshold comparator mode: 0 – The Current Threshold Comparator Mode is disabled. 1 – `adcCtcv` is decremented when the absolute current value is below the threshold and incremented otherwise. 2 – `adcCtcv` is reset when the absolute current value is below the threshold and incremented otherwise. 3 – `adcCtcv` retains its value when the absolute current value is below the threshold and incremented otherwise.
CAccuThEna		[3]	0_{BIN}	RW	If set to 1, enables the strobe to interrupt the controller when the current accumulator exceeds its threshold.
COvrEna		[4]	1_{BIN}	RW	If set to 1, enables the strobes to interrupt the controller when an over-range or overflow has been detected in the current channel.
VTOvrEna		[5]	1_{BIN}	RW	If set to 1, enables the strobes to interrupt the controller when an over-range or overflow has been detected in the voltage/temperature channel.
ctcvRstMode		[6]	0_{BIN}	RW	If set to 1, then `adcCtcv` is reset when the current result counter is reset (`adcCrcv`).
accuRstMode		[7]	0_{BIN}	RW	If set to 1, then `adcCaccu` is reset when the current result counter is reset (`adcCrcv`).
VThWuEna	$4F_{HEX}$	[0]	0_{BIN}	RW	If set to 1, enables the strobe to interrupt the controller for the voltage threshold comparator and voltage accumulator functionality.
VThSel		[1]	0_{BIN}	RW	If set to 0, the absolute value of the single voltage conversion result is compared to the threshold `adcVTh`. If set to 1, the accumulated results of all voltage conversions within an MRCS are compared to the threshold `adcVTh`.
TWuEna		[2]	0_{BIN}	RW	If set to 1, enables the strobe to interrupt the controller for checking the temperature limits.
Unused		[7:3]	$0\ 0000_{BIN}$	RO	Unused; always write as 0.

3.8.3.31 Register "adcGomd" – Reference Voltage and SDM Configuration

Table 3.55 Register adcGomd

Name	Address	Bits	Default	Access	Description
vrefSel	50_{HEX}	[1:0]	00_{BIN}	RW	Selection of the voltage reference: 0: vbgh (high precision bandgap) 1: vbgl (low power bandgap) 2: vcm (common mode voltage) 3: External reference voltage
sdmChopClkDiv		[3:2]	00_{BIN}	RW	Clock divider value for the chop clock related to the SDM clock. See equation (5) in section 3.8.1.1 for the FP State and equation (8) in section 3.8.1.2 for the LP/ULP State.
sdmSetup		[7:4]	0001_{BIN}	RW	Configuration of the initial setup procedure: 0: Execute 4 SDM clock cycles 1: Execute 8 SDM clock cycles … 7: Execute 512 SDM clock cycles 8-15: Execute 1024 SDM clock cycles

3.8.3.32 Register "adcSamp" – Oversampling and Filter Configuration

Table 3.56 Register adcSamp

Name	Address	Bits	Default	Access	Description
osr	51_{HEX}	[1:0]	00_{BIN}	RW	Oversampling rate: 0: 256x oversampling 1: 128x oversampling 2: 64x oversampling 3: 32x oversampling
Unused		[2]	0_{BIN}	RO	Unused; always write as 0.
avgFiltCfg		[4:3]	00_{BIN}	RW	Configuration of post filter (averaging filter) : 0-1: No averaging 2: 2-stage averaging filter 3: 3-stage averaging filter
chopPause		[5]	0_{BIN}	RW	Length of pause in chopping mode: 0: 8 SDM clock cycles 1: 16 SDM clock cycles
Unused		[7:6]	00_{BIN}	RO	Unused; always write as 0.

3.8.4 ADC Control and Conversion Timing

In the FP State, the ADC unit is running with the 4MHz clock derived from the HP oscillator. Its operation can be fully controlled by the external microcontroller via register settings. In the LP or ULP State, the ADC unit is running with the 125 kHz clock from the LP oscillator. Basic configurations for the ADC unit are taken from the register file; however, its operation is fully controlled by the PMU.

3.8.4.1 ADC Operation in the FP State

Before any of the ADCs can be used in the FP State, they must be powered up by setting the `pwrAdcI` bit for the current ADC and/or the `pwrAdcV` bit for the voltage/temperature ADC in the `pwrCfgFp` register to 1 (see Table 3.18). These bits can be kept set to 1 when entering one of the power-down states as the PMU takes over the control of the power signals.

The user can select which kind of operation will be performed by the ADCs and can control the input multiplexers shown in Figure 3.12 by setting the field `adcMode` in the `adcCtrl` register appropriately (see Table 3.58).

The following settings are possible:

Table 3.57 adcMode Settings

adcMode	Current ADC Configuration	Voltage / Temperature ADC Configuration
0	Current	Voltage
	INP/INN	Divided VBAT/VSSA
1	Current	External temperature
	INP/INN	VDDA/NTH and NTH/NTL
2	Current	Internal temperature
	INP/INN	VPTAT/VREF
3	Offset Calibration Mode; shortened inputs	
	VCM/VCM	VCM/VCM
4	Gain Calibration Mode @ maximum (positive) input	
	VREF / VSSA [1)]	VREF/VSSA
5	Gain Calibration Mode @ minimum (negative) input	
	VSSA / VREF [1)]	VSSA / VREF
6	1 mV internal test voltage	Voltage
	1 mV/VSSA	Divided VBAT/VSSA
7	Test Mode; each multiplexer is individually controlled by the following:	
	`cSel` field in `adcChan` register (Table 3.59)	`vtSel` field in `adcChan` register

1) The two gain calibration modes cause an ADC over-range error in the current ADC as the minimum gain of PGA2 is 4. Therefore these modes are not usable for the current ADC.

After setting the desired mode of operation, the user must start the conversion by setting the `startAdcC` bit in the `adcCtrl` register (see Table 3.58) for the current channel and/or the `startAdcV` bit for the voltage/ temperature channel to 1. After an initial setup phase, measurement results are stored in the corresponding result registers. By controlling the `startAdc` bits, the user is able to generate an individual conversion sequence (ADC operation stops after one conversion sequence has finished) or continuous conversion (ADC operation continues after one conversion sequence has finished).

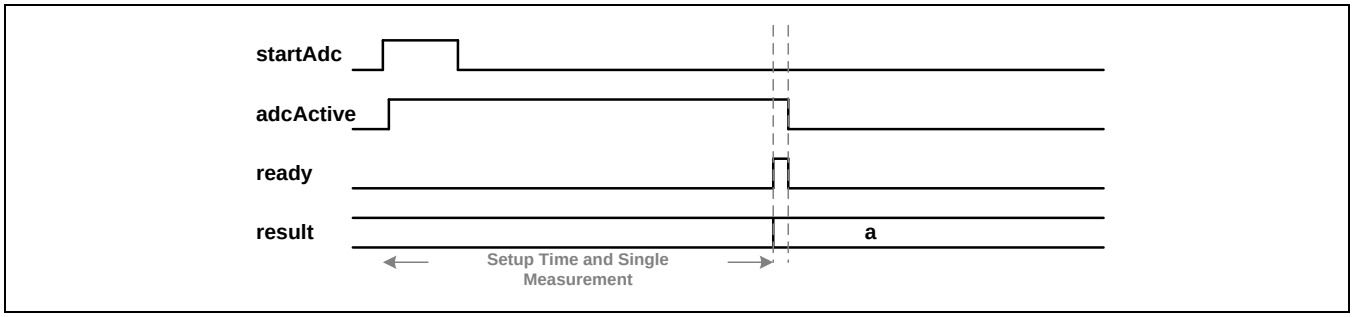
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A conversion sequence is defined as a series of several measurements. The number of measurements to be performed is controlled by the result counter functionality, so it is possible to have multiple measurements per conversion sequence (MRCS) or just a single measurement (SRCS). At the end of one conversion sequence, the "set interrupt" strobe for the corresponding conversion interrupt ready status bit (`irqStat[7:5]`) is generated. Although this strobe is only generated after the last measurement within an MRCS, each measurement in the MRCS is used for accumulation and minimum/maximum determination.

Note: The MRCS functionality is only available for current and voltage measurements, not for temperature measurements.

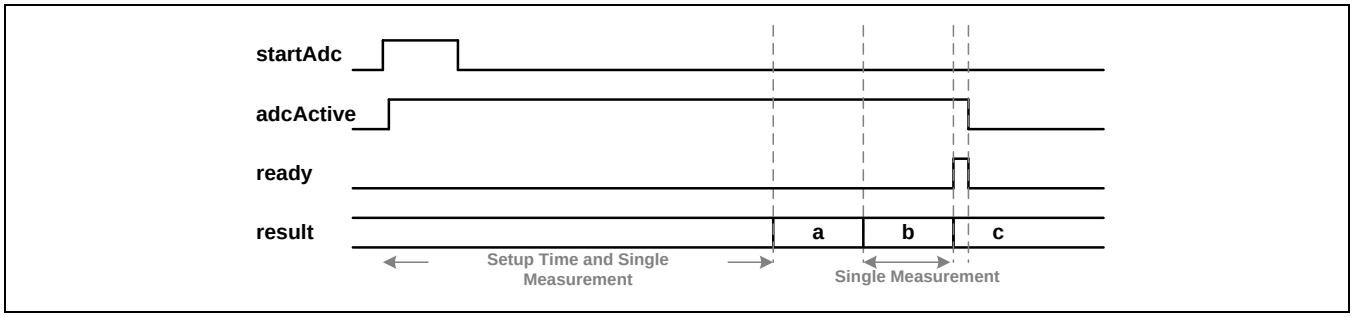
To perform an individual conversion sequence for a SRCS or MRCS, the user must generate a strobe signal on the corresponding `startAdc` bit by setting the `startAdc` bit to 1 (rising edge) first and then to 0 (falling edge). The rising edge of `startAdc` signals the ADC to start the conversion. On this start signal, the corresponding `adcActive` flag is set to 1, which can be read from bits 4 and 5 in the SSW (see section 3.1.1). When the conversion sequence has finished, the corresponding ready signal is generated. At that time, the internal logic evaluates the status of the `startAdc` bit again. If it was cleared already as required for an individual conversion sequence, the ADC stops its operation and clears the `adcActive` flag. This behavior is shown in Figure 3.22 and Figure 3.23.

Figure 3.22 Individual SRCS



Note that the ADC stops since `startAdc` is low at the end of the conversion sequence for the individual SRCS.

Figure 3.23 Individual MRCS (Example for Result Counter of 3)

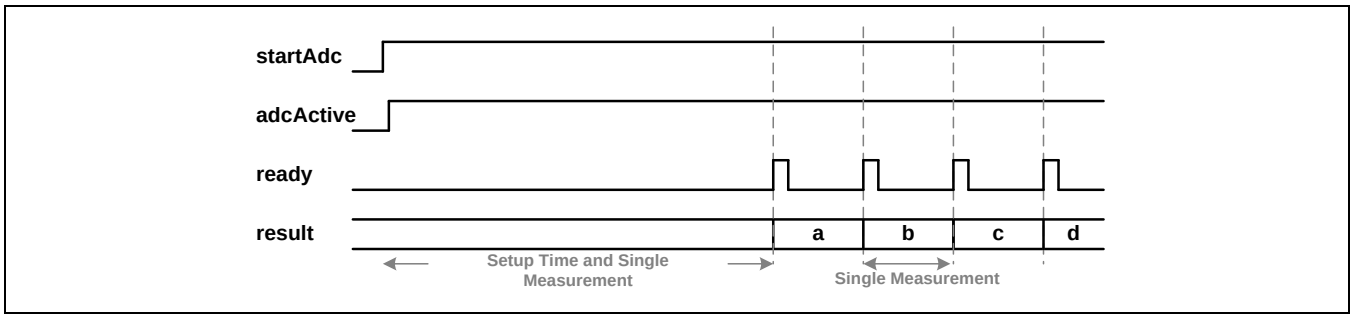


Note that the ADC stops since `startAdc` is low at the end of the conversion sequence for an individual MRCS.

Important: The ready strobe shown in Figure 3.22 and Figure 3.23 is used to set the interrupt status bit, but the interrupt status bit remains set until it is cleared by the user's software.

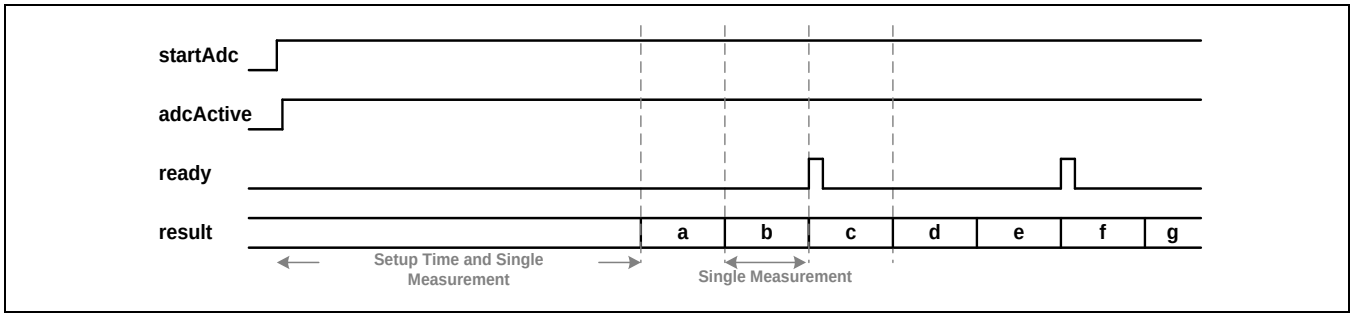
To perform a continuous conversion sequence for SRCS or MRCS, the user must set the corresponding `startAdc` bit to 1 (rising edge). The rising edge of `startAdc` signals the ADC to start the conversion. On this start signal, the corresponding `adcActive` flag is set to 1, which can be read from bits 4 and 5 in the SSW. When one conversion sequence has finished, the corresponding ready signal is generated. At that time, the internal logic evaluates the status of the `startAdc` bit again. As the `startAdc` bit is still 1, the ADC continues its operation but without the need for the setup time. This behavior is shown in Figure 3.24 and Figure 3.25.

Figure 3.24 Continuous SRCS



Note that the ADC continues since `startAdc` is high at the end of the conversion sequence for a continuous SRCS.

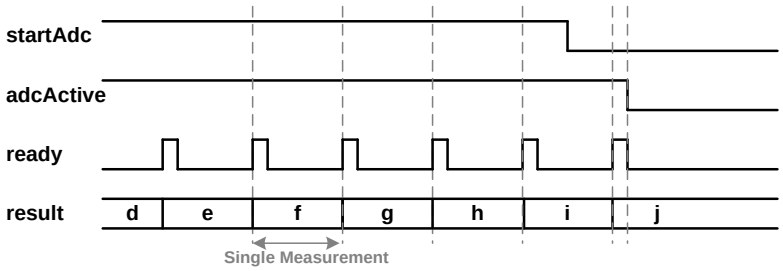
Figure 3.25 Continuous MRCS (Example for Result Counter of 3)



Note that the ADC continues since `startAdc` is high at the end of the conversion sequence for a continuous MRCS.

When a continuous conversion sequence is performed that will be stopped after the present active conversion sequence has completed, the user only needs to clear the `startAdc` bit of the channel that will be stopped. Then the user can either wait for the next interrupt, which will be set by the last ready strobe, or check the corresponding `adcActive` bit in the SSW.

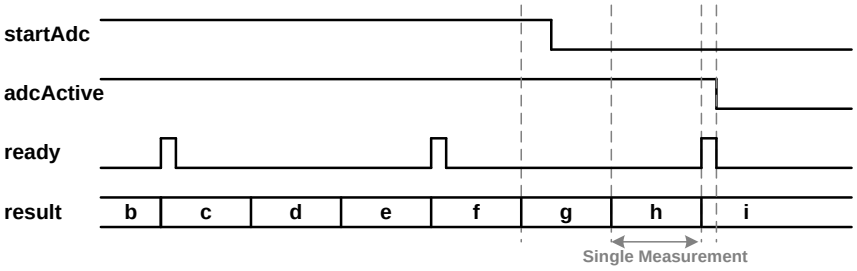
Figure 3.26 Stopping Continuous SRCS



Note that the ADC stops since `startAdc` is low at the end of the conversion sequence for a continuous SRCS.

When a conversion sequence is performed that will be interrupted (stopped immediately), the user must clear the `startAdc` bit of the channel that will be stopped (when set) and must set the `stopAdc` bit in the `adcCtrl` register to 1. In the ADC unit, the `stopAdc` bit is only evaluated when the `startAdc` bit of a channel is low and the corresponding `adcActive` bit is high.

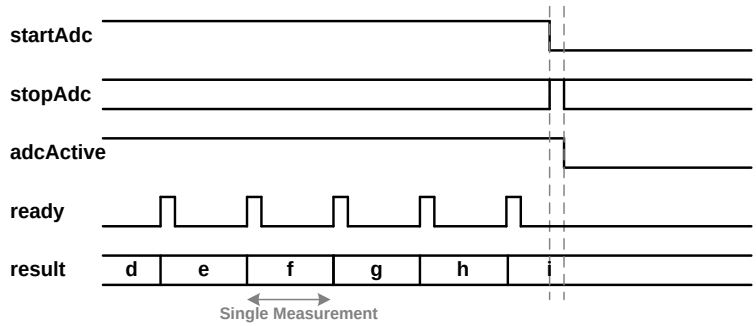
Figure 3.27 Stopping Continuous MRCS (Example for Result Counter of 3)



Note that the ADC stops since `startAdc` is low at the end of the conversion sequence for a continuous MRCS; otherwise the `stopAdc` bit is ignored. Therefore there is only one `stopAdc` bit that is used for both channels. This allows the user to stop both channels by clearing both `startAdc` bits when setting the `stopAdc` bit or to stop only one channel by keeping one `startAdc` bit high.

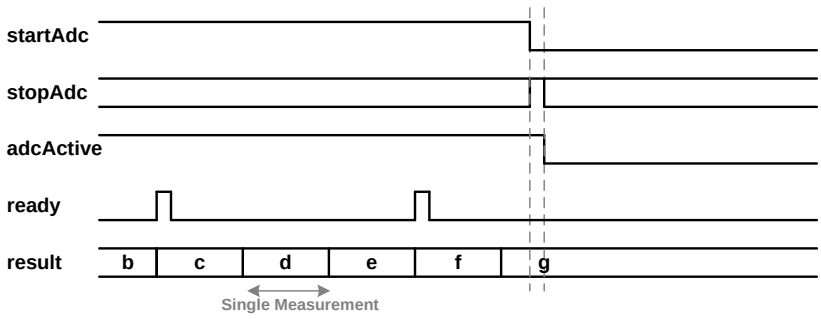
The signal behavior for interrupting a channel is shown in Figure 3.28 and Figure 3.29.

Figure 3.28 Interrupting a Continuous SRCS



Note that the ADC immediately stops since `startAdc` is low and `stopAdc` is high.

Figure 3.29 Interrupting a Continuous MRCS (Example for Result Counter of 3)



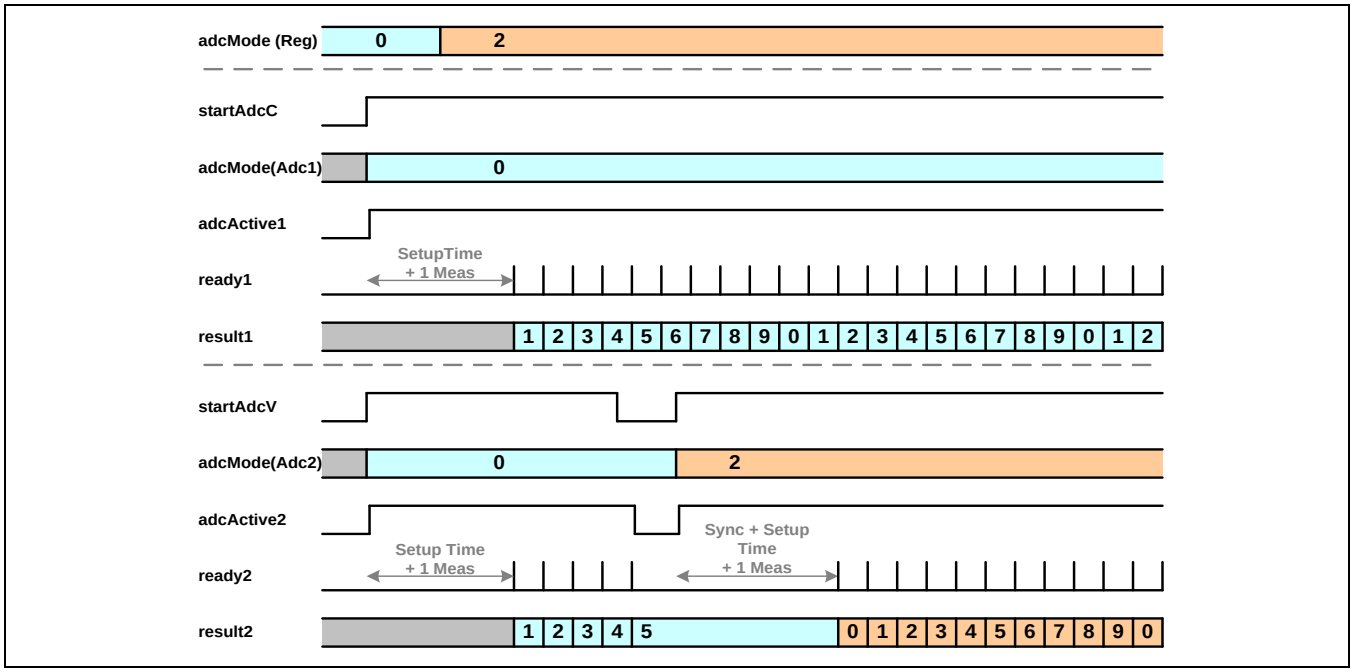
Note that the ADC immediately stops since `startAdc` is low and `stopAdc` is high.

Important: The `stopAdc` bit is only evaluated when `startAdc` bit is low.

Note: The interrupt sequence shown in Figure 3.28 and Figure 3.29 is also performed by the PMU on transition from the FP State to any power-down state as well as on transition from any power-down state to the FP State. This allows the user to keep the `startAdc` bits set on transition to any power-down state. After wake-up, the ADCs continue the operation they performed before going to power-down.

Most of the register settings that influence both ADC channels (e.g., oversampling rate) can only be changed when both ADC channels are inactive. As explained above, this is not true for the `stopAdc` bit. The `adcMode` field can also be changed while any ADC channel is active. This is useful for continuing with current measurements in the first ADC channel while changing the second ADC channel from voltage to temperature measurements (as an example). On the rising edge of its `startAdc` bit, each ADC channel stores internally the mode it is configured for and keeps this setting until the next rising edge of its `startAdc` bit. When one channel is reconfigured while the other one is active, this channel does not start immediately after being re-enabled but synchronizes to the active channel so that the results are generated at the same time. See Figure 3.30.

Figure 3.30 Signal Behavior of adcMode



3.8.4.2 Register "adcCtrl" – ADC Control Register

Table 3.58 Register `adcCtrl`

Name	Address	Bits	Default	Access	Description
startAdcC	56$_{HEX}$	[0]	0$_{BIN}$	RW	Start signal for the current ADC; used in the FP State, ignored in other states.
startAdcV		[1]	0$_{BIN}$	RW	Start signal for the voltage/temperature ADC; used in the FP State, ignored in other states.
stopAdc		[2]	0$_{BIN}$	RW	Stop signal for both ADCs; used in the FP State, ignored in other states.
adcMode		[5:3]	000$_{BIN}$	RW	ADC multiplexer configuration; used in the FP State, ignored in other states; for settings 0, 1, 2, and 6, the first value is applied to the current ADC, the second to the voltage/temperature ADC. (See section 3.8.4.1 for more details.) 0 – Measure current and voltage 1 – Measure current and external temperature 2 – Measure current and internal temperature 3 – Offset calibration 4 – Gain calibration @ maximum (positive) input 5 – Gain calibration @ minimum (negative) input 6 – Internal test voltage and voltage 7 – Test Mode (control multiplexer via the `adcChan` register's `cSel` and `vtSel` fields)
chopEna		[6]	0$_{BIN}$	RW	If set to 1, Chopping Mode is enabled.
Unused		[7]	0$_{BIN}$	RO	Unused; always write as 0.

3.8.4.3 ADC Operation in LP/ULP State

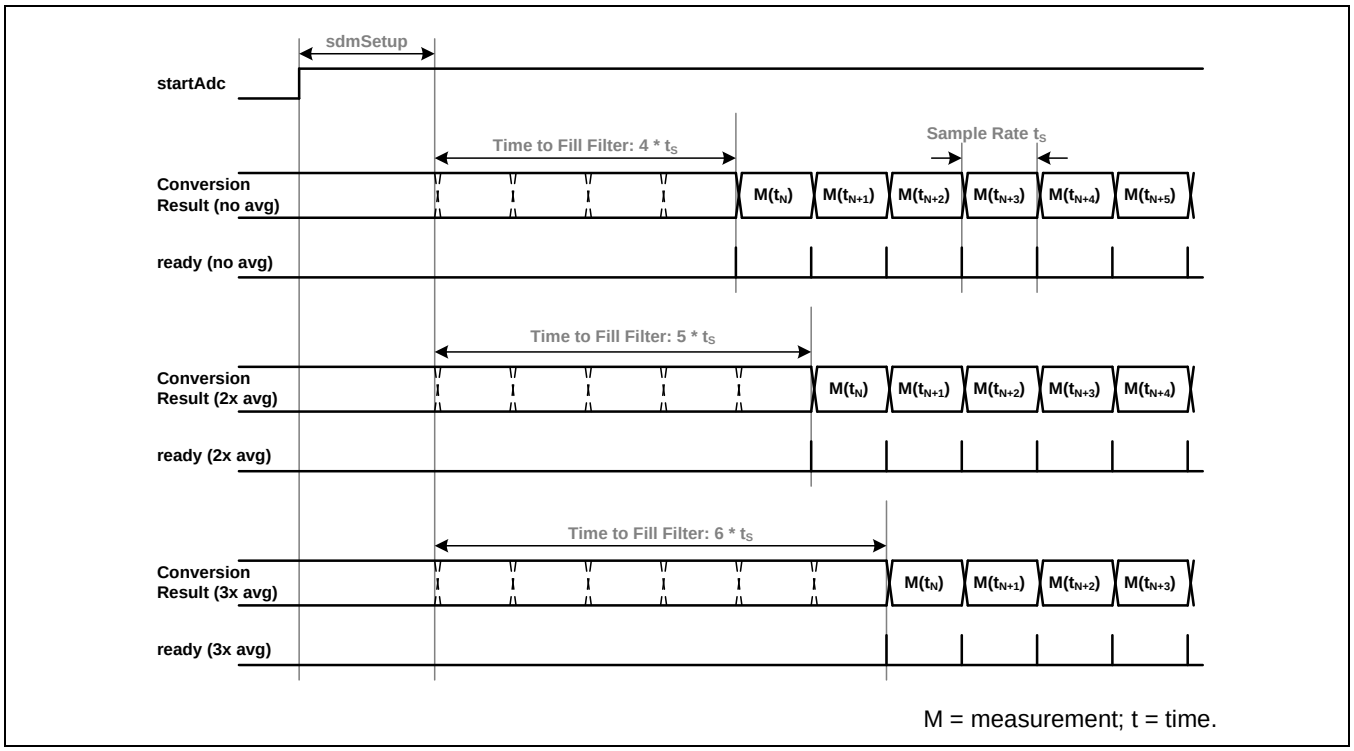
During the LP or ULP State, the ADCs are fully controlled by the PMU depending on the settings of register `pwrCfgLp` (see Table 3.19). The PMU overrides the settings of the `startAdc` bits, the `stopAdc` bit, and `adcMode` field. The settings of `pwrAdcI` and `pwrAdcV` are also ignored until the system wakes up. While no further settings are required for the continuous measurement set-ups, the user can independently configure how many current and/or voltage measurements happen within a single measurement window. For current (the green and orange boxes In Figure 3.6 to Figure 3.9), the number of current measurements in each window is configured by the setting of `adcCrcl` (see Table 3.37). For voltage (the orange boxes shown in Figure 3.6 to Figure 3.9), the number of voltage measurements in each window is configured by the setting of `adcVrcl` (see Table 3.39).There is always only one temperature measurement as the last measurement made by the voltage/temperature ADC in a sample period.

Important: If an interrupt wakes up the system before the end of a measurement window, the conversion sequence is interrupted and less than the configured number of measurements will have been completed. This can be checked by the registers `adcCrcv` (see Table 3.38) and `adcVrcv` (see Table 3.40).

3.8.4.4 ADC Conversion Timing

The complete conversion process is controlled by an internal state machine that guarantees that only valid measurement results are used. The base for all ADC timings is the SDM clock, which is generated from the 4MHz clock in FP State or from the 125kHz clock in LP and ULP State. After the ADC measurement has been started (rising edge of `startAdc`), the state machine always introduces a configurable number of SDM clock cycles (field `sdmSetup` in register `adcGomd`; see Table 3.55) to allow the analog part of the SDM to settle. After this delay, the incoming bit streams are used to fill the sinc^4 decimation filter. This lasts 4 times the sample rate, which is configured by the oversampling rate (the `osr` field in register `adcSamp`; see Table 3.56). Then the first valid result value comes from the decimation filter.

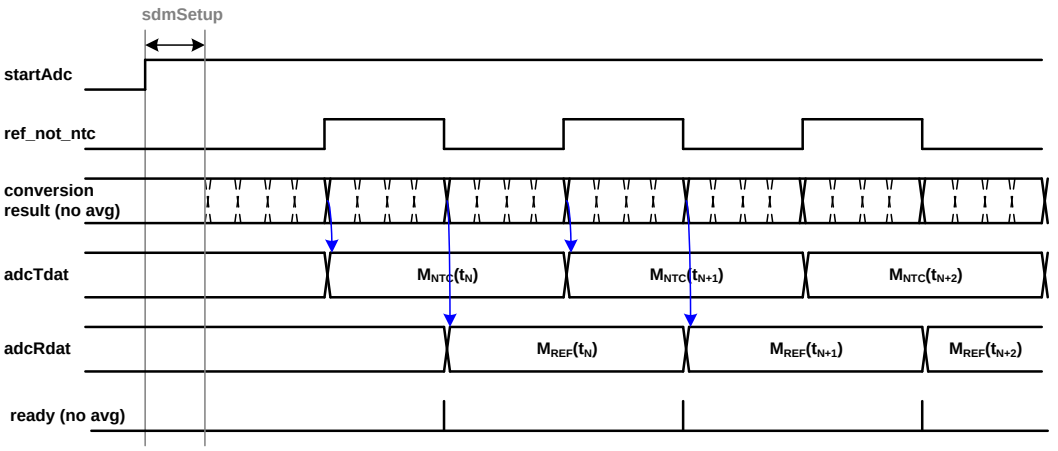
Figure 3.31 Timing for Current, Voltage, and Internal Temperature Measurements without Chopping for Different Configurations of the Average Filter



For current, voltage, or internal temperature measurement without chopping, when only one input source must be measured, this is the first valid value. The time when the first valid result is present also depends on the configuration of the average filter (the `avgFiltCfg` field in register `adcSamp`). If no averaging is used, the first valid value is also the first valid result stored in `adcCdat`, `adcVdat`, or `adcTdat`. For the 2-stage or 3-stage average filter, respectively, two or three valid values are needed to calculate a valid result. This adds an additional delay, respectively, of 1 or 2 times the sample rate.

For external temperature measurement without chopping, two input sources must be measured: the voltage drop over the reference resistor (the result is stored in register `adcRdat`) and the voltage drop over the NTC resistor (result stored in register `adcTdat`). The `sdmSetup` time is only introduced at the beginning of the conversion sequence (the rising edge of `startAdc`). Each single measurement of one of the two values needs 4 times the sample rate when averaging is disabled, or respectively, 5 or 6 times the sample rate when using the 2-stage or 3-stage average filter. This also means that a complete pair of values used to calculate one external temperature value needs 8 (10 or 12 for averaging) times the sample rate because for each value, the pipeline of the sinc^4 decimation filter must be filled first.

Figure 3.32 Timing for External Temperature Measurements without Chopping when No Average Filter is Enabled



M = measurement; t = time.

Note that using an average filter will lead, respectively, to 5 and 6 conversion results during each high and low phase of ref_not_ntc.

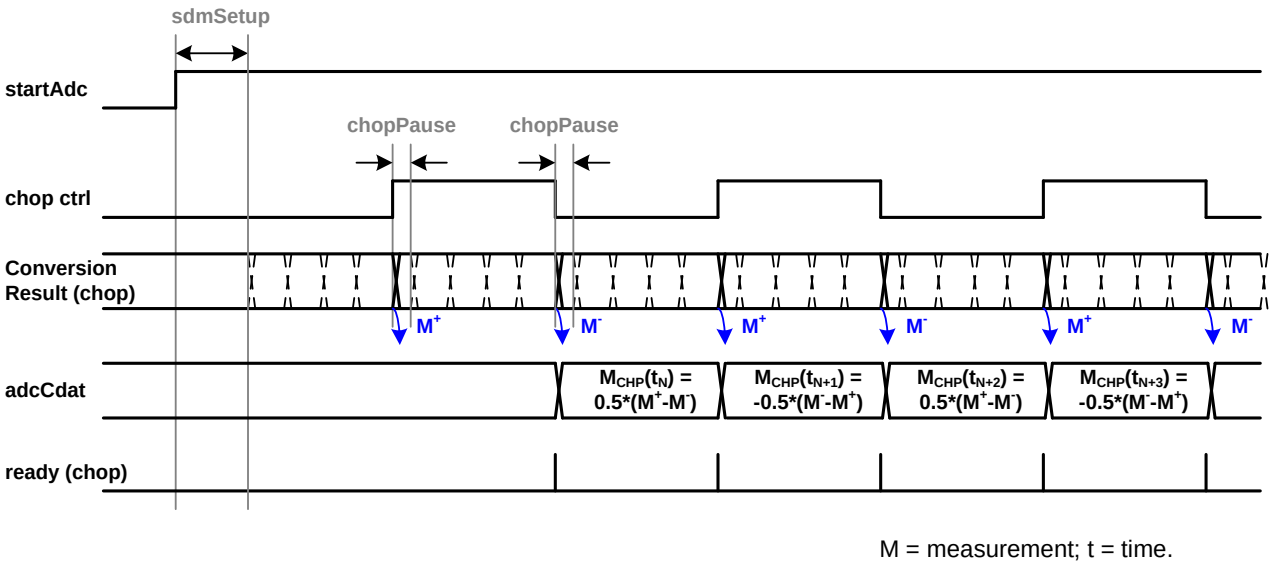
The timings shown in the previous two figures are without chopping, which means that the differential input signal is always applied in the same manner to the analog SD-ADC. Although this kind of measurement is fast (one result value after each sample time), it has the drawback that it also converts any offset present in the analog blocks. This would lead to less accurate measurement results. To overcome this, chopping can be enabled (bit `chopEna` in register `adcCtrl`; see Table 3.58). When chopping is enabled, the differential input signal is directly applied to the analog SD-ADC the first time and inverted the second time. Taking this into account in the digital part removes the offset applied by the ADC itself:

$$\text{data} = \frac{(V_{in} + \text{offset}) + (-1) * (-V_{in} + \text{offset})}{2} = V_{in} \quad (15)$$

For current, voltage, or internal temperature measurement with Chopping Mode enabled (chopEna set to 1), this leads to a timing similar to the external temperature measurement without chopping and averaging since two values are measured: the normal input and the inverted input. Each single measurement of one of the two values needs 4 times the sample rate as no averaging of the single measurement is performed. Instead, the average filter is automatically configured as a 2-stage average filter to calculate the formula above. The second difference is that a small pause (chopping pause) is introduced each time the chop control signal changes to allow the analog blocks to settle due to the input change. This is possible since the chopEna bit influences both ADC paths. The length of the chop pause is either 8 or 16 SDM clock cycles, which can be configured using the chopPause bit in register adcSamp.

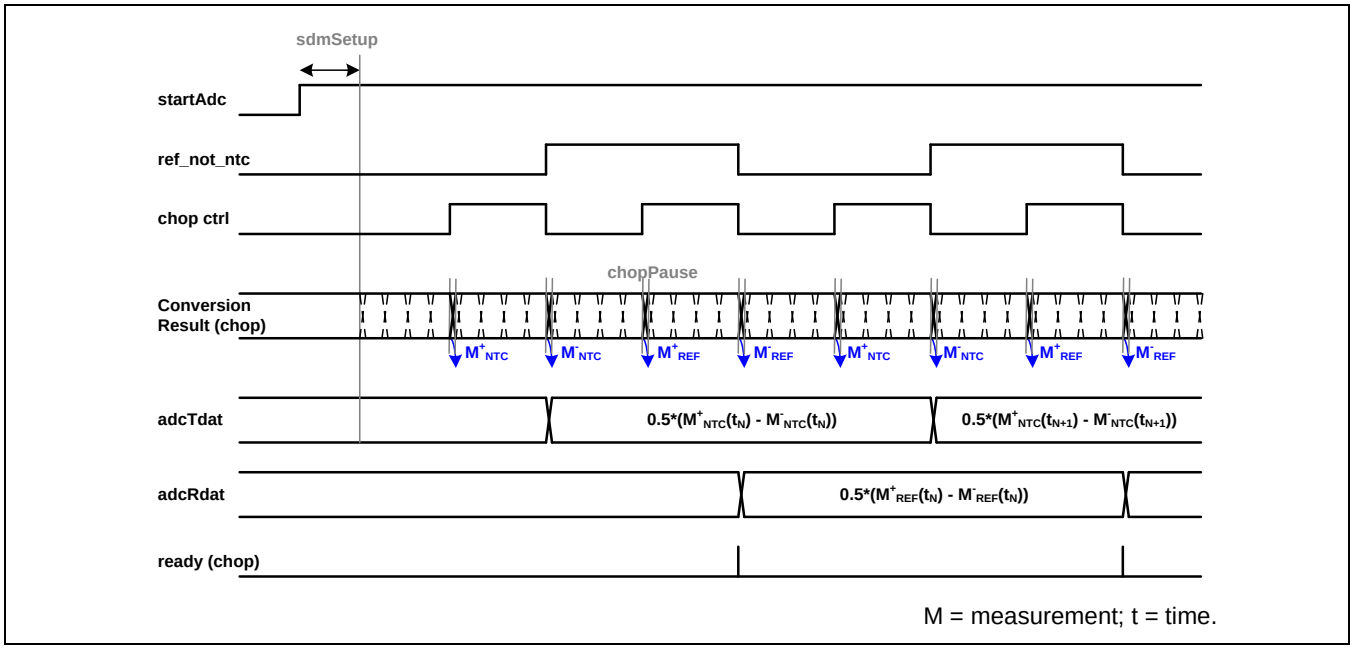
Figure 3.33 Timing for Current, Voltage, and Internal Temperature Measurements using Chopping

Example shown is for current measurement:



For external temperature measurement using chopping, two different input sources must be measured twice, non-inverted and inverted, which leads to four values to be measured to determine a result. To keep both ADC paths aligned, the chopPause is introduced for each measured value.

Figure 3.34 Timing for External Temperature Measurements using Chopping



Important: The timings only show the principle. Additional small delays such as pipeline delays are not included.

3.8.5 Diagnostic Features

3.8.5.1 ADC Analog Multiplexer Control for Diagnosis and Test

In the FP State, the three multiplexers shown in Figure 3.12 can be directly controlled via the register `adcChan` (see Table 3.59) when the `adcMode` field in register `adcCtrl` is set to 7 (see Table 3.58). For other settings of `adcMode`, the settings of register `adcChan` are ignored and both multiplexers for input selection are controlled either by the `adcMode` field in the FP State or by the PMU in LP or ULP State.

The `vtSel` field in register `adcChan` is used to select the input sources of the voltage/temperature ADC. The `cSel` field in register `adcChan` is used to select the input sources of the current ADC.

Important: the reference voltage (non-inverted as well as inverted) cannot be measured by the current ADC as the minimum gain of PGA-2 is 4, which causes an ADC over-range error.

For some settings of `adcMode`, `cSel`, and `vtSel`, the reference voltage is applied to the ADCs. The user can select the source of the reference voltage with the `vrefSel` field in register `adcGomd` (see Table 3.55). As can be seen from Figure 3.12, the user's software can connect internal current sources to the input wires of the INP and INN pins as well as to the input wires of the NTH and NTL pins. To enable the different current sources for the four input wires, the corresponding enable bit in register `currentSrcEna` must be set to 1 (see Table 3.62).

Important Warning: Do not enable both current sources on the same input at the same time.

Important: The current sources can be enabled independent of the `adcMode`.

3.8.5.2 Register "adcChan" – Analog Multiplexer Configuration

Table 3.59 Register adcChan

<table>
<tr><th>Name</th><th>Address</th><th>Bits</th><th>Default</th><th>Access</th><th>Description</th></tr>
<tr><td>vtSel</td><td rowspan="3">D0$_{HEX}$</td><td>[2:0]</td><td>000$_{BIN}$</td><td>RW</td><td>When adcMode == 7, this field selects the differential sources for the voltage/temperature ADC:
<table>
<tr><th>vtSel</th><th>inp</th><th>inn</th></tr>
<tr><td>000$_{BIN}$</td><td>VDDA</td><td>NTH</td></tr>
<tr><td>001$_{BIN}$</td><td>NTL</td><td>NTH</td></tr>
<tr><td>010$_{BIN}$</td><td>VPTAT</td><td>VBGH (i.e., V_{REF})</td></tr>
<tr><td>011$_{BIN}$</td><td>VBATP</td><td>VBATN</td></tr>
<tr><td>100$_{BIN}$</td><td>VBGH (i.e., V_{REF})</td><td>VSSA</td></tr>
<tr><td>101$_{BIN}$</td><td>VBGL (i.e., V_{REFLP})</td><td>VSSA</td></tr>
<tr><td>110$_{BIN}$</td><td>VCM</td><td>VCM</td></tr>
<tr><td>111$_{BIN}$</td><td>High impedance</td><td>High impedance</td></tr>
</table></td></tr>
<tr><td>cSel</td><td>[5:3]</td><td>000$_{BIN}$</td><td>RW</td><td>When adcMode == 7, this field selects the differential sources for the current ADC:
<table>
<tr><td>000$_{BIN}$</td><td>INP</td><td>INN</td></tr>
<tr><td>001$_{BIN}$</td><td>INP</td><td>INN</td></tr>
<tr><td>010$_{BIN}$</td><td>INP</td><td>INN</td></tr>
<tr><td>011$_{BIN}$</td><td>INP</td><td>INN</td></tr>
<tr><td>100$_{BIN}$</td><td>1 mV</td><td>VSSA</td></tr>
<tr><td>101$_{BIN}$</td><td colspan="2">Unused</td></tr>
<tr><td>110$_{BIN}$</td><td colspan="2">Unused</td></tr>
<tr><td>111$_{BIN}$</td><td>VCM</td><td>VCM</td></tr>
</table></td></tr>
<tr><td>Unused</td><td>[6]</td><td>0$_{BIN}$</td><td>RW</td><td>Unused; always write as 0.</td></tr>
<tr><td>Unused</td><td>[7]</td><td>0$_{BIN}$</td><td>RW</td><td>Unused; always write as 0.</td></tr>
</table>

3.8.6 Digital Features

3.8.6.1 Built-in Self-Test (BIST)

The digital ADC BIST feature allows the user to test the digital logic of the ADC data path. The BIST feature is enabled by setting the bistEna bit in register adcDiag to 1 (see Table 3.61). When the BIST feature is enabled, the same programmable bit stream is applied to both inputs of the decimation filter instead of the outputs from the noise cancellation filters. The ADCs must also be set into operation as during normal operation.

The bit stream to be applied to the decimation filter is programmed to the lower 30 bits of register adcCaccTh (see Table 3.44). These 30 bits function as a shift-rotate register as shown in Figure 3.35, and the output of the lowest bit is used as the bit stream for the BIST.

Important: Since register adcCaccTh is used for the BIST, the current accumulator threshold functionality cannot be used.

Figure 3.35 Usage of Register adcCaccTh for the Digital ADC BIST

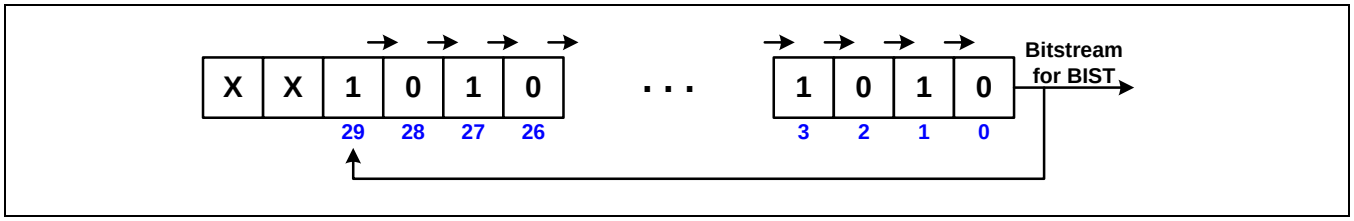


Table 3.60 shows four example bit streams as well as the expected output stored in the corresponding data registers `adcCdat`, `adcVdat`, `adcTdat`, and/or `adcRdat` if enabled. In these examples, the offset correction value (e.g., register `adcCoff`) is set to 0, the gain correction value (e.g., register `adcCgan`) is set to 1.0, and the post correction gain factor (e.g., bit field `curPoCoGain` [1:0] in register `adcPoCoGain`) is set to gain factor 1 (bit field set to 00_{BIN}) and then to gain factor 2 (bit field set to 01_{BIN}).

Table 3.60 Example Results of BIST

1/0 Bit Ratio	Bit Stream	Result Data (xPoCoGain = Gain Factor 1, Bit Field = 00_{BIN})	Result Data (xPoCoGain = Gain Factor 2, Bit Field = 01_{BIN})
1/6	100000_100000_100000_100000_100000 20820820_{HEX}	$AAAAAA_{HEX}$	800000_{HEX} (negative over-range)
5/6	111110_111110_111110_111110_111110 $3EFBEFBE_{HEX}$	555555_{HEX}	$7FFFFF_{HEX}$ (positive over-range)
2/5	10010_10010_10010_10010_10010_10010 $25294A52_{HEX}$	$E66666_{HEX}$	$CCCCCC_{HEX}$
3/5	10110_10110_10110_10110_10110_10110 $2D6B5AD6_{HEX}$	199999_{HEX}	333332_{HEX}

3.8.6.2 Decimation Filter Output Test

The decimation filter output test allows the user to observe the outputs of both decimation filters. This feature is enabled by setting bit `rawEna` in register `adcDiag` to 1. When this feature is enabled, the 32-bit output value of the decimation filter for the current ADC is stored in registers `adcCmax` (MSBs; see Table 3.48) and `adcCmin` (LSBs; see Table 3.49) and the 32-bit output value of the decimation filter for the voltage/temperature ADC is stored in registers `adcVmax` (MSBs; see Table 3.50) and `adcVmin` (LSBs; see Table 3.51). The ADCs must also be set into operation as during normal operation.

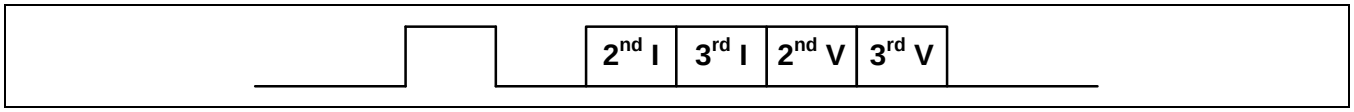
Note: When this feature is enabled, all normal ADC operations described in the previous sections function as described except the minimum and maximum functionality for the current and voltage values because the registers are used for this test function.

Note: This feature can be combined with the digital ADC BIST feature.

3.8.6.3 ADC Interface Test

The ADC interface test allows the user to observe the incoming 2nd and 3rd order bit streams from both analog parts of the SD-ADCs. This feature is enabled by setting bit `adcIfTestEna` in register `adcDiag` to 1. The digital part of the ADC unit must be enabled as for normal operation as it generates the correct sample strobe for the test logic. This function is only available in the FP State as it runs on the 20MHz clock from the high-precision oscillator. All sampled values (4 bits) are shifted out of the STO pad. To enable the user to synchronize on the sampled data, a 1 and a 0 are shifted out before each 4-bit value as shown in Figure 3.36.

Figure 3.36 Bit Stream of ADC Interface Test at STO Pad



Note: This feature can be combined with the digital ADC BIST feature and with the decimation filter output test.

3.8.6.4 Register "adcDiag" – Enable Register for Test and Diagnosis Features

Table 3.61 Register `adcDiag`

Name	Address	Bits	Default	Access	Description
bistEna	$D1_{HEX}$	[0]	0_{BIN}	RW	If set to 1, enables BIST.
rawEna		[1]	0_{BIN}	RW	If set to 1, enables the decimation filter output test (ADC raw data test).
adcIfTestEna		[2]	0_{BIN}	RW	If set to 1, enables the serial ADC test.
Unused		[5:3]	000_{BIN}	RW	Unused; always write as 0.
stopClkChop		[6]	0_{BIN}	RW	Disable signal for the global chopper (overall analog and digital part chopping). Keep this bit '0' in application if chopping is required.
clkChopEna		[7]	1_{BIN}	RW	Enable signal for internal chopper of the sigma-delta modulator input stage. Keep this bit '0' in application.

3.8.6.5 Register "currentSrcEna" – Enable Register for Current Source

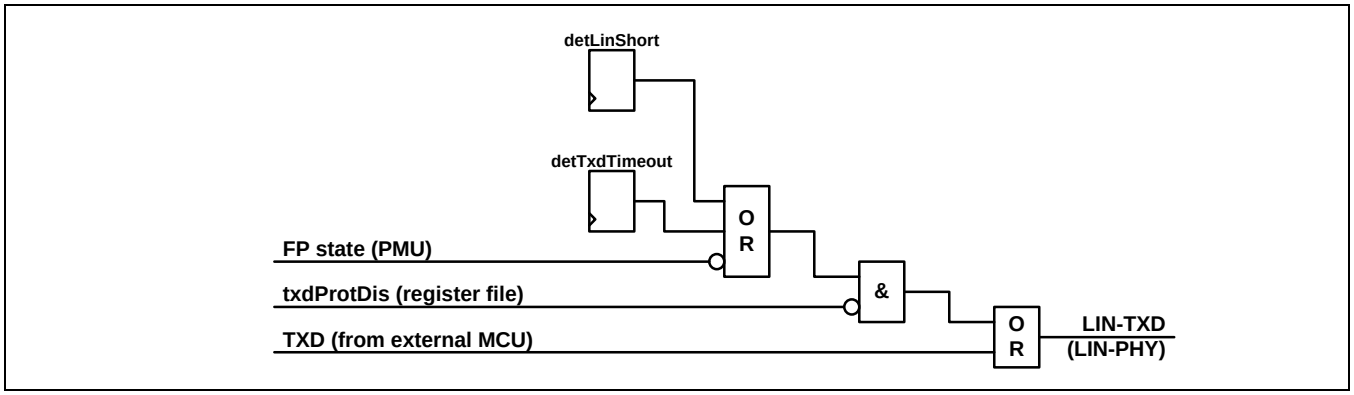
Table 3.62 Register `currentSrcEna`

Name	Address	Bits	Default	Access	Description
inampInpSrcEna	$D2_{HEX}$	[0]	0_{BIN}	RW	Enable 50µA current source to INP.
Unused		[1]	0_{BIN}	RW	Unused; always write as 0.
inampInnSrcEna		[2]	0_{BIN}	RW	Enable 50µA current source to INN.
Unused		[3]	0_{BIN}	RW	Unused; always write as 0.
psrcEnVbat		[4]	0_{BIN}	RW	Enable 50µA current source on NTH.
psinkEnVbat		[5]	0_{BIN}	RW	Enable -50µA current source on NTH.
nsrcEnVbat		[6]	0_{BIN}	RW	Enable 50µA current source on NTL.
nsinkEnVbat		[7]	0_{BIN}	RW	Enable -50µA current source on NTL.

3.9 SBC LIN Support Logic (for ZSSC1750 only)

The ZSSC1750 LIN support logic handles two error conditions: a LIN dominant timeout on the TXD pin and a short to VBAT on the LIN pin. Figure 3.37 illustrates the error protection logic discussed in the next sections.

Figure 3.37 Protection Logic of the LIN TXD Line



3.9.1 LIN Wakeup Detection

A LIN master generates a LIN wakeup frame by driving a dominant value of 0 of at least 250µs on the LIN bus. The standard requires that a LIN slave must recognize a LIN wakeup when the LIN bus is low for more than 150µs.

There is a 6-bit counter running with the 125kHz LP clock implemented in the ZSSC1750 to support the LIN wakeup detection. When the function is disabled (`irqEn[4]` is set to 0), the counter is set to 20_{HEX} and no interrupt can occur. When the function is enabled (`irqEn[4]` is set to 1), the LIN RXD line is observed. When the LIN RXD line is high, the counter is set to 00_{HEX}. When the LIN RXD line becomes low, the counter is incremented in each clock cycle until it reaches the value 20_{HEX} where it stops incrementing. When the counter is equal to the programmed wakeup delay (register `linWuDelay`; see Table 3.66), a set strobe for the corresponding interrupt is generated, which causes the system to wake up.

The register `linWuDelay` has a default value of 14_{HEX}. This setting guarantees that no low level less than 150µs on the LIN RXD line causes a wakeup due to the inaccuracy of the LP oscillator.

3.9.2 TXD Timeout Detection

The digital LIN controller in the external microcontroller must ensure that it does not completely block the LIN bus due to continuously transmitting a dominant value of 0. As it is still possible that the TXD line from the external microcontroller is stuck at 0 due to a software or hardware error in the external microcontroller or a broken connection between the external microcontroller and the ZSSC1750, the LIN support logic observes the TXD line in FP State to detect if the TXD line is erroneously low. The timeout detection circuit can handle baud rates down to 1kBaud, where the maximum time that a digital LIN controller (slave device!) can transmit a low level is 9ms (start bit and 8 data bits). To overcome inaccuracies of the internal clocks, the internal logic and untrimmed LIN nodes, the timeout value is 10.24ms.

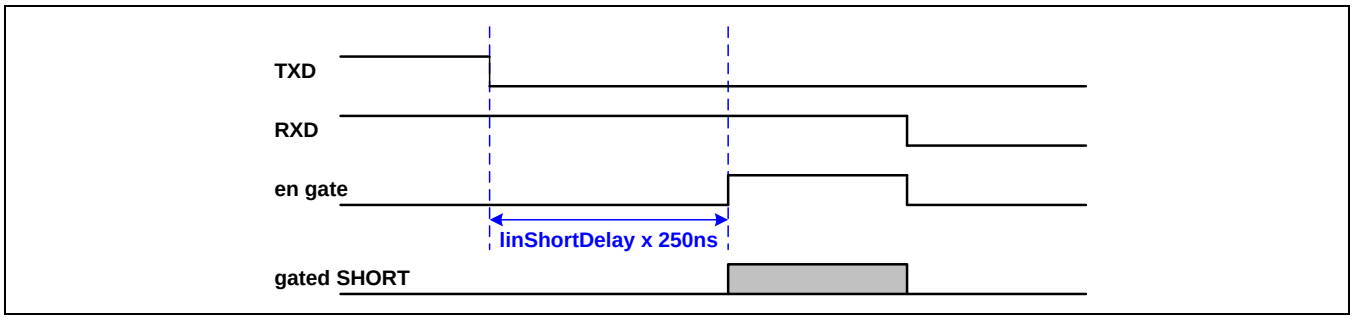
On detection of a TXD timeout, an internal flag (`detTxdTimeout` in Figure 3.37) is set to the high level, which forces the LIN TXD line to 1, and the corresponding interrupt status (`irqStat[2]`) is set. While the interrupt status bit is cleared on read access to the interrupt status register, the internal flag remains high, also keeping LIN TXD at the high level. The status of the internal flag is mirrored in `SSW[2]`. To clear this internal flag and to be able to transmit again via the LIN bus, a value of 1 must be written to bit `clrTxdTimeout` in register `linCfg` (see Table 3.64).

3.9.3 LIN Short Detection

The LIN PHY contains a function to detect a short to VBAT on the LIN bus by sensing the current through the open-drain output transistor in the LIN PHY. When the current is too high, the LIN PHY drives the SHORT signal going to the digital block to the high level (see Figure 3.38). Under normal circumstances, the LIN PHY signals a short only if a dominant value of 0 will be transmitted, but the bus remains at its recessive high level. However, high current consumption is also possible due to EMC events. To increase the safety of the system and to avoid misinterpretation, the incoming SHORT signal is gated and filtered.

First, the SHORT signal from the LIN PHY is driven through a configurable gating block inside the digital block. The gating block is configured using register `linShortDelay` (see Table 3.65). If register `linShortDelay` is set to a value not equal to 0, the TXD line going to and the RXD line coming from the LIN PHY are observed. When the TXD line becomes low while the RXD line remains high, the gating block waits for `linShortDelay` times 4MHz clock cycles before opening the gate. The gate is closed when either TXD becomes high again or RXD becomes low (see Figure 3.38). This feature is used to evaluate the SHORT signal only when a dominant value of 0 is transmitted, but the bus remains at its recessive high level as well as to eliminate the delay from the TXD line through the LIN PHY back to the RXD line.

Figure 3.38 Waveform Showing the Gating Principle for Non-zero Values of `linShortDelay`



When the register `linShortDelay` is set to 0, the gate for the SHORT signal is always open. This means that the SHORT signal is always passed through the gating block even when the TXD line is high or the RXD line is low.

The gated SHORT signal is applied to a configurable de-bouncing filter. This de-bouncing filter is configured using register `linShortFilter` (see Table 3.64), and it monitors the gated SHORT signal using the internal 4MHz clock. When the gated SHORT signal is continuously high for (`linShortFilter` + 1) clock cycles, the LIN short interrupt status bit (`irqStat[3]`) is set, enabling the user's software running on the connected external microcontroller to respond to this situation. The interrupt status bit is cleared on read access to the interrupt status register.

The software can also enable the hardware to protect the TXD line in the case of a detected short condition. When the `shortProtEna` bit in register `linCfg` (see Table 3.63) is set to 1 and a short condition is detected by the de-bouncing filter, an internal flag (`detLinShort` in Figure 3.37) is set to the high level, which forces the LIN TXD line high. The status of the internal flag is mirrored in `SSW[3]`. The internal flag remains high until it is explicitly cleared by the software by writing a value of 1 to the `clrLinShort` bit in register `linCfg`.

3.9.4 LIN Testing

The LIN TXD line protection features (TXD timeout, LIN short, LP State) might restrict the possibility of testing the LIN PHY. Therefore the protection can be disabled by setting the `txdProtDis` bit in register `linCfg` to 1 (see Figure 3.37).

Important Warning: This must never be done during normal operation. The IC will not be damaged, but communication errors will not be detected.

3.9.4.1 Register "linCfg" – LIN Configuration Register (ZSSC1750 Only)

Table 3.63 ZSSC1750 Register `linCfg`

Important: For the ZSSC1751 this register is not used and must remain as the default setting.

Name	Address	Bits	Default	Access	Description
linFastEna	$B4_{HEX}$	[0]	0_{BIN}	RW	When set to 1, the slew rate control in the LIN PHY transmitter is disabled allowing higher LIN data rates of up to 125kBaud (non-standard feature).
txdProtDis		[1]	0_{BIN}	RW	When set to 1, all protection features that force the LIN TXD line to 1 are overwritten (for test purposes only).
shortProtEna		[2]	0_{BIN}	RW	If set to 1, enables the LIN short protection.
Unused		[3]	0_{BIN}	RO	Unused; always write as 0.
clrTxdTimeout		[4]	0_{BIN}	RWS	Strobe register; write 1 to clear the detected TXD timeout flag and to release the protection of the LIN TXD line.
clrLinShort		[5]	0_{BIN}	RWS	Strobe register; write 1 to clear the detected LIN SHORT flag and to release the protection of the LIN TXD line.
Unused		[7:6]	00_{BIN}	RO	Unused; always write as 0.

3.9.4.2 Register "linShortFilter" Configuration for the LIN Short De-bounce Filter (ZSSC1750 Only)

Table 3.64 ZSSC1750 Register `linShortFilter`

Important: For the ZSSC1751 this register is not used and must remain as the default setting.

Name	Address	Bits	Default	Access	Description
linShortFilter	$B5_{HEX}$	[7:0]	$0F_{HEX}$	RW	Filter configuration for the LIN short detector. This register defines the number of 4MHz clock cycles (`linShortFilter` + 1) where the gated LIN SHORT signal in the LIN PHY must be high to detect a SHORT condition on the LIN bus.

3.9.4.3 Register "linShortDelay" –Configuration Register LIN Short TX-RX Delay (ZSSC1750 Only)

Table 3.65 ZSSC1750 Register `linShortDelay`

Important: For the ZSSC1751 this register is not used and must remain as the default setting.

Name	Address	Bits	Default	Access	Description
linShortDelay	$B6_{HEX}$	[7:0]	$4F_{HEX}$	RW	Delay configuration for gating the LIN SHORT signal. This register defines the number of 4MHz clock cycles where TXD is low and RXD is high before the gating logic of the LIN SHORT signal from the LIN PHY is removed. When RXD becomes low or TXD becomes high, the gating logic is reactivated. **Note:** When `linShortDelay` is set to 0, the TXD and RXD levels are ignored and the LIN SHORT signal is not gated.

3.9.4.4 Register "linWuDelay" – Configuration Register for LIN Wakeup Time (ZSSC1750 Only)

Table 3.66 ZSSC1750 Register linWuDelay

Important: For the ZSSC1751 this register is not used and must remain as the default setting.

Name	Address	Bits	Default	Access	Description
linWuDelay	$B7_{HEX}$	[4:0]	10100_{BIN}	RW	LIN wakeup time. This register defines the number of 125 kHz clock cycles where LIN-RXD must be low before a LIN wakeup conditions is detected. **Important Warning:** Do not set to 0.
Unused		[7:5]	000_{BIN}	RO	Unused; always write as 0

3.10 ZSSC1750/51 OTP (CONFIG REGISTER)

The ZSSC1750/51 has an integrated 32x8 bit one-time programmable (OTP) memory that contains the required trimming data as well as the traceability information. The default (erased) state of the OTP cells is 0. Because some of the programmed trim bits are critical for operation, such as the voltage trim bits, redundancy is implemented for the lower quarter of the OTP memory. This part of the OTP contains only up to four bits of information that are programmed to bits [3:0] as well as to bits [7:4]. During the download procedure, the correct content is determined by combining bit 0 and bit 4, bit 1 and bit 5, bit 2 and bit 6, and bit 3 and bit 7 via an OR gate.

Table 3.67 OTP Memory Map

Name	OTP Address	SPI Address	Bit Range	Copy to Reg.	Redun-dancy	Byte Order	Description
OTP_VALID	00_{HEX}	$E0_{HEX}$	0	No	Yes	---	[0]: OTP content valid
LIN_TRIM	01_{HEX}	$E1_{HEX}$	3:0	Yes	Yes	---	[3:0]: IBIAS_LIN_TRIM[3:0]
VDD_TRIM	02_{HEX}	$E2_{HEX}$	3:0	Yes	Yes	---	[0]: VDDC trim bit [1]: VDDP trim bit [3:2]: vbgh_trim[1:0]
BG_TRIM	03_{HEX}	$E3_{HEX}$	3:0	Yes	Yes	---	[3:0]: vbgh_trim[5:2]
IREF_OSC_0	04_{HEX}	$E4_{HEX}$	3:0	Yes	Yes	LSB	[3:0]: IREF_OSC_TC_TRIM[3:0]
IREF_OSC_1	05_{HEX}	$E5_{HEX}$	3:0	Yes	Yes	MSB LSB	[0]: IREF_OSC_TC_TRIM[4] [2]: IBIAS_LIN_TRIM[4] [3]: IREF_OSC_TRIM[0]
IREF_OSC_2	06_{HEX}	$E6_{HEX}$	3:0	Yes	Yes	---	[3:0]: IREF_OSC_TRIM[4:1]
IREF_OSC_3	07_{HEX}	$E7_{HEX}$	3:0	Yes	Yes	MSB	[3:0]: IREF_OSC_TRIM[8:5]
IREF_LP_OSC	08_{HEX}	$E8_{HEX}$	6:0	Yes	No	---	Trim value for the low-power oscillator
ADCCGAN_0	09_{HEX}	$E9_{HEX}$	7:0	Yes	No	LSB	Gain for the current measurement
ADCCGAN_1	$0A_{HEX}$	EA_{HEX}	7:0	Yes	No	---	
ADCCGAN_2	$0B_{HEX}$	EB_{HEX}	7:0	Yes	No	MSB	
ADCCOFF_0	$0C_{HEX}$	EC_{HEX}	7:0	Yes	No	LSB	Offset for the current measurement
ADCCOFF_1	$0D_{HEX}$	ED_{HEX}	7:0	Yes	No	---	
ADCCOFF_2	$0E_{HEX}$	EE_{HEX}	7:0	Yes	No	MSB	
ADCVGAN_0	$0F_{HEX}$	EF_{HEX}	7:0	Yes	No	LSB	Gain for the voltage measurement
ADCVGAN_1	10_{HEX}	$F0_{HEX}$	7:0	Yes	No	---	
ADCVGAN_2	11_{HEX}	$F1_{HEX}$	7:0	Yes	No	MSB	
ADCVOFF_0	12_{HEX}	$F2_{HEX}$	7:0	Yes	No	LSB	Offset for the voltage measurement
ADCVOFF_1	13_{HEX}	$F3_{HEX}$	7:0	Yes	No	---	
ADCVOFF_2	14_{HEX}	$F4_{HEX}$	7:0	Yes	No	MSB	
ADCTGAN_0	15_{HEX}	$F5_{HEX}$	7:0	Yes	No	LSB	Gain for the temperature measurement
ADCTGAN_1	16_{HEX}	$F6_{HEX}$	7:0	Yes	No	MSB	
ADCTOFF_0	17_{HEX}	$F7_{HEX}$	7:0	Yes	No	LSB	Offset for the temperature measurement
ADCTOFF_1	18_{HEX}	$F8_{HEX}$	7:0	Yes	No	MSB	
---	19_{HEX}	$F9_{HEX}$	---	No	No	---	Unused

Name	OTP Address	SPI Address	Bit Range	Copy to Reg.	Redun-dancy	Byte Order	Description
LOT_ID_0	$1A_{HEX}$	FA_{HEX}	7:0	No	No	LSB	Lot ID number
LOT_ID_1	$1B_{HEX}$	FB_{HEX}	7:0	No	No	MSB	
WAFER_NO_0	$1C_{HEX}$	FC_{HEX}	7:0	No	No	LSB	Wafer number
WAFER_NO_1	$1D_{HEX}$	FD_{HEX}	7:0	No	No	MSB	
DIE_POS_0	$1E_{HEX}$	FE_{HEX}	7:0	No	No	LSB	Die position
DIE_POS_1	$1F_{HEX}$	FF_{HEX}	7:0	No	No	MSB	

After reset of the SBC, the OTP download procedure is automatically triggered. First, the OTP contents are checked for validity (“bit 0 OR bit 4” must be equal to 1). If the content is not valid, the download procedure is stopped. Otherwise, the information stored at OTP addresses 1 to 18_{HEX} is copied into the corresponding registers. The download procedure can also be started by the user by writing the value 1 into the `otpDownload` bit in register `cmdExe` (see Table 3.7). Special care must be taken after starting the OTP download procedure as the system must not go to the power-down state as long as the download procedure is active. The status of the download procedure is signaled to the user via the `SSW` bit 0: the OTP download procedure is active when `SSW[0]` = 1.

In addition to being read by triggering the OTP download procedure that copies the OTP contents into the corresponding registers, the raw contents of the OTP can be read by the user via the SPI interface at SPI addresses $E0_{HEX}$ to FF_{HEX}. This might be useful for checking the contents of the OTP. For the lowest quarter of the OTP, this is useful for checking that no bit has changed its value. The user might also choose to implement redundancy for the other values by mirroring the contents into the nonvolatile memory on the external micro-controller.

3.11 Miscellaneous Registers

3.11.1.1 Register “pullResEna” – Pull-down Resistor Control Register

CSN, SCLK, MOSI, TXD, TRSTN, TCK, TMS, and WDT_DIS each contain a configurable internal pull-down resistor that is active by default. The pull-down resistors are present to prevent a floating input pin if the bonding wire is broken and to enable the system to detect such a broken wire or broken connections with the external microcontroller.

Example: If the bonding wire at TXD is broken, the pull-down resistor would drive TXD low continuously and the LIN TXD timeout detector will trigger and inform the external microcontroller that an error is present.

Directly behind the input pins is a secondary protection stage because VDDP is disabled in some power-down states. The ZSSC1750/51’s three SPI inputs, CSN, SCLK, and MOSI, as well as the TXD input, are only enabled in FP State. The WDT_DIS input is enabled as long as MCU_RSTN is high (in the FP or LP State) while the ZSSC1750/51’s three test inputs, TRSTN, TCK, and TMS, are only enabled when TEST is high.

Note: Because the TEST input pin also contains a pull-down resistor, disabling the pull-down resistors for the three test input pins is safe as long as TEST is low.

Table 3.68 Register `pullResEna`

Name	Address	Bits	Default	Access	Description
pullResEnaCsn	$B8_{HEX}$	[0]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the CSN pin is connected to the pin.
pullResEnaSpiClk		[1]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the SCLK pin is connected to the pin.
pullResEnaMosi		[2]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the MOSI pin is connected to the pin.
pullResEnaTxd		[3]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the TXD pin is connected to the pin.
pullResEnaTrstn		[4]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the TRSTN pin is connected to the pin.
pullResEnaTck		[5]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the TCK pin is connected to the pin.
pullResEnaTms		[6]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the TMS pin is connected to the pin.
pullResEnaWdtDis		[7]	1_{BIN}	RW	When set to 1, the pull-down resistor behind the WDT_DIS pin is connected to the pin

3.11.1.2 Register “versionCode” – Version Code of SBC

The version code of the SBC is 200_{HEX}.

Table 3.69 Register `versionCode`

Name	Address	Bits	Default	Access	Description
versionCode[7:0]	BA_{HEX}	[7:0]	00_{HEX}	RO	Version code of the SBC.
versionCode[11:8]	BB_{HEX}	[3:0]	0010_{BIN}	RO	
Unused		[7:4]	0000_{BIN}	RO	Unused; always write as 0.

3.11.1.3 Register "pwrTrim" – Trim Register for the Voltage Regulators and Bandgap

Table 3.70 Register `pwrTrim`

Name	Address	Bits	Default	Access	Description
vddcTrim	$C0_{HEX}$	[0]	0_{BIN}	RW	Trim register for VDDC regulator: 0 – VDDC is trimmed to 1.2V 1 – VDDC is trimmed to 1.8V **Note:** This register is set by the OTP download procedure when the OTP content is valid.
vddpTrim		[1]	0_{BIN}	RW	Trim register for the VDDP regulator: 0 – VDDP is trimmed to 2.5V 1 – VDDP is trimmed to 3.3V **Note:** This register is set by the OTP download procedure when the OTP content is valid.
vbghTrim		[7:2]	011111_{BIN}	RW	Trim register for the high-precision bandgap. **Note:** This register is set by the OTP download procedure when OTP content is valid.

Important Warning: Changing the settings of bits `vddcTrim` and `vddpTrim` could cause damage to the connected external microcontroller or cause it to malfunction!

3.11.1.4 Register "ibiasLinTrim" – Trim Register for the Bias Current of the LIN Block

Table 3.71 Register `ibiasLinTrim`

Name	Address	Bits	Default	Access	Description
ibiasLinTrim	$C3_{HEX}$	[4:0]	10000_{BIN}	RW	Trim register for the bias current of the LIN block: 0 – Smallest value 1 – Largest value **Note:** This register is set by the OTP download procedure when OTP contents are valid.
Unused		[7:5]	000_{BIN}	RO	Unused; always write as 0.

3.12 Voltage Regulators

In addition to the battery voltage (VBAT), four additional voltage domains are implemented in the ZSSC1750/51 as described in the following sections. The VDDA supply voltage for the analog sections is generated in the VDDA_REG block and available on the VDDA pin. The VDDL voltage for the digital sections during the ZSSC1750/51's LP State is generated in the LP_REG block and output on the VDDL pin, and it can be used as an optional low-power supply for the external microcontroller. The VDDP supply voltage for the SBC's I/O circuits is generated in the VDDP_REG block and output on the VDDP pin as an optional supply for the external microcontroller. The VDDC supply voltage, an optional supply for the external microcontroller, is generated in the VDDC_REG block and output on the VDDC pin. The regulators are low-dropout regulators (LDOs). The VDDL regulator, which is active in the low-power states, has very low power consumption.

3.12.1 VDDE

The following blocks are connected directly to V_{DDE}:

- Low-power bandgap
- High-precision bandgap
- High-precision oscillator
- POR
- Regulator for VDDA
- Regulator for VDDL
- Regulator for VDDC
- Regulator for VDDP

3.12.2 VBAT

VBAT is the input for the battery voltage measurement using the voltage ADC. It is connected to a resistive divider, dividing VBAT to a usable single-ended voltage for the voltage ADC (maximum 1.2V).

3.12.3 VDDA

The analog regulator provides a 2.5V output and can drive up to 10mA of load current. The output voltage is continuously regulated with respect to the bandgap voltage (vbgh). A resistor chain generates the appropriate voltage for the feedback comparison with the bandgap voltage so that the correct voltage is generated. This internal regulated voltage serves as a supply voltage for the analog blocks. The analog regulator can be switched off (e.g., in Sleep Mode).

The following blocks are connected directly to VDDA:

- Level-Shifter
- PGA
- Divider
- Temperature Measurement
- SD-ADC Channel 1 (current)
- SD-ADC Channel 2 (voltage and temperature)
- All blocks necessary for data acquisition (current, voltage, and temperature measurements)

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3.12.4 VDDL

The VDDL regulator provides the supply voltage for the ZSSC1750/51's digital domain. This regulator remains active in ULP and OFF States. The following blocks are connected directly to VDDL:

- LIN PHY control (ZSSC1750 only)
- Power Management Unit
- All ZSSC1750/51 registers
- Watchdog timer

3.12.5 VDDP

The peripheral regulator provides 3.3V. The VDDP regulator can drive up to 40mA of load current and can be switched off (e.g., in Sleep Mode). This voltage is recommended for the supply of the external microcontroller to ensure matching I/O voltage levels as the I/O blocks of the ZSSC1750/51 are also connected directly to VDDP.

VDDP can be trimmed to the lower range given in specification 1.3.9 using the `vddpTrim` bit field in Table 3.70.

Important Warning: An improper `vddpTrim` setting could cause damage to the connected external microcontroller or cause it to malfunction! See section 3.3.4 regarding VDDP trimming and the reset function.

3.12.6 VDDC

The core regulator provides 1.8V. This regulator can drive up to 40mA of load current and can be switched off (e.g., in Sleep Mode).This voltage can be used for powering the core of an external microcontroller that requires a lower core voltage than VDDP.

VDDC can be trimmed to the lower range given in specification 1.3.8 using the `vddcTrim` bit field in Table 3.70.

Important Warning: An improper `vddcTrim` setting could cause damage to the connected external microcontroller or cause it to malfunction!

4 ESD / EMC

The ZSSC175x is designed to maximize EM immunity and minimize emissions. (References to LIN communication are only applicable to the ZSSC1750.)

Functional status A: According to specifications; no LIN communication errors; memory content must not be lost; no wake-up from Sleep Mode; no reset.

Functional status B: According to specifications; offset error extended to ≤ 100mA; no LIN communication errors; memory content must not be lost; no wake-up from Sleep Mode; no reset.

Functional status C: Measurement tolerance beyond specifications; LIN communication errors allowed; memory content must not be lost; reset allowed.

During EM exposure, all functions perform as designed; after exposure, all functions return automatically to within normal limits; memory functions always remain in functional status A.

4.1 Electrostatic Discharge

Table 4.1 ESD Protection According to AEC-Q100 Rev. G

No.	Parameter	Condition	Min	Max	Unit
4.1.1.	ESD, LIN on system level [1)]	IEC 61000-4-2	±6		kV
4.1.2.	ESD, BAT+ on system level [2)]	IEC 61000-4-2	±6		kV
4.1.3.	ESD, HBM, all other pins	AEC Q 100-002	±2		kV
4.1.4.	ESD, CDM, corner pins	AEC Q 100-011	±750		V
4.1.5.	ESD, CDM, all other pins	AEC Q 100-011	±500		V

1) For higher ESD levels additional diode is required (see Figure 4 1).
2) With external protection diode GSOT36 (see Figure 4.1).

4.2 Power System Ripple Factor

Component functionality meets these specifications.

U_N = 13.5V
Voltage variation: sine wave
Amplitude ΔV = ±2V
Frequency range: 50Hz ≤ f ≤ 25kHz *(linear sweep width for 10 minutes)*
Ri of output stage ≤ 100mΩ

4.3 Application Circuit Examples for EMC Conformance

The final application might require adaption of the external circuit for EMC compliance in the target system as shown in Figure 4.1 and Figure 4.2.

Figure 4.1 Optional External Components for ZSSC1750

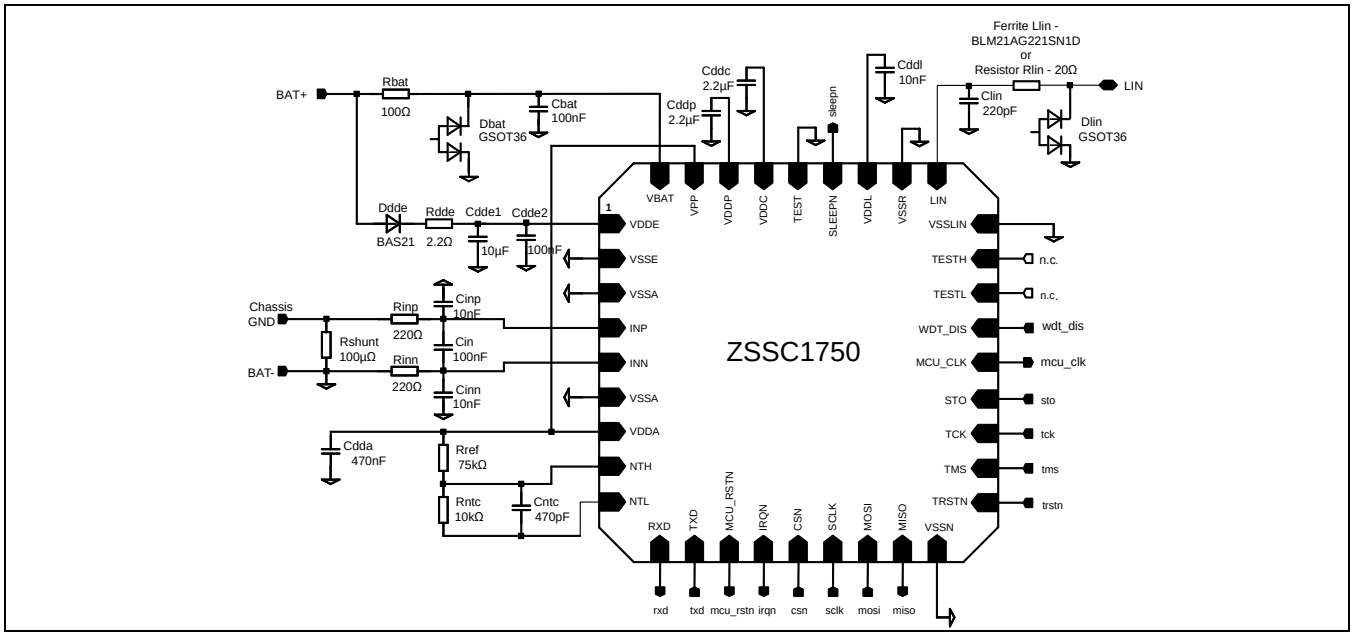
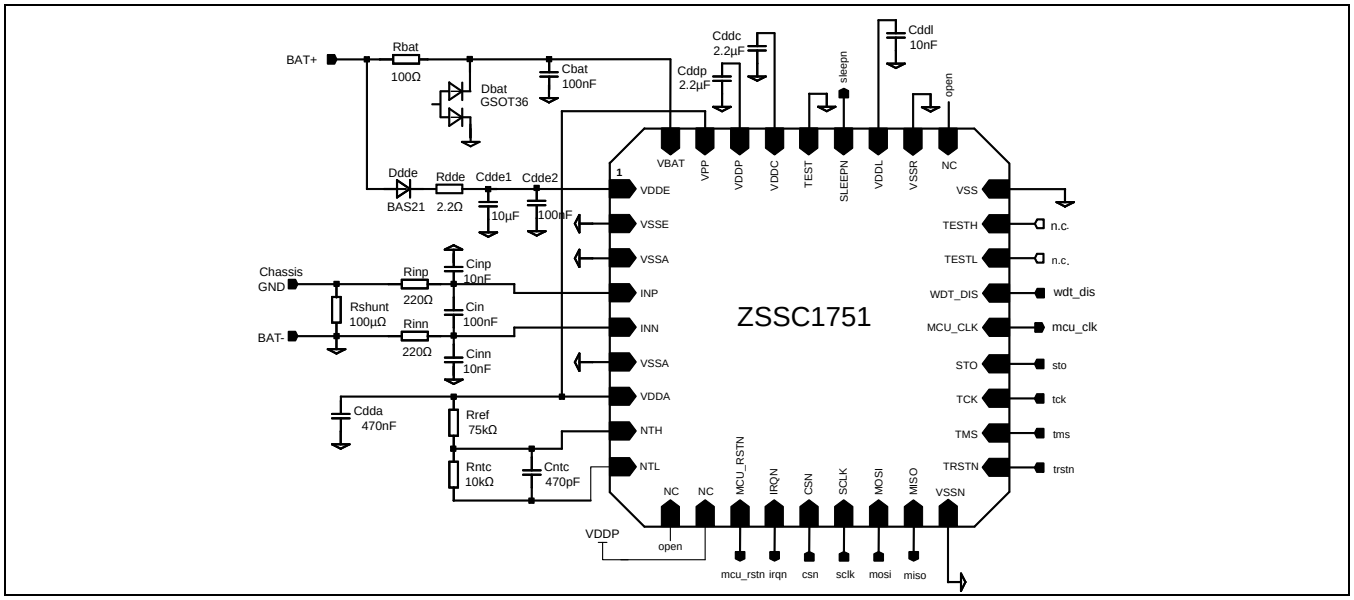
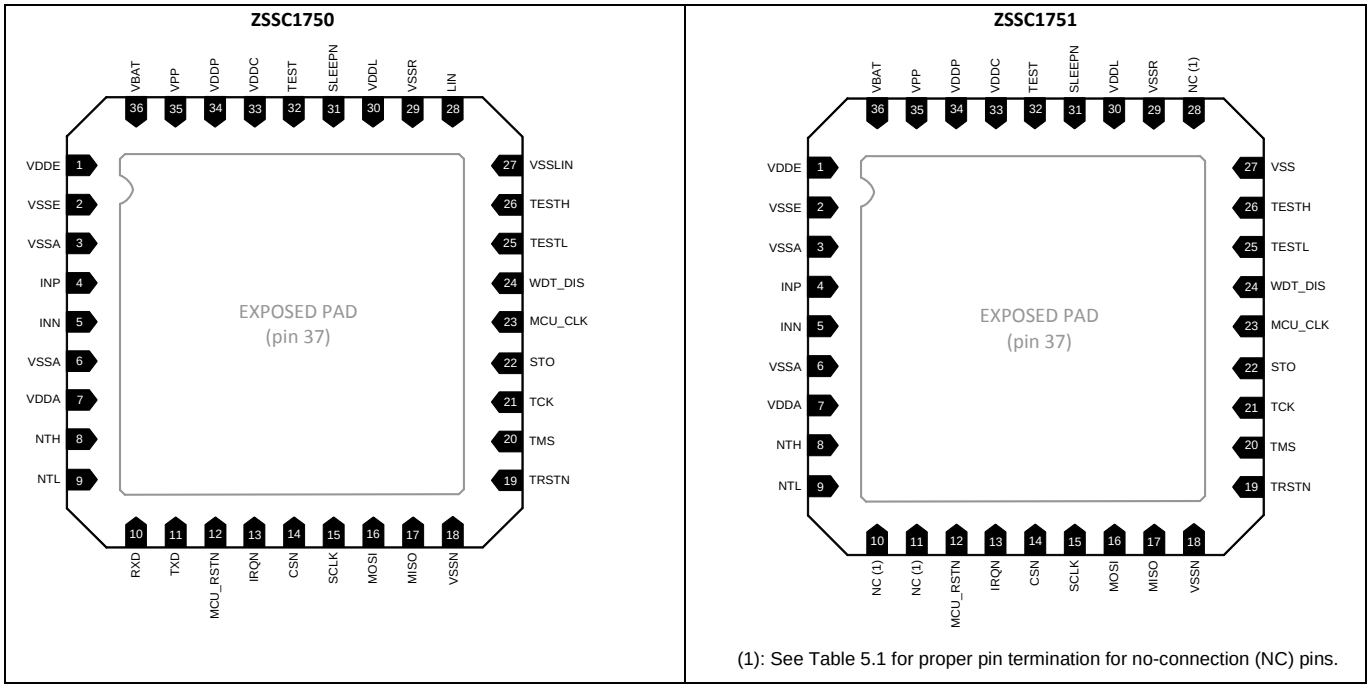


Figure 4.2 Optional External Components for ZSSC1751



5 Pin Configuration and Package

Figure 5.1 ZSSC1750/51 PQFN36 6x6mm Package Pin-out (Top View)



(1): See Table 5.1 for proper pin termination for no-connection (NC) pins.

Table 5.1 ZSSC1750/51 Pins Description

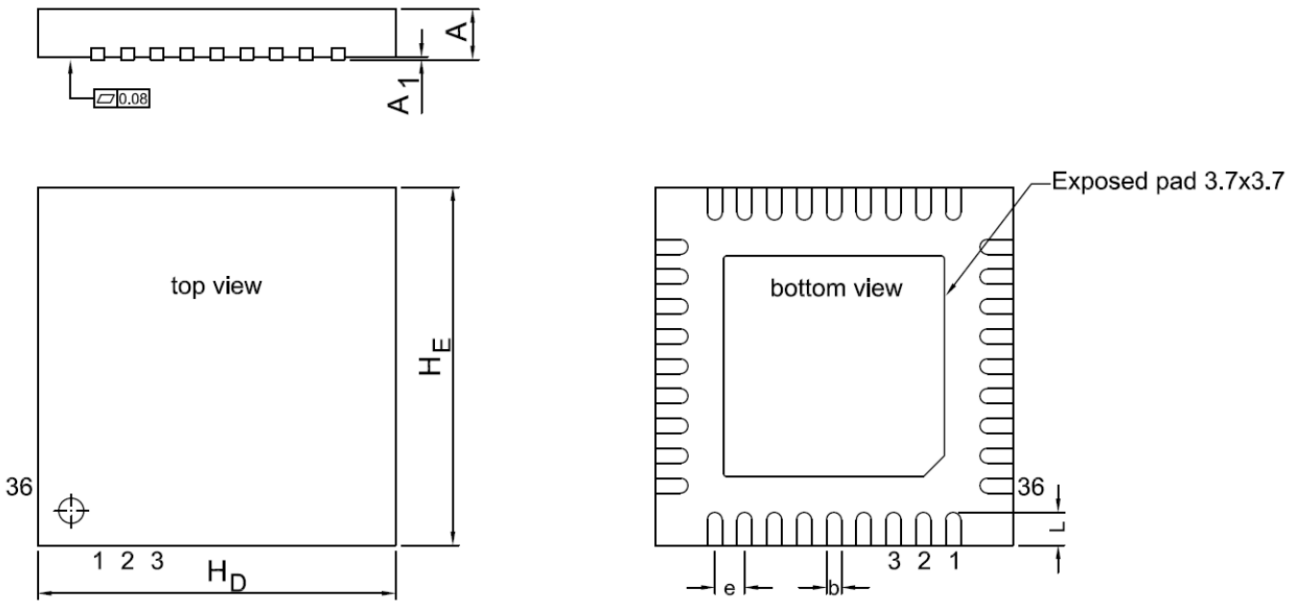
Note: See important notes at the end of the table.

Pin	Pin Name	Type	Mode	Description
1	VDDE	Supply	Input	Power supply
2	VSSE	Supply	Input	Power ground
3	VSSA	Supply	Input	Analog voltage ground
4	INP	Analog	Input	Positive input for current channel
5	INN	Analog	Input	Negative input for current channel
6	VSSA	Supply	Input	Analog voltage ground
7	VDDA	Analog	Output	Analog voltage supply
8	NTH	Analog	Input	Positive input for the temperature channel
9	NTL	Analog	Input	Negative input for the temperature channel
10	RXD	Digital	Output	LIN receiver output for ZSSC1750 only
	NC	N/A	N/A	Not used in ZSSC1751 – **keep open**
11	TXD [1)]	Digital	Input	LIN transmitter input for ZSSC1750 only

Pin	Pin Name	Type	Mode	Description
	NC	N/A	N/A	Not used in ZSSC1751 – **connect to VDDP**
12	MCU_RSTN	Digital	Output	Reset for external microcontroller
13	IRQN	Digital	Output	Interrupt for external microcontroller
14	CSN [1)]	Digital	Input	SPI chip select
15	SCLK [1)]	Digital	Input	SPI clock
16	MOSI [1)]	Digital	Input	SPI Master output, Slave input
17	MISO	Digital	Output	SPI master input, slave output
18	VSSN	Supply	Input	Digital voltage ground
19	TRSTN [1), 2)]	Digital	Input	Test interface
20	TMS [1), 2)]	Digital	Input	Test interface
21	TCK [1), 2)]	Digital	Input	Test interface
22	STO	Digital	Output	Test interface
23	MCU_CLK	Digital	Output	Clock signal to external microcontroller (20MHz)
24	WDT_DIS [1)]	Digital	Input	Watchdog timer disable pin
25	TESTL [2)]	Analog	In/Out	Test interface
26	TESTH [2)]	Analog	In/Out	Test interface
27	VSSLIN	Supply	Input	LIN ground for ZSSC1750
	VSS	Supply	Input	Power ground for ZSSC1751
28	LIN	Analog	In/Out	LIN bus for ZSSC1750
	NC	N/A	N/A	Not used in ZSSC1751 – **keep open.**
29	VSSR	Supply	Input	Power ground
30	VDDL	Analog	Output	SBC digital core supply
31	SLEEPN	Digital	Output	SBC power state indicator pin
32	TEST	Digital	Input	Test interface enable; connect to ground in application
33	VDDC	Analog	Output	External microcontroller supply voltage (core)
34	VDDP	Analog	Output	External microcontroller supply voltage (periphery)
35	VPP	Analog	Input	OTP programming voltage
36	VBAT	Analog	Input	Input for battery voltage monitor
37	EXPOSED PAD	Supply	Input	Connect to VSSE in application

1) Digital input with internal pull-down resistor. See parameter R_{PULL_DOWN} in Table 1.3.
2) Connect to ground in application.

Figure 5.2 Package Drawing of the ZSSC1750/51



Dimensions	Min (mm)	(mm)
A	0.8	0.9
A_1	0	0.05
b	0.2	0.3
E	0.5 nom	
H_D	5.9	6.1
H_E	5.9	6.1
L	0.45	0.65

6 Ordering Information

Product Sales Code	Description	Package
ZSSC1750EA3R	ZSSC1750 Battery Sensing SBC—Temperature Range: -40°C to 125°C	PQFN36 6x6 mm, reel
ZSSC1751EA3R	ZSSC1751 Battery Sensing SBC—Temperature Range: -40°C to 125°C	PQFN36 6x6 mm, reel
ZSSC1750KIT V1.1	ZSSC1750/51 Evaluation Kit: modular evaluation and development board for ZSSC1750/51, 3 IC samples, and USB cable, (software and documentation can be downloaded from www.IDT.com)	

7 Related Documents

Document
ZSSC1750/51 Feature Sheet
Application Notes
Technical Note – Die Pad Dimensions and Coordinates

Visit the ZSSC175x product pages at www.IDT.com or contact your nearest sales office for the latest version of these documents.

8 Glossary

Term	Description
ADC	Analog-to-Digital Converter
BIST	Built-In Self-Test
DAP	Debug Access Port
ECC	Error Correction Code
FP	Full Power State
FSR	Full Scale Range
IFC	Current Interface
IFT	Temperature Interface
ITS	Internal Temperature Sensor
LIN	Local Interconnect Network
LP	Low Power state
LSB	Least Significant Bit or Byte Depending on Context
MCU	Micro Controller Unit (external microcontroller)
MPX	Multiplexer
MRCS	Multiple Results per Conversion Sequence

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Term	Description
MSB	Most Significant Bit
NMI	Non-maskable Interrupt
NTC	Negative Temperature Coefficient
OTP	One-Time Programmable Memory
PA-C	Preamplifier for Current
PA-T	Preamplifier for Temperature
PGA	Programmable Gain Amplifier
POR	Power-On-Reset
PPB	Private Peripheral Bus
PTAT	Proportional to Absolute Temperature
SBC	System Basis Chip
SDM	Sigma Delta Modulator
SPI	System Packet Interface
SRCS	Single Result per Conversion Sequence
ULP	Ultra Low Power State

9 Document Revision History

Revision	Date	Description
1.00	July 10, 2014	First release.
	April 20, 2016	Changed to IDT branding.

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