Integrated Circuit Systems, Inc.

ICS950811

Frequency Generator with 200MHz Differential CPU Clocks

Recommended Application:

CK-408 clock for Brookdale-Mobile chipsets.

Programmable for group to group skew.

Output Features:

- 3 Differential CPU Clock Pairs (differential current mode)
- 7 PCI (3.3V) @ 33.3MHz
- 3 PCI_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz
- 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 5 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz

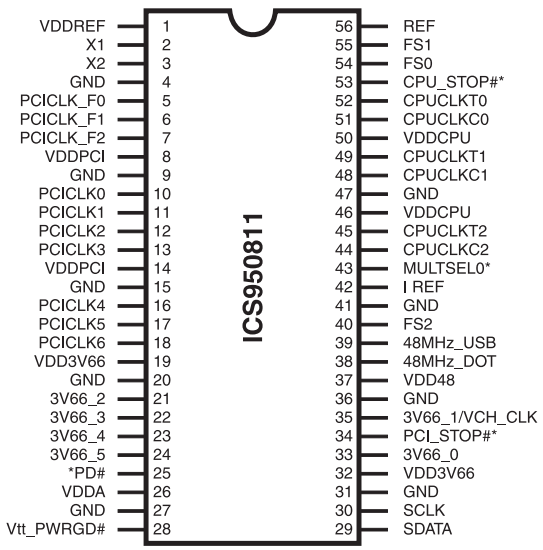
Features:

- Supports spread spectrum modulation, down spread 0 to -0.5%.
- Efficient power management scheme through PD#, CPU_STOP# and PCI_STOP#.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- 66MHz Output Jitter (Buffered Mode Only) <100ps
- CPU Output Skew <100ps

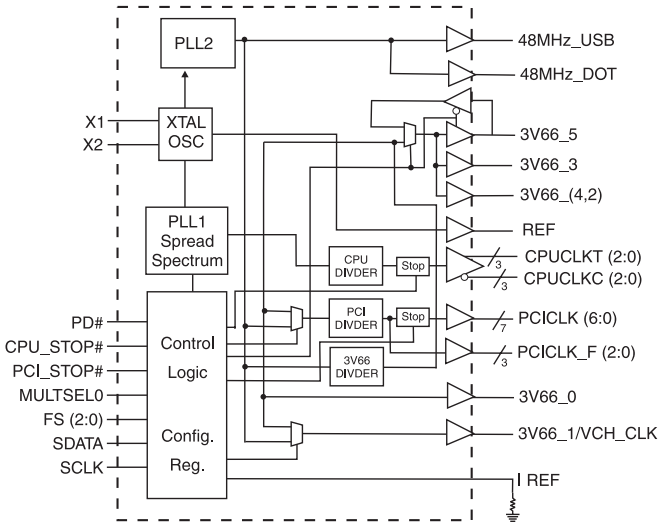
Pin Configuration



56 pin SSOP/TSSOP

* These inputs have 150K internal pull-up resistor to VDD.

Block Diagram



Functionality

FS2	FS1	FS0	CPU (MHz)	3V66(1:0) (MHz)	66MHzOut(2:0) 3V66(4:2) (MHz)	PCI_F PCI (MHz)	66MHzIn 3V66(5) (MHz)
0	0	0	66.66	66.66	66.66	33.33	66.66
0	0	1	100.00	66.66	66.66	33.33	66.66
0	1	0	200.00	66.66	66.66	33.33	66.66
0	1	1	133.33	66.66	66.66	33.33	66.66
1	0	0	66.66	66.66	Buffered Mode Not Supported See ICS950805		
1	0	1	100.00	66.66			
1	1	0	200.00	66.66			
1	1	1	133.33	66.66			
Mid	0	0	Tristate	Tristate	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/4
Mid	1	0	Reserv-ed	Reserved	Reserved	Reserved	Reserved
Mid	1	1	Reserv-ed	Reserved	Reserved	Reserved	Reserved

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 14, 19, 26, 32, 37, 46, 50	VDD	PWR	3.3V power supply
2	X1	X2 Crystal Input	14.318MHz Crystal input
3	X2	X1 Crystal Output	14.318MHz Crystal output
7, 6, 5	PCICLK_F (2:0)	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
4, 9, 15, 20, 27, 31, 36, 41, 47	GND	PWR	Ground pins for 3.3V supply
18, 17, 16, 13, 12,11, 10	PCICLK (6:0)	OUT	PCI clock outputs
24, 23, 22, 21	3V66 (5:2)	OUT	66MHz reference clocks, from internal VCO
25	PD#	IN	Invokes power-down mode. Active Low.
28	Vtt_PWRGD#	IN	
29	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
30	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
33	3V66_0	OUT	66MHz reference clocks, from internal VCO
34	PCI_STOP#	IN	Halts PCICLK clocks at logic 0 level, when input low except PCICLK_F which are free running
35	3V66_1/VCH_CLK	OUT	3.3V output selectable through I^2C to be 66MHz from internal VCO or 48MHz (non-SSC)
38	48MHz_DOT	OUT	48MHz output clock for DOT
39	48MHz_USB	OUT	48MHz output clock for USB
40	FS2	IN	Special 3.3V input for Mode selection
42	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43	MULTSEL0	IN	3.3V LVTTL input for selecting the current multiplier for CPU outputs
44, 48, 51	CPUCLKC (2:0)	OUT	"Complementory" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
45, 49, 52	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
53	CPU_STOP#	IN	Halts CPUCLK clocks at logic 0 level, when input low
55, 54	FS (1:0)	IN	Frequency select pins
56	REF	OUT	14.318MHz reference clock.

Power Groups

(Analog)	(Digital)
VDDA = PLL1	VDDPCI
VDD48 = 48MHz, PLL	VDD3V66
VDDREF = VDD for Xtal, POR	VDDCPU

Truth Table

FS2	FS1	FS0	CPU (MHz)	3V66 (1:0) (MHz)	66Buff (2:0) 3V66 (4:2) (MHz)	66MHz_IN/ 3V66_5	PCI_F PCI (MHz)	REF0 (MHz)	USB/DOT (MHz)
0	0	0	66.66	66.66	66.66	66.66	33.33	14.318	48.00
0	0	1	100.00	66.66	66.66	66.66	33.33	14.318	48.00
0	1	0	200.00	66.66	66.66	66.66	33.33	14.318	48.00
0	1	1	133.33	66.66	66.66	66.66	33.33	14.318	48.00
1	0	0	66.66	66.66	Buffered Mode Not Supported See ICS950805				
1	0	1	100.00	66.66					
1	1	0	200.00	66.66					
1	1	1	133.33	66.66					
Mid	0	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/4	TCLK/4	TCLK/4	TCLK/8	TCLK	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Maximum Allowed Current

Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PWRDWN# = 0)	40mA
Full Active	360mA

Host Swing Select Functions

MULTISEL0	Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3*Rr)	Output Current	Voh @ Z
0	Buffered Mode Not Supported See ICS950805			
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Byte 0: Control Register

Bit	Pin#	Name	PWD[2]	Type[1]	Description
Bit 0	54	FS0	X	R	Reflects the value of FS0 pin sampled on power up
Bit 1	55	FS1	X	R	Reflects the value of FS1 pin sampled on power up
Bit 2	40	FS2	X	R	Reflects the value of FS2 pin sampled on power up
Bit 3	34	PCI_STOP#[3]	X	R	Hardware mode: Reflects the value of PCI_STOP# pin sampled on PWD
			1	RW	Software mode: 0=PCICLK stopped 1=PCICLK not stopped
Bit 4	53	CPU_STOP#	X	R	Reflects the current value of the external CPU_STOP# pin
Bit 5	35	3V66_1/VCH	0	RW	VCH Select 66MHz/48MHz 0=66MHz, 1=48MHz
Bit 6	-	CPU_T(2:0)	0		In power down mode controls output level 0=stop high 1=stop low
Bit 7	-	Spread Enabled	0	RW	0=Spread Off, 1=Spread On

Byte 1: Control Register

Bit	Pin#	Name	PWD[2]	Type[1]	Description
Bit 0	52, 51	CPUCLKT0 CPUCLKC0	1	RW	0=Disabled 1=Enabled[4]
Bit 1	49, 48	CPUCLKT1 CPUCLKC1	1	RW	0=Disabled 1=Enabled[4]
Bit 2	45, 44	CPUCLKT2 CPUCLKC2	1	RW	0=Disabled 1=Enabled[4]
Bit 3	52, 51	CPUCLKT0 CPUCLKC0	0	RW	Allow control of CPUCLKT0/C0 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 4	49, 48	CPUCLKT1 CPUCLKC1	0	RW	Allow control of CPUCLKT1/C1 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 5	45, 44	CPUCLKT2 CPUCLKC2	0	RW	Allow control of CPUCLKT2/C2 with assertion of CPU_STOP# 0=Not free running 1=Free running
Bit 6	-	-	0	-	(Reserved)
Bit 7	43	MULTSEL0	X	R	Reflects the current value of MULTSEL0

Notes:

1. R= Read only RW= Read and Write
2. PWD = Power on Default
3. The purpose of this bit is to allow a system designer to implement PCI_STOP functionality in one of two ways. Wither the system designer can choose to use the externally provided PCI_STOP# pin to assert and de-assert PCI_STOP functionality via I^2C Byte 0 Bit 3.

   In Hardware mode it is not allowed to write to the I^2C Byte 0 Bit3. In Software mode it is not allowed to pull the external PCI_STOP pin low. This avoids the issues related with Hardware started and software stopped PCI_STOP conditions. The clock chip is to be operated in the Hardware or Software PCI_STOP mode ONLY, it is not allowed to mix these modes.

   In Hardware mode the I^2C byte 0 Bit 3 is R/W and should reflect the status of the part. Whether or not the chip is in PCI_STOP mode.

   Functionality PCI_STOP mode should be entered when [(PCI_STOP#=0) or (I^2C Byte 0 Bit 3 = 0)].
4. For disabled clocks, they stop low for single ended clocks. Differential CPU clocks stop with CPUCLKT at high, CPUCLKC off, and external resistor termination will bring CPUCLKC low.

Byte 2: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	10	PCICLK0	1	RW	0=Disabled 1=Enabled
Bit 1	11	PCICLK1	1	RW	0=Disabled 1=Enabled
Bit 2	12	PCICLK2	1	RW	0=Disabled 1=Enabled
Bit 3	13	PCICLK3	1	RW	0=Disabled 1=Enabled
Bit 4	16	PCICLK4	1	RW	0=Disabled 1=Enabled
Bit 5	17	PCICLK5	1	RW	0=Disabled 1=Enabled
Bit 6	18	PCICLK6	1	RW	0=Disabled 1=Enabled
Bit 7	-	-	0	-	(Reserved)

Byte 3: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	5	PCICLK_F0	1	RW	0=Disabled 1=Enabled
Bit 1	6	PCICLK_F1	1	RW	0=Disabled 1=Enabled
Bit 2	7	PCICLK_F2	1	RW	0=Disabled 1=Enabled
Bit 3	5	PCICLK_F0	0	RW	Allow control of PCICLK_F0 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 4	6	PCICLK_F1	0	RW	Allow control of PCICLK_F1 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 5	7	PCICLK_F2	0	RW	Allow control of PCICLK_F2 with assertion of PCI_STOP#. 0=Free Running, 1=Not free running
Bit 6	39	48MHz_USB	1	RW	0=Disabled 1=Enabled
Bit 7	38	48MHz_DOT	1	RW	0=Disabled 1=Enabled

Byte 4: Control Register

Bit	Pin#	Name	PWD	Type	Description
Bit 0	21	3V66-2	1	RW	0=Disabled 1=Enabled
Bit 1	22	3V66-3	1	RW	0=Disabled 1=Enabled
Bit 2	23	3V66-4	1	RW	0=Disabled 1=Enabled
Bit 3	24	3V66_5	1	RW	0=Disabled 1=Enabled
Bit 4	35	3V66_1/VCH_CLK	1	RW	0=Disabled 1=Enabled
Bit 5	33	3V66_0	1	RW	0=Disabled 1=Enabled
Bit 6	-	-	0	R	(Reserved)
Bit 7	-	-	0	R	(Reserved)

Notes:

1. R= Read only RW= Read and Write
2. PWD = Power on Default

Byte 5: Programming Edge Rate
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Type	Description
Bit 0	X	48MHz_USB	0	RW	USB edge rate cntrol
Bit 1	X	48MHz_USB	0	RW	USB edge rate cntrol
Bit 2	X	48MHz_DOT	0	RW	DOT edge rate control
Bit 3	X	48MHz_DOT	0	RW	DOT edge rate control
Bit 4	X	-	0	-	(Reserved)
Bit 5	X	-	0	-	(Reserved)
Bit 6	X	-	0	-	(Reserved)
Bit 7	X	-	0	-	(Reserved)

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Type	Description
Bit 0	X	Vendor ID Bit0	1	R	(Reserved)
Bit 1	X	Vendor ID Bit1	1	R	(Reserved)
Bit 2	X	Vendor ID Bit2	1	R	(Reserved)
Bit 3	X	Vendor ID Bit3	1	R	(Reserved)
Bit 4	X	Revision ID Bit0	1	R	Revision ID values will be based on individual device's revision
Bit 5	X	Revision ID Bit1	1	R	
Bit 6	X	Revision ID Bit2	1	R	
Bit 7	X	Revision ID Bit3	1	R	

Notes:

1. R= Read only RW= Read and Write
2. PWD = Power on Default

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V

Ambient Operating Temperature . . . . . 0°C to +85°C

Case Temperature . . . . . 115°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz	229	230	360	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz	220	233	360	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=5 mA		38.1	45	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency		1	3	ms
Time to first clock[1]	T_{1C}	Time to first clock			1.8	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Rise Time	t_{r3}	V_{OL} = 0.41V, V_{OH} = 0.86V	175	240	700	ps
Fall Time	t_{f3}	V_{OH} = 0.86V V_{OL} = 0.41V	175	242	700	ps
Duty Cycle	d_{t3}	measurement from differential wavefrom -0.35V to +035V	45	51	55	%
Skew	t_{sk3}	V_T = 50%		50	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		76	150	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - PCICLK

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			33.33		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12	33	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.32	0.5to 2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.39	0.5 to 2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		247	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		111	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.38	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.45	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.4	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		243	500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66		139	300	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			48		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.6	1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.8	1	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.2	2	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.3	2	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.8	55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53.5	55	%
48 DOT Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		183	350	ps
VCH Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		223	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

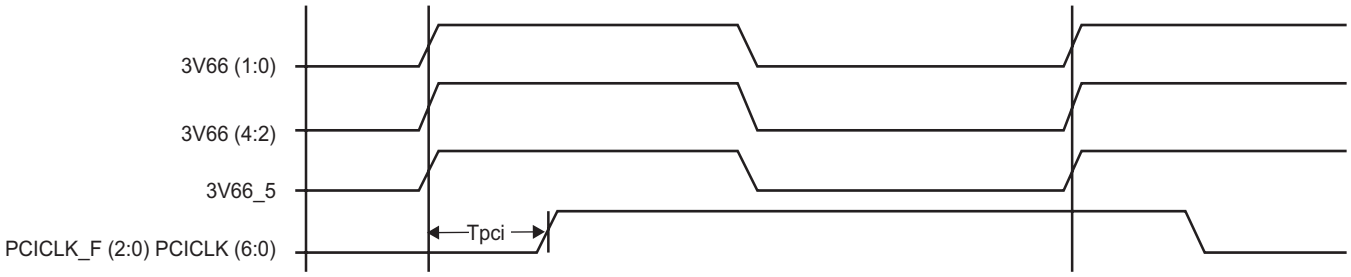
T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			14.318		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.25	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.15	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		723	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Un-Buffered Mode 3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group Skews at Common Transition Edges: (Un-Buffered Mode)

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 (5:0) pin to pin skew	0	42	500	ps
PCI	PCI	PCI_F (2:0) and PCI (6:0) pin to pin skew	0	130	500	ps
3V66 to PCI	$S_{3V66-PCI}$	3V66 (5:0) leads 33MHz PCI	1.5	2.86	3.5	ns

[1]Guaranteed by design, not 100% tested in production.

Normal operation transition to Suspend State S1 Entry sequence of events:

1. Power-Down (PD#) pin is taken from a high to low to start into S1 Suspend state with digital filtering of the transition in the clock circuit.
2. The first clocks to be forced to a Stop Low power down condition are the PCI buffer output clocks after a full clock cycle. If the PCI_Stop# is low, then the free-running PCI clocks (for PCI and APIC signals) are the remaining PCI buffer clocks stopped.
3. Immediately after the PCI clocks have been stopped the 66Buf_0:2 clocks are stopped low after the next high to low transition. It will always be a sequence of PCI stopping, THEN the 66Buf clocks.
4. Following the two buffer output clocks being stopped (PCI then 66.6Buffer outputs), the remaining clocks within a short delay will transition to a stopped power-down state. The first of these driven clocks that transition to a stopped state are all of the CPU PLL clocks: the CPU and the driven 3V66 clocks.
5. After the CPU PLL clocks are stopped, the 48 MHz clocks (USB, DOT clocks) will stop low, then the REF clock 14.318 MHz clock will stop low.
6. After the clocks have all been stopped, the internal PLL stages and the Crystal oscillator will all be driven to a low power stopped condition.
7. As a note to power management calculations, please be aware that the CPU design requires that in the Power-Down (S1 mode) the CPU outputs have a differential bias voltage driving the differential input stage of the CPU in this S1 state. For this PD condition of the clock generator, the IDD_PD is running around 30 to 45 mA from having the Iref running (5 mA), the output multiplier bias generator at a 2X condition and the output current source outputs are running at a 2xIref bias level (for approx 10 mA each CPU output). This results in a higher level of Clock generator IDD_PD than in prior generations of clocks due to the CPU output differential requirements.

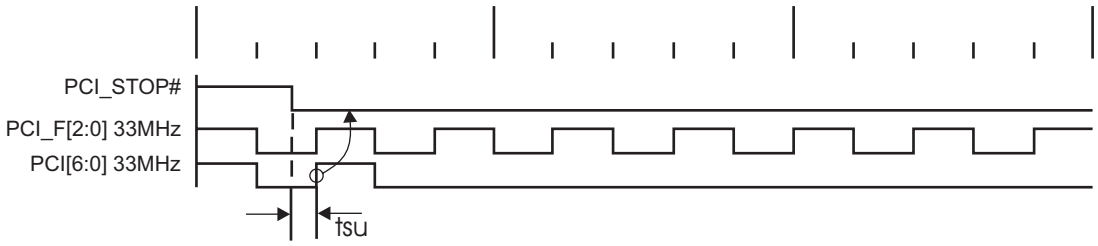
Suspend State S1 Exit transition to normal operation sequence of events:

1. Power-Down (PD#) pin is taken from Low to High with digital filtering of the transition in the clock circuit to return to normal running operation.
2. The Crystal Oscillator and the two PLL stages are released from PD to start-up to normal operation. No clocks will operate until the Lock detect circuitry verifies the PLL has reached stable final frequency (the same as normal initial power-up).
3. The CPU PLL clocks (differential CPU outputs and the driven 3V66_(0:1) clocks are operating first as soon as the Lock detect releases the clocks. With the release of these clocks, the single 66Buf_1 buffer driven output (at pin 22) is also released from the PD stopped state (but NOT the other 66Buf0,2 and not the PCI outputs). This allows the GMCH chipset 66.6 MHz DLL stage to start operating and have an operating feedback path before the other buffer outputs are released. This change is why the requirement is made that pin 22 be the connection from the clock to the GMCH chipset. Note that along with the 66Buf_0,2 and the PCI clocks, the 48 MHz and REF (14.318 MHz) clocks are also NOT released at this point.
4. A delay is built into the clock generator that allows the CPU, driven 3V66_0,1 and the single buffer clock 66Buf_1 (at pin 22) to operate before other clocks are released. This delay is larger than 30 uS and shorter than 400 uS, and after this the other clocks are staged for a sequential release.
5. The initial clocks released after the delay are the 66Buf_0, 2 outputs.
6. After the 66Buf_0,2 clocks are released, then the PCI clocks are released.
7. It will always be the sequence of 66_1 (pin 22) released with the CPU clocks, then after the delay the remaining 66Buf_0,2 first, THEN the PCI clocks.
8. Following the 66Buf_0,2 clocks, the 48 MHz (DOT and USB clocks) and the REF (14.318MHz) clocks are released.
9. Note, the initial power-up time is the same as this PD release, the PLL will power-up and the outputs will be running within a 3 ms time point.

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

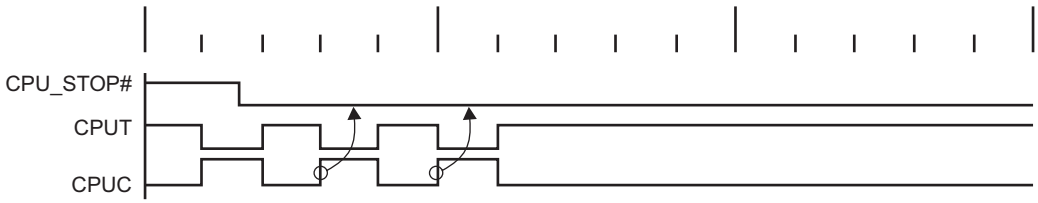
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=High and CPUC=Low. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

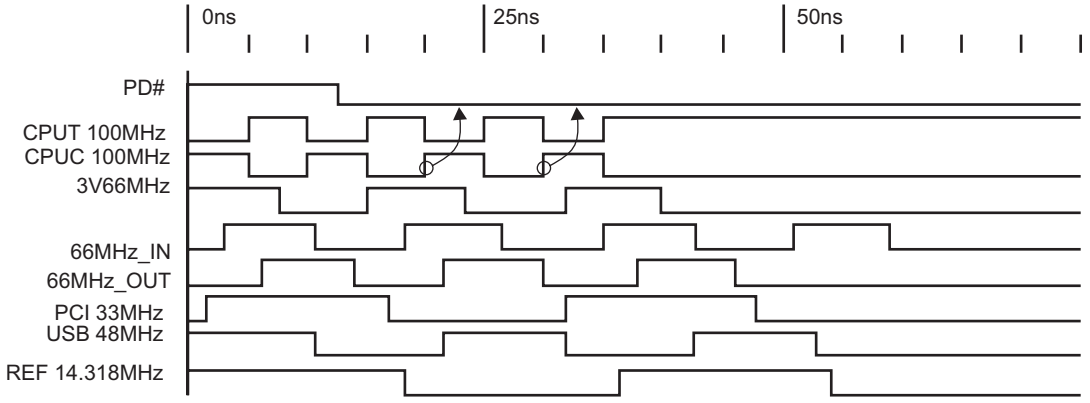
CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float

PD# - Assertion (transition from logic "1" to logic "0")

When PD# is sampled low by two consecutive rising edges of CPU clock then all clock outputs except CPU clocks must be held low on their next high to low transition. CPU clocks must be held with the CPU clock pin driven high with a value of 2x Iref, and CPUC undriven. Note the example below shows CPU = 100MHz, this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200MHz.

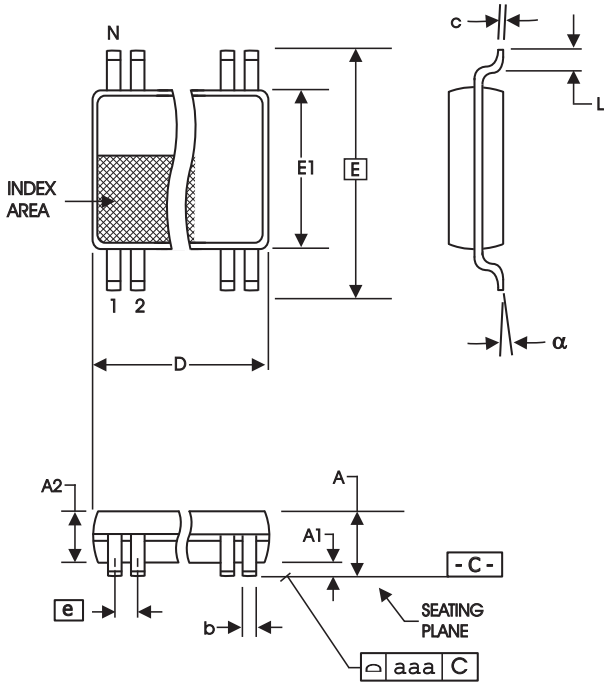
Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms - Buffered Mode



PD# Functionality

CPU_STOP#	CPUT	CPUC	3V66	66MHz_OUT	PCICLK_F PCICLK	PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	66MHz_IN	66MHz_IN	66MHz_IN	48MHz
0	iref * Mult	Float	Low	Low	Low	Low	Low



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS950811yGLFT

Example:

ICS XXXX y G - LF - T

Designation for tape and reel packaging

Lead Free, RoHS Compliant (Optional)

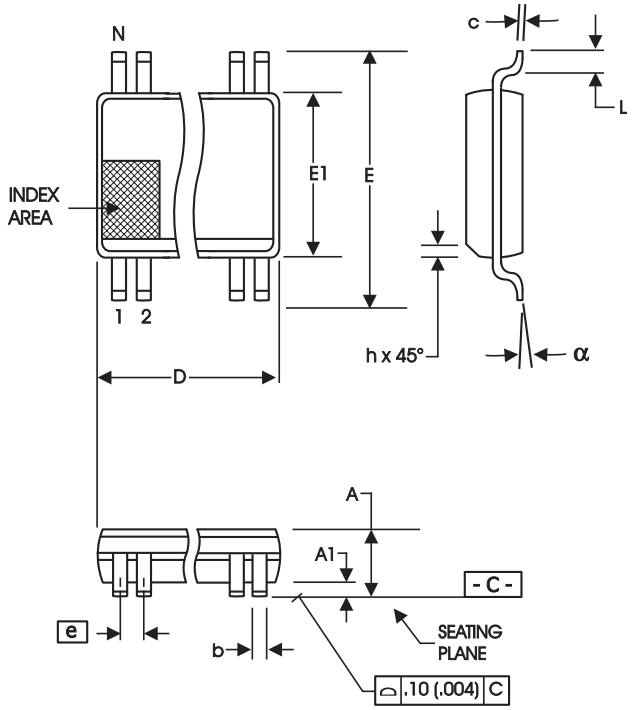
Package Type
G = TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS = Standard Device

0482E—08/09/07



56-Lead, 300 mil Body, 25 mil, SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950811yFLFT

Example:

ICS XXXX y F - LF - T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0482E—08/09/07

Revision History

Rev.	Issue Date	Description	Page #
D	12/21/06	1. Removed SSOP Package Information. 2. Added LF Ordering Information.	16
E	08/09/07	Added SSOP Package Information.	17