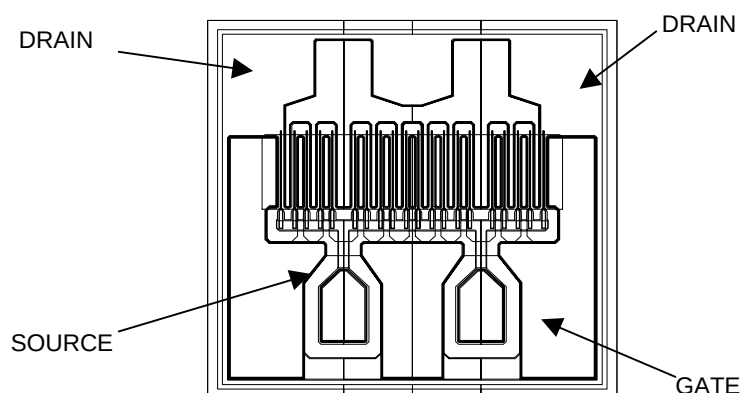


FEATURES

- +31.5 dBm Typical Power at 18 GHz
- 8.5 dB Typical Power Gain at 18 GHz
- +27 dBm at 3.3V Battery Voltage
- +45 dBm Typical Intercept Point
- 50% Power-Added-Efficiency at 18 GHz
- Plated Source Thru-Vias



DIE SIZE: 16.5 x 16.1 mils (420 x 410 μm)
 DIE THICKNESS: 3.0 mils (75 μm typ.)
 BONDING PADS: 1.9 x 2.4 mils (50 x 60 μm typ.)

DESCRIPTION AND APPLICATIONS

The LPV1500 is an Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 μm by 1500 μm Schottky barrier gate. The recessed "mushroom" gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for reliable high-power applications. The LPV1500 also features Si_3N_4 passivation and is available in a flanged ceramic package (P100). The LPV1500 features plated source thru-vias for improved performance.

Typical applications include commercial and military high-performance power amplifiers, including SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters. The LPV1500 may be procured in a variety of grades, depending upon specific user requirements. Standard lot screening is patterned after MIL-STD-19500, JANC grade. Space-level screening to FSS JANS grade is also available.

PERFORMANCE SPECIFICATIONS ($T_A = 25^\circ\text{C}$)

SYMBOLS	PARAMETERS	MIN	TYP	MAX	UNITS
I_{DSS}	Saturated Drain-Source Current $V_{DS} = 2V$ $V_{GS} = 0V$	375	490	600	mA
P_{1dB}	Output Power at 1dB Gain Compression $V_{DS} = 8.0V$, $I_{DS} = 50\% I_{DSS}$ $f = 18 \text{ GHz}$	30.0	31.5		dBm
G_{1dB}	Power Gain at 1dB Gain Compression $V_{DS} = 8.0V$, $I_{DS} = 50\% I_{DSS}$ $f = 18 \text{ GHz}$	6.5	8.5		dB
IP3	Output 3rd-Order Intercept Pt. $V_{DS} = 8V$, $I_{DS} = 40\% I_{DSS}$		45		dBm
η_{ADD}	Power-Added Efficiency		50		%
I_{MAX}	Maximum Drain-Source Current $V_{DS} = 2V$ $V_{GS} = +1V$		925		mA
G_M	Transconductance $V_{DS} = 2V$ $V_{GS} = 0V$	350	450		mS
V_P	Pinch-Off Voltage $V_{DS} = 2V$ $I_{DS} = 5mA$	-0.25	-1.2	-2.0	V
I_{GSO}	Gate-Source Leakage Current $V_{GS} = -5V$		10	75	μA
BV_{GS}	Gate-Source Breakdown Voltage $I_{GS} = 8mA$	-12	-15		V
BV_{GD}	Gate-Drain Breakdown Voltage $I_{GD} = 8mA$	-12	-16		V
Θ_J	Thermal Resistivity		45		$^\circ\text{C/W}$

DSS-041 WA

ABSOLUTE MAXIMUM RATINGS (25°C)		
SYMBOL	PARAMETER	RATING ¹
V _{DS}	Drain-Source Voltage	+12V
V _{GS}	Gate-Source Voltage	-5V
I _{DS}	Drain-Source Current	2 x I _{DSS}
I _G	Gate Current	70 mA
P _{IN}	RF Input Power	750 mW
T _{CH}	Channel Temperature	+175°C
T _{STG}	Storage Temperature	-65/175°C
P _T	Power Dissipation	3.33W ^{3,4}

RECOMMENDED CONTINUOUS OPERATING LIMITS		
SYMBOL	PARAMETER	RATING ²
V _{DS}	Drain-Source Voltage	+8V
V _{GS}	Gate-Source Voltage	-1V
I _{DS}	Drain-Source Current	0.8 x I _{DSS}
I _G	Gate Current	15 mA
P _{IN}	RF Input Power	300 mW
T _{CH}	Channel Temperature	+150°C
T _{STG}	Storage Temperature	-20/50°C
P _T	Power Dissipation	3.0 W ^{3,4}
G _{XdB}	Gain Compression	8 dB

NOTES:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Recommended Continuous Operating Limits should be observed for reliable device operation.
- Power Dissipation defined as: $P_T \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where: P_{DC} = DC bias power, P_{OUT} = RF output power, and P_{IN} = RF input power.
- Power Dissipation to be de-rated as follows:
- Specifications subject to change without notice.

Example #1:

V_{DS} = 8V, I_{DS} = 315 mA

P_{IN} = P_{OUT} = 0 dBm (quiescent condition):

P_T = P_{DC} = 2.52W

Max. continuous T_{HS} = 37°C

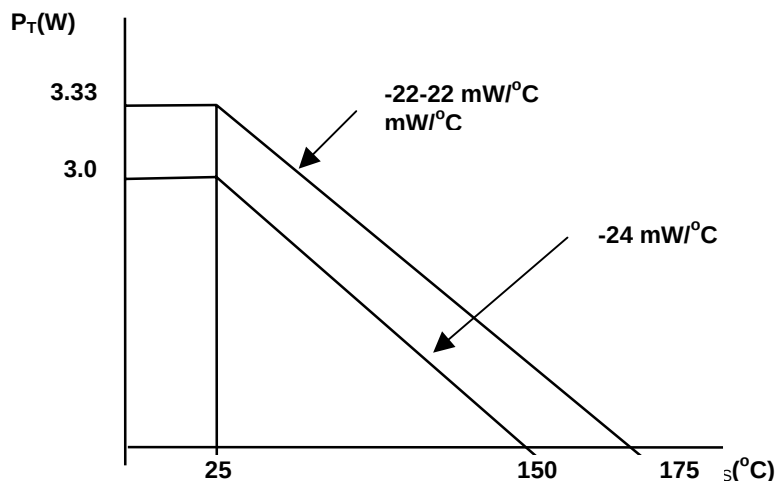
Example #2:

V_{DS} = 8V, I_{DS} = 315 mA

P_{IN} = 23 dBm P_{OUT} = 31 dBm

P_T = (2.52+0.2) - 1.26 = 1.46W

Max. continuous T_{HS} = 84°C


HANDLING PRECAUTIONS:

PHEMT chips should be stored in a dry nitrogen environment until assembly. Care should be exercised during handling to avoid damage to the devices. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500V), and further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

ASSEMBLY INSTRUCTIONS:

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is 1 min. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

APPLICATIONS NOTES AND DESIGN DATA:

Applications Notes are available from your local FSS Sales Representative, or directly from the factory. Complete design data, including S-parameters, Noise data, and Large-Signal models, is available on 3.5" diskette, or may be down-loaded from our Web Page.

DSS-041 WA