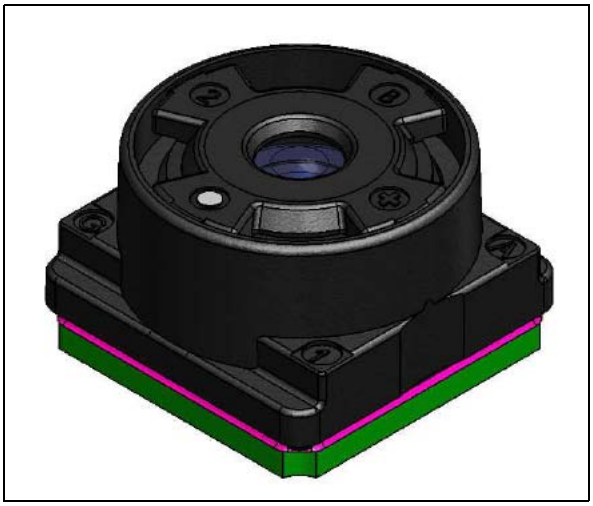
VS6663CD

1.3 megapixel camera module

Datasheet - production data



Features

- 1280 x 960 1.3 Mpixel resolution sensor
- Compact size: 6.5 mm x 6.5 mm x 4.1 mm
- Short focus distance: 15 cm
- MIPI CSI-2[(a)] (D-PHY v1.0) and CCP2 Video data interface
- Ultra low power standby mode (<15uW)
- Binning 2x2 mode
- Defect correction
- 4-channel lens shading correction

Description

The VS6663CD is a compact camera module designed for imaging and machine vision applications which require a short focus distance. It is designed to be used for high quality still camera function and also supports video modes. The camera silicon device is capable of generating raw Bayer 1.3 Mpixel images up to 30 fps. The VS6663CD supports the CCI control and CCP2 and CSI-2 data interfaces.

The module design is optimized for both footprint and height.

A separate hardware accelerator can be incorporated in the phone system to run the algorithms in hardware. The specification of these devices are contained in a separate document.

Table 1. Device summary

Order code	Package	Packing
VS6663CDQ05I/1	SMIA65	Tape and reel

a. Copyright© 2005 MIPI Alliance, Inc. Standard for Camera Serial Interface 2 (CSI-2) version 1.01, limited to 1 Gbps per lane

This is information on a product in full production. www.st.com

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1 Overview

The VS6663CD 1.3 Mpixel image sensor produces raw digital video data at up to 30 fps. It has both CCP2 and MIPI CSI-2 video data interfaces selectable over the camera control interface (CCI).

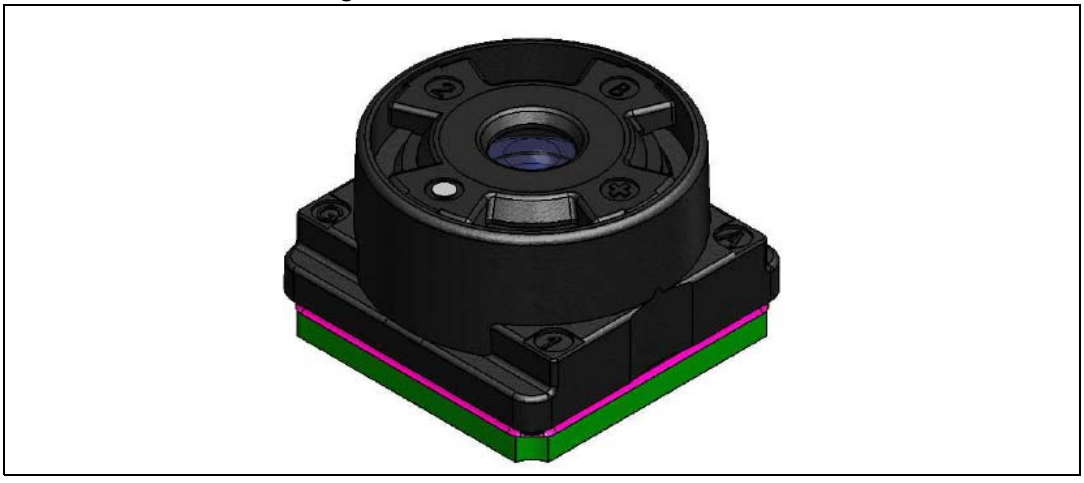
The image data is digitized using an internal 10-bit column ADC. The resulting 10-bit pixel data is output as 8-bit, 10-bit or 10-8 bit compressed data and includes checksums and embedded codes for synchronization. The interface conforms to both the CCP2 and MIPI CSI-2 interface standards. The sensor is fully configurable through a CCI serial interface.

The module is available in a SMOP type package measuring 6.5 mm x 6.5 mm x 4.1 mm. It is designed to be used with a board mounted socket or flex.

Table 2. Technical specification

Feature	Detail
Sensor technology	IMG140 ST's 65 nm based CMOS imaging process
Pixel size	1.75 µm x 1.75 µm
Analogue gain	24 dB (max)
Dynamic range	60 dB (typical)
Signal to noise	38 dB (typical)
SNR10 value	50 lux
Supply voltage	Analogue: 2.6 V to 2.9 V Digital: 1.68 V to 1.92 V
Average power consumption 30 fps	150 mW (typical)
Lens	51° HFOV F/2.8
TV distortion	<1%
System attach	Socket or flex

Figure 1. VS6663CD camera module

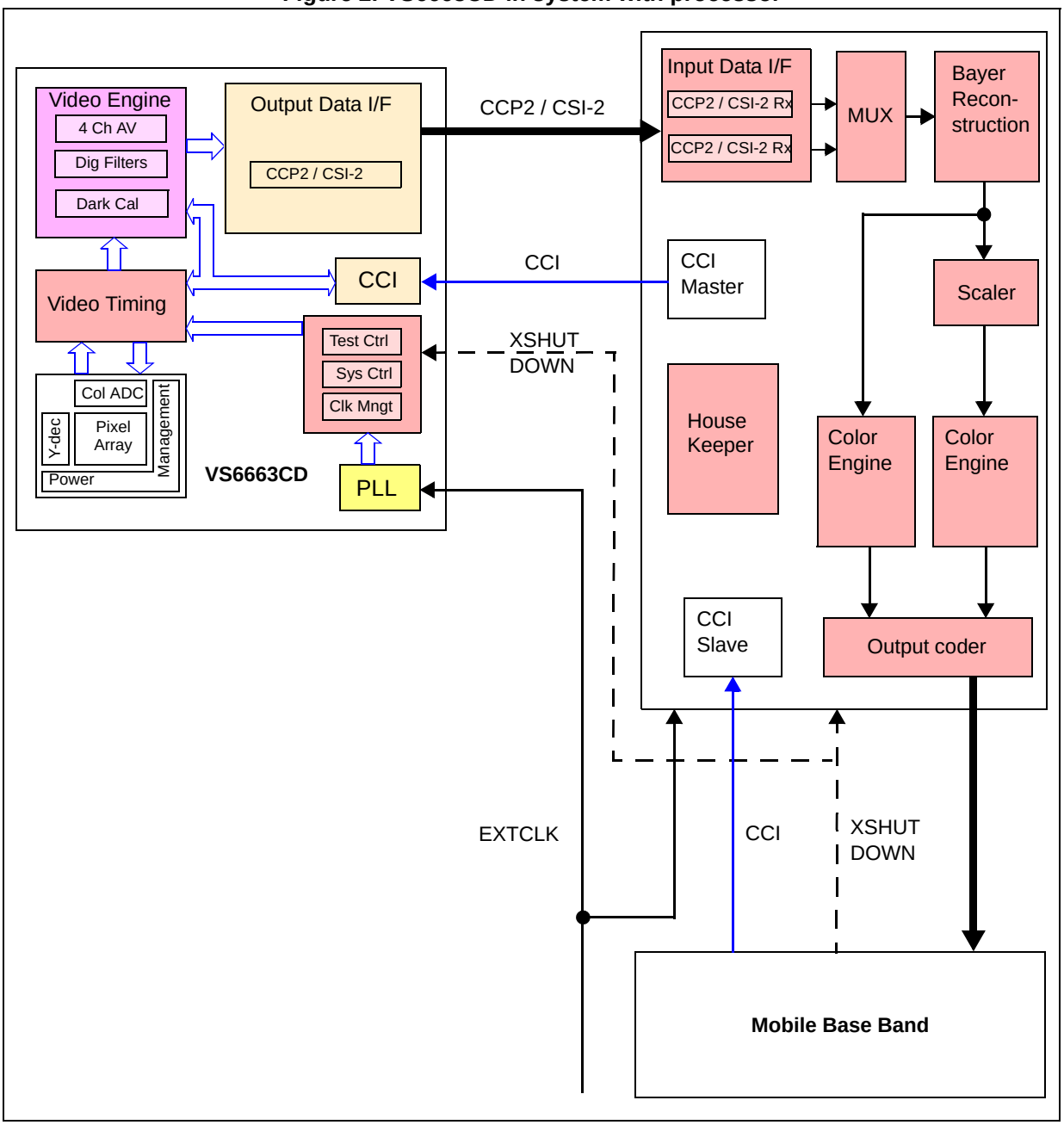


1.1 VS6663CD use in system with hardware coprocessor

The VS6663CD as an image sensor can be paired with an STMicroelectronics hardware accelerator. The coprocessor and the sensor together form a complete imaging system.

Figure 2 illustrates a typical system using VS6663CD.

Figure 2. VS6663CD in system with processor



The module's main function is to convert the viewed scene into a data stream. The companion processor's function is to manage the sensor included in the module in order to produce the best possible pictures given the module's optics and the scene itself. The companion processor processes the data stream into a form which is easily handled by up stream mobile baseband or multimedia processor (MMP) chipsets.

The sensor supplies high-speed clock signal to the coprocessor and provides the embedded control sequences which allow the coprocessor to synchronize with the frame and line level timings. The coprocessor then performs the color processing on the raw image data from the sensor before supplying the final image data to the host.

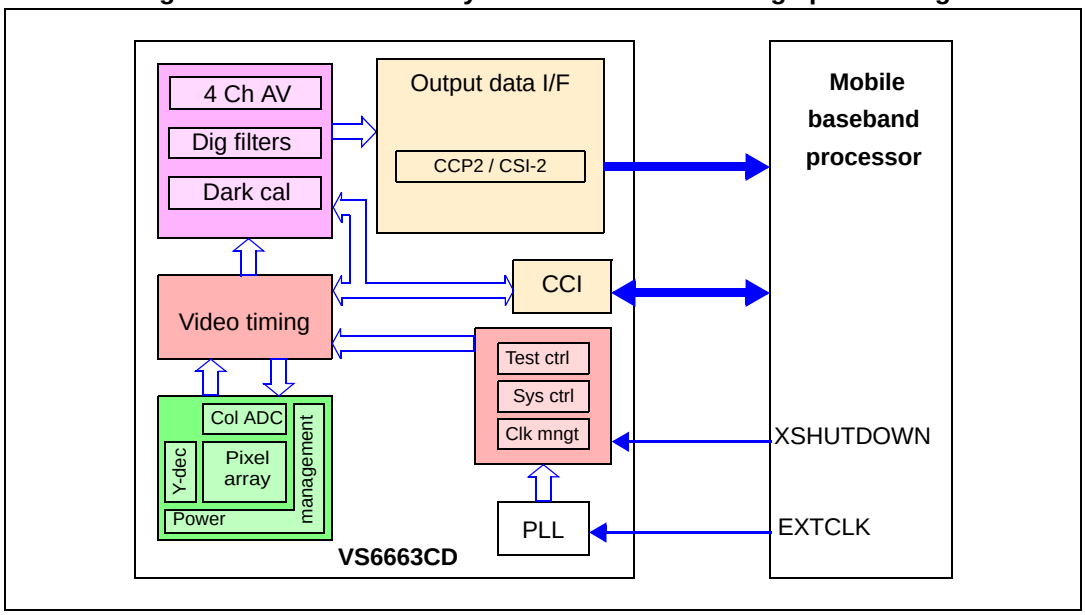
In a coprocessor architecture, a low speed clock (external clock) is sent by the host to both the VS6663CD and the coprocessor. This is used by the sensor in all phases of operation and by the coprocessor during the initial stages of system boot up.

During streaming phase, the VS6663CD supplies the high-speed data qualification clock for the coprocessor. The high-speed clock is generated using the VS6663CD embedded PLL and is provided as the continuous data qualification clock.

1.2 VS6663CD use in a system with software image processing

The VS6663CD image sensor can also be directly connected to a baseband or multimedia processor. No dedicated coprocessor is used in this configuration. The image processing is done in software within the baseband processor.

Figure 3. VS6663CD in a system with software image processing



1.3 Reference documents

Table 3. Reference documents

Title	Date
MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) v1.0	29-Nov-2005
MIPI Alliance D-PHY Specification (v1.00.00)	14-May-2009

2 Device pinout

Figure 4 shows the position of the pins on the module and *Table 4* provides the signal descriptions.

Figure 4. VS6663CD module pinout (viewed from bottom of camera module)

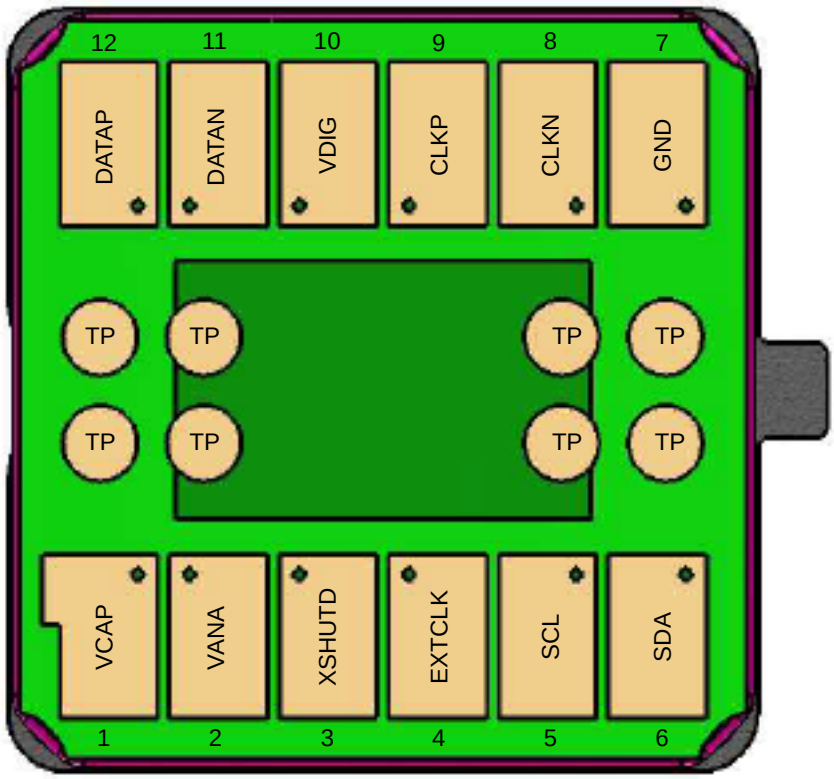


Table 4. Pin description

Pad number	Pad name	I/O type	Description
Power supplies			
1	VCAP	PWR	Do not connect(1)
7	GND	PWR	Ground (combined)
2	VANA	PWR	Analog power
10	VDIG	PWR	Digital power
System			
3	XSHUTDOWN	I	Power down control(2)
4	EXTCLK	I	System clock input
Control			
5	SCL	I	Serial communication clock

Table 4. Pin description (continued)

Pad number	Pad name	I/O type	Description
6	SDA	I/O	Serial communication data
Data			
8	CLK-	SubLVDS output	Output qualifying clock
9	CLK+	SubLVDS output	Output qualifying clock
11	DATA-	SubLVDS output	Serial output data
12	DATA+	SubLVDS output	Serial output data
ST test			
TP		ST test pins	Do not connect(3)

1. No connection should be made to VCAP.
2. Signal is active low.
3. Test pins are not floating.

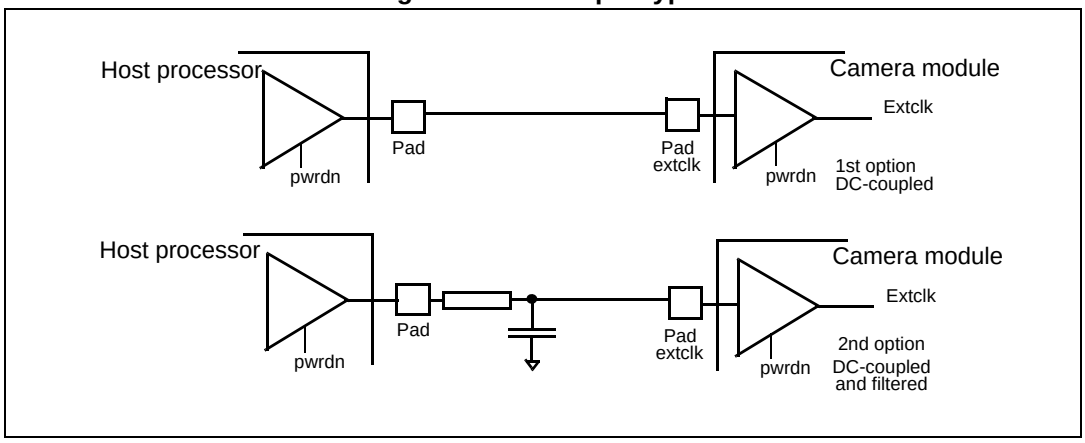
3 Functional description

3.1 External clock

3.1.1 Clock input type

The external clock provided by the host to the VS6663CD must be a DC coupled square wave and may also be RC-filtered.

Figure 5. Clock input types



3.1.2 PLL and clock input

The VS6663CD has an embedded PLL block. This block generates all necessary internal clocks from an input range defined in *Table 5*.

Table 5. System input clock frequency range

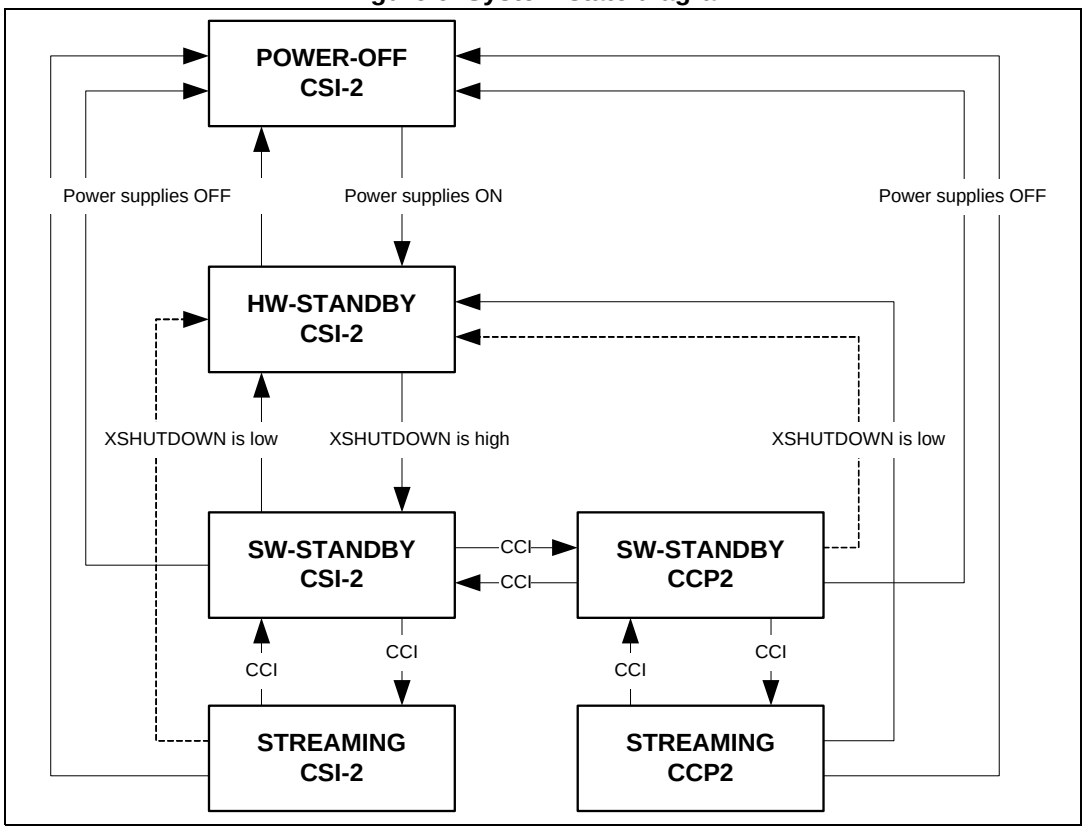
Minimum (MHz)	Maximum (MHz)
6	27

The value of the external clock frequency must be written to register 0x0136 (extclk_frequency_mhz).

3.2 Device operating modes

The mode changes in VS6663CD are shown in *Figure 6*. Further details are provided in the following sections.

Figure 6. System state diagram



3.2.1 Power-up procedure

The digital and analog supply voltages can be powered up in any order, for example, VDIG then VANA or VANA then VDIG.

On power-up the on-chip power-on reset cell ensures that the CCI register values are initialized correctly to their default values.

The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock.

The power-up sequence timing constraints are shown in *Table 6*.

Table 6. Power-up sequence timing constraints

Symbol	Parameter	Min.	Max.	Units
t0	VANA rising – VDIG rising	VANA and VDIG may rise in any order. The rising separation can vary from 0 ns to indefinite.		ns
t1	VDIG rising – VANA rising			ns
t2	VDIG / VANA rising – XSHUTDOWN rising	XSHUTDOWN must rise later than or coincident with the later rising supply (VDIG or VANA)		µs
t3	XSHUTDOWN – First I^2C transaction	2400	-	EXTCLK cycles
t4	Minimum number of EXTCLK cycles prior to the first I^2C transaction	2400	-	EXTCLK cycles
t5	PLL start up/lock time	-	1	ms
t6	Entering streaming mode – First frame start sequence (fixed part)	-		ms
t7	Entering streaming mode – First frame start sequence (variable part) = Integration time	The delay is the coarse integration time value.		

Figure 7. VS6663CD power-up sequence for CCP2

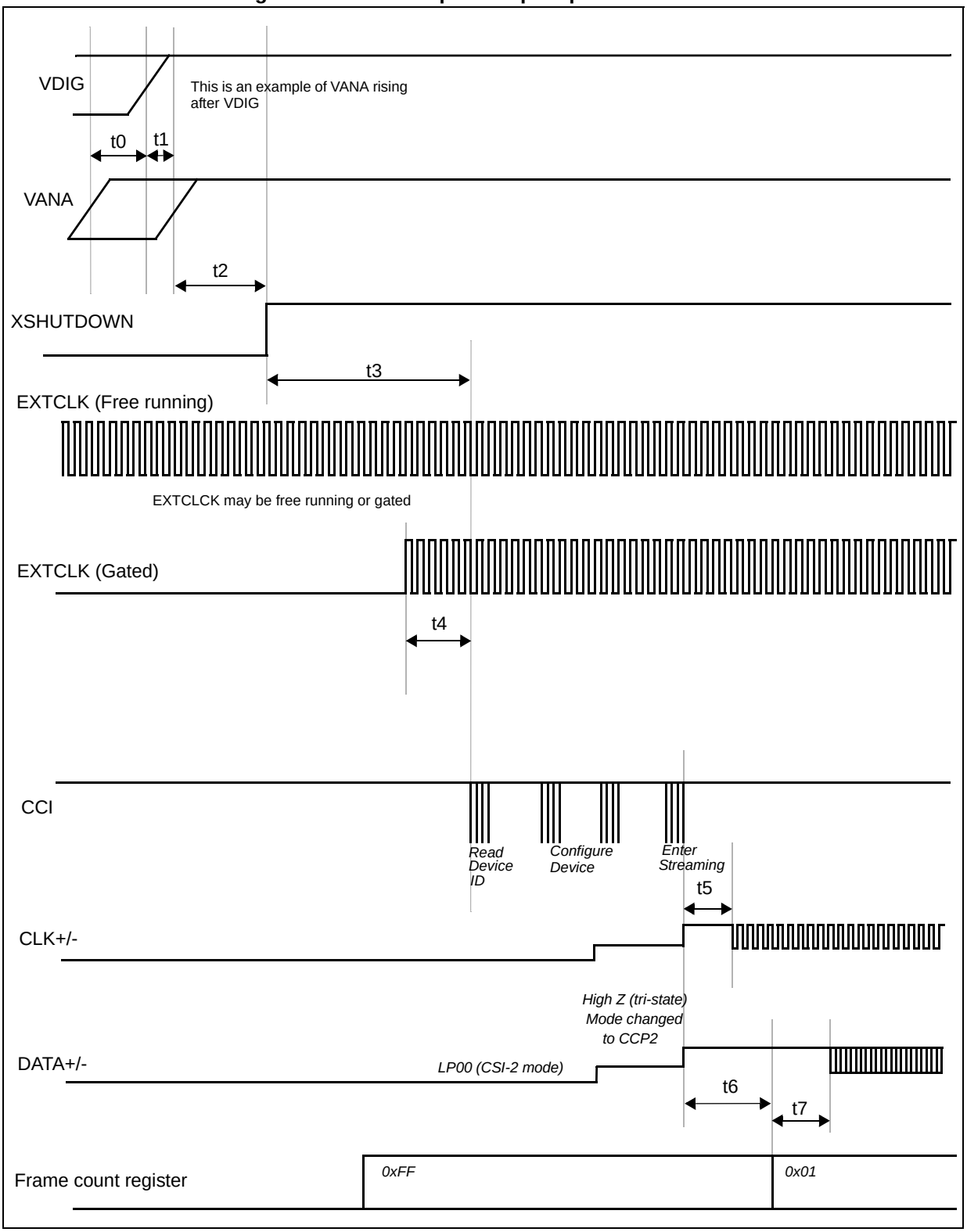
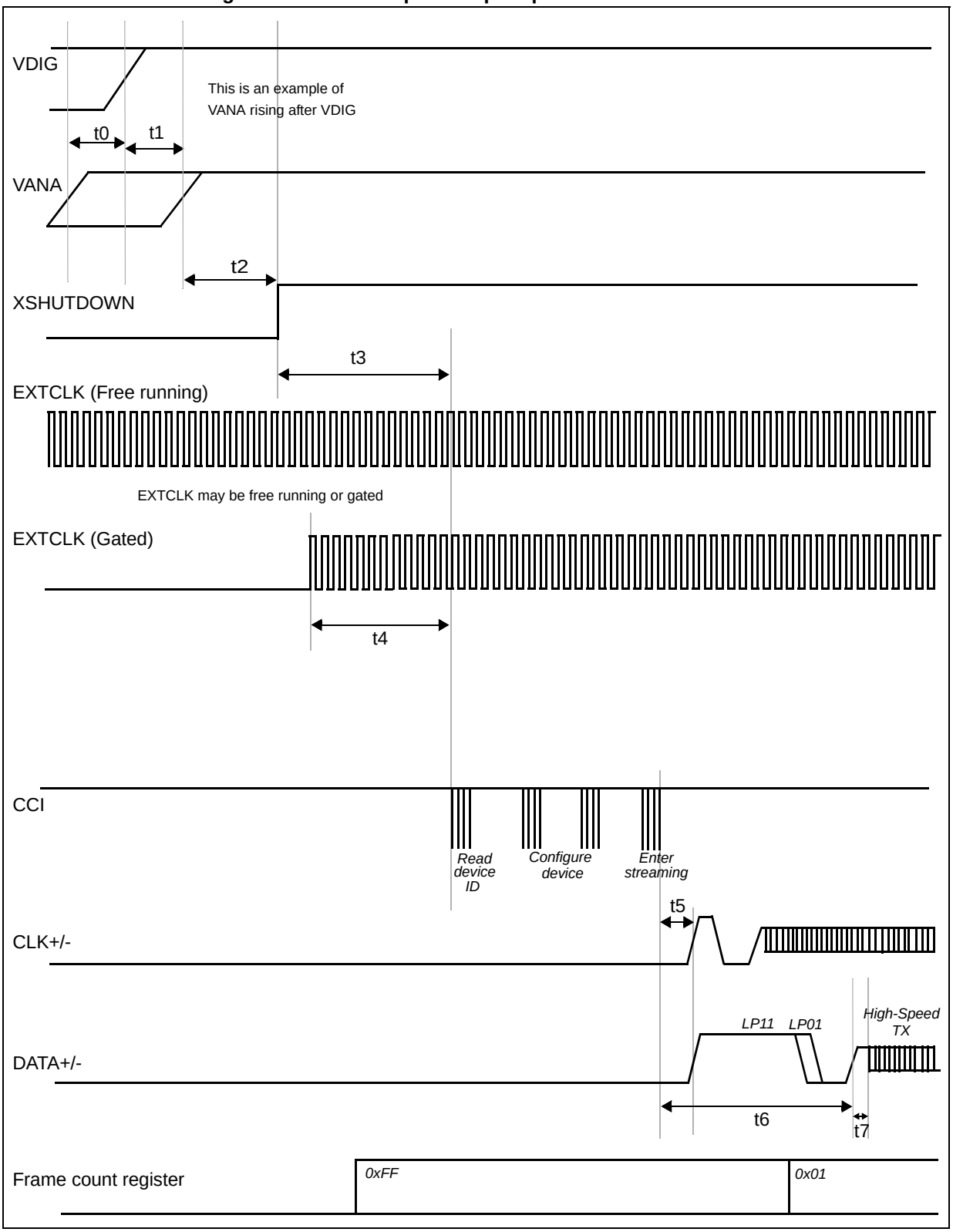


Figure 8. VS6663CD power-up sequence for CSI-2 mode



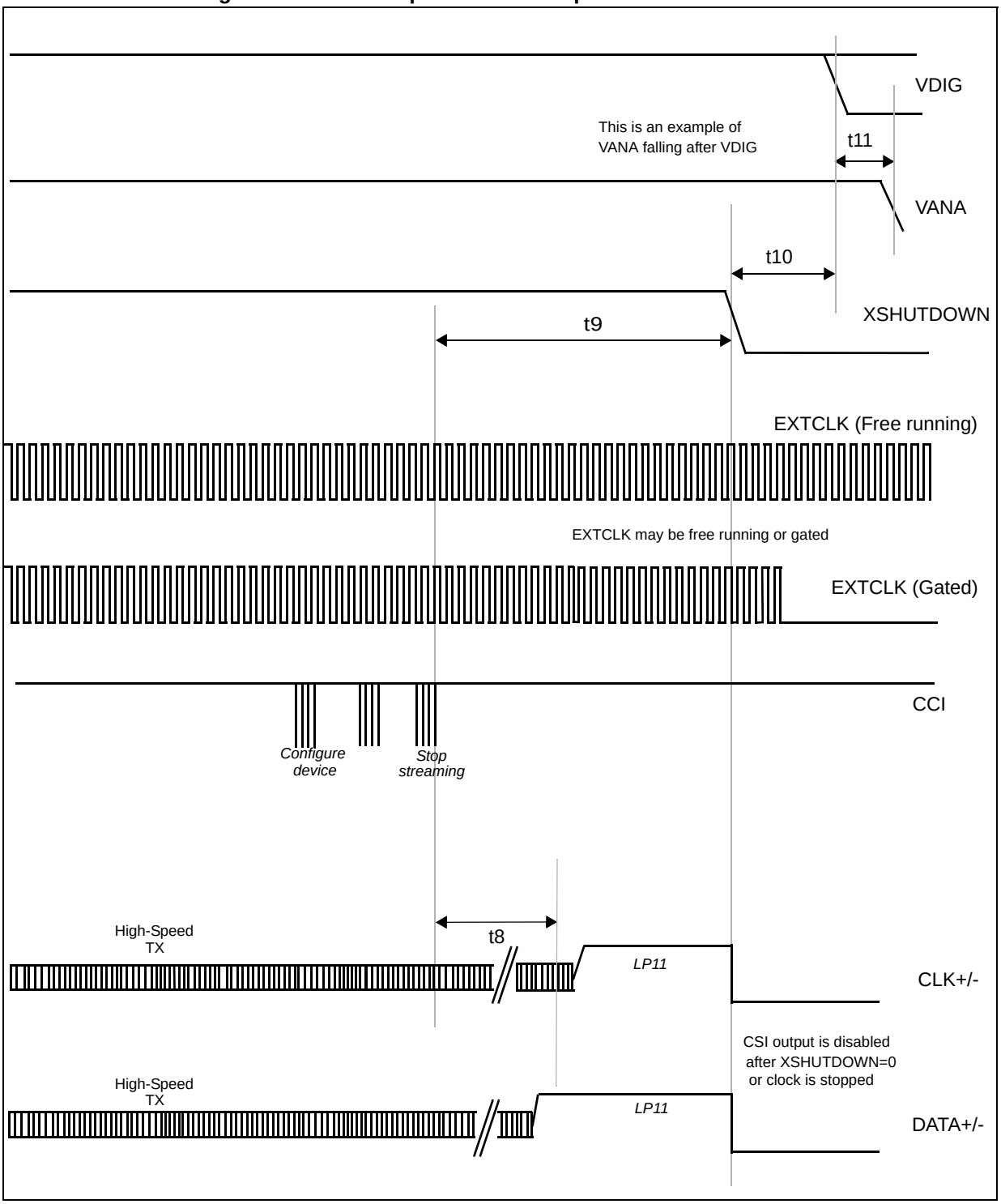
3.2.2 Power-down procedure

The power-down sequence timing constraints are shown in *Table 7*.

Table 7. Power-down sequence timing constraints for CSI2 communications

Symbol	Parameter	Minimum	Maximum	Units
t8	Last I^2C transaction to software standby	-	1 frame	
t9	Last I^2C transaction or MIPI frame end to XSHUTDOWN falling	512	-	clock cycles
t10	XSHUTDOWN to VANA/VDIG falling	XSHUTDOWN must fall at the same time as, or earlier than, both power supplies (VDIG and VANA)		
t11	VANA to VDIG or VDIG to VANA falling	VANA and VDIG may fall in any order, the rising separation can vary from 0 ns to indefinite		

Figure 9. VS6663CD power-down sequence for CSI-2 mode



3.2.3 Internal power-on reset (POR)

The VS6663CD internally performs a power-on reset (POR) when the digital supply rises through the trigger level, Vtrig_rising. Similarly, if the digital power supply falls through the trigger level, Vtrig_falling, then the power-on reset will also trigger.

Figure 10. POR timing

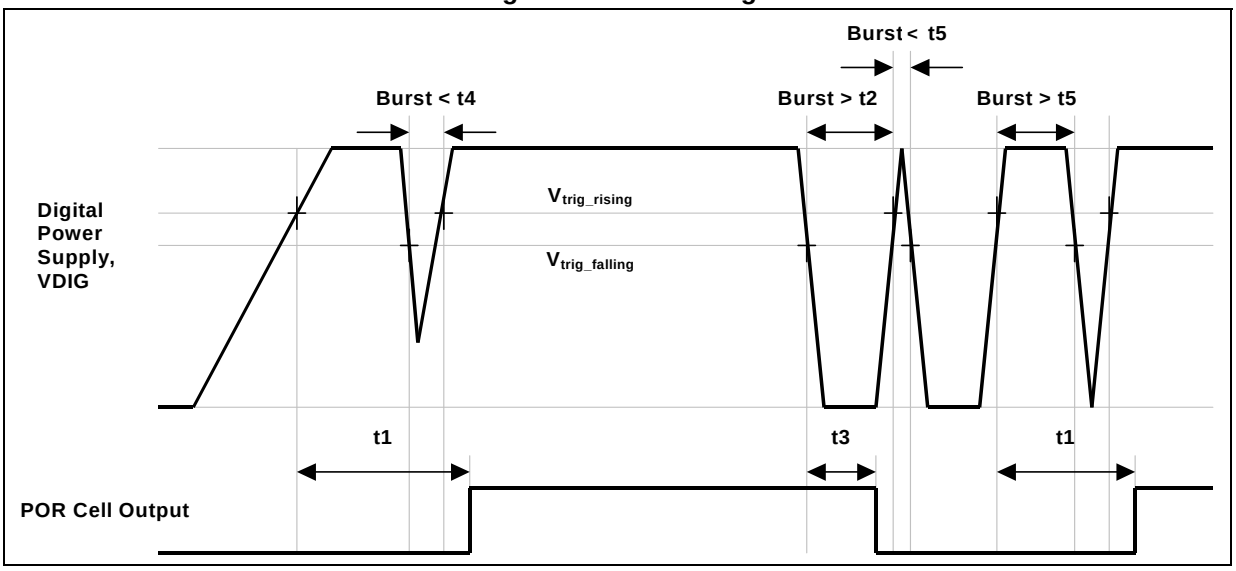


Table 8. POR cell characteristics

Symbol	Constraint	Minimum	Typical	Maximum	Units
t1	VDIG rising crossing Vtrig_rising – Internal reset being released.	20.7	30.7	50.7	µs
t2	Minimum VDIG spike width below Vtrig_falling which is considered to be a reset when POR cell output high.	1.25	2.1	6.9	µs
t3(1)	VDIG falling crossing Vtrig_falling - Internal reset active.	1.25	2.1	6.9	µs
t4	Minimum VDIG spike width below Vtrig_falling which is considered to be a reset when POR cell output low.	1.5	2.1	6.9	µs
t5	Minimum VDIG spike width above Vtrig_rising which is considered to be a supply is stable when POR cell output low. While the POR cell output is low, all VDIG spikes above Vtrig_rising which are less than t5 must be ignored.	20.7	30.7	50.7	ns
Vtrig_rising	VDIG rising trigger voltage.	429	755	944	mV
Vtrig_falling	VDIG falling trigger voltage.	401	725	904	mV

1. The device could be reset by any VDIG voltage excursion falling below Vtrig_falling and will always be reset by a VDIG voltage excursion below Vtrig_falling of > 0.5 µs

3.2.4 Power-off

The power-off state is defined as either or both of the digital and analog supplies not present.

3.2.5 Hardware standby

This is the lowest power consumption mode. CCI communications are not supported in this mode. The PLL and the video blocks are powered down. This state is entered by pulling the control pin XSHUTDOWN down (active low). All registers are returned to their default values

3.2.6 Software standby

Software standby mode preserves the contents of the CCI register map. CCI communications are supported in this mode. The software standby mode is selected using a serial interface command. If this state is entered from hardware standby the data pads remain high impedance. If this state is entered from streaming then the data pads go high impedance at the end of the current frame. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The values of the serial interface registers like exposure and gain are preserved. The system clock must remain active when communicating with the sensor.

This state is entered by releasing the device from hard reset by setting XSHUTDOWN high, writing 0x00 to the mode control register (0x0100) or commanding a soft reset by writing 0x01 to the software reset register (0x0103).

Note: After a soft reset or the transition of XSHUTDOWN to high, all registers are returned to their default values.

3.2.7 Streaming

The VS6663CD streams live video. This mode is entered by writing 0x01 to the mode control register (0x0100).

3.2.8 Dark calibration algorithm

VS6663CD runs an automatic dark calibration algorithm on the raw image data to control the video offsets caused by dark current. This ensures that a high quality image is output over a range of operating conditions. First frame dark level is correctly calibrated, for subsequent frames the adjustment of the dark level is damped by a leaky integrator function to avoid possible frame to frame flicker.

4 Camera control interface (CCI)

This chapter specifies the camera control interface (CCI). The I^2C-type interface uses 1.8 V I/O with two signals: serial data line (SDA) and serial clock line (SCL). CCI is used for control data transfer. Clock signal (SCL) generation is performed by the master device (the camera module is a slave device). The master device initiates data transfer. The CCI bus on the camera module has a maximum speed of 400 Kbits/s and has a software switchable device address.

Any internal register that can be written to, can also be read from. There are also read only registers that contain device status information, (for example, design revision details). A read instruction from an un-used register location will return the value 0x00. A read instruction from the manufacturers specific registers may return any value. A write instruction to a reserved or unused register location is illegal and the effect of such a write is undefined. It is the responsibility of the host system to only write to register locations which have been defined.

4.1 Valid register data types

The contents of the registers can represent a number of different data types (see *Table 9*). The register map uses this coding to help with the interpretation of the contents of each register.

Table 9. Valid register data types

Data type	Name	Range	Description
8UI	8-bit unsigned integer	0 to 255	-
8SI	8-bit signed integer	-128 to 127	Two’s complement notation
16UI	16-bit unsigned integer	0 to 65535	-
16SI	16-bit signed integer	-32768 to 32767	Two’s complement notation
16UR	16-bit unsigned iReal	0 to 255.99609375	08.08 fixed point number. 8 integer bits (MS Byte), 8 fractional bits (LS Byte)
16SR	16-bit signed iReal	-128 to 127.9960375	Two’s complement notation, 8 fractional bits
32SF	32-bit IEEE floating-point number	As per IEEE 754	As per IEEE 754. 1 sign bit, 8 exponent bits, 23 fractional bits
8C or 16C	8-bit or 16-bit Coded	-	This indicates that the value is decoded to select one of several functions or modes.
8B or 16B	8 or 16 Bits	-	Each bit represents a specific function or mode.

4.2 Register map

4.2.1 General status registers [0x0000 to 0x001F]

Table 10. General status registers [0x0000 to 0x001F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0000	Hi	model_id	16UI	02.97	RO	Camera model identification 0x0297 = 663_{10}
0x0001	Lo					
0x0002		revision_number_major	8UI	04	RO	Revision identifier of the camera
0x0003		manufacturer_id	8C	01	RO	Manufacturer ID: ST Micro
0x0004		smia_version	8C	0A	RO	0x0A: SMIA 1.0
0x0005		frame_count	8UI	FF	RO	Frame count increments from 1 to 254 when streaming. When moving from video to sleep the frame count is reset to 255. The frame count is also reset to 255 after a soft reset (register 0x0103).
0x0006		pixel_order	8C	00	RO	Color pixel readout order. Defines the order of the color pixel readout. Changes with mirror and flip (register 0x0101). 0x00 - GR/BG - normal 0x01 - RG/GB - horizontal mirror 0x02 - BG/GR - vertical flip 0x03 - GB/RG - vertical flip and horizontal mirror
0x0008	Hi	data_pedestal	16UI	00.40	RO	The video data is offset by 64
0x0009	Lo					
0x000C		pixel_depth	8UI	0A	RO	Pixel data resolution. For VS6663CD the pixel depth is 10 bits.

4.2.2 Frame format description registers [0x0040 to 0x007F]

For a full description of the frame format description refer to *Chapter 5: Video data interface on page 36*.

Table 11. Frame format description registers [0x0040 to 0x007F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0040		frame_format_model_type	8C	01	RO	Generic frame format. 0x01: 2-byte data format.
0x0041		frame_format_model_subtype	8C	12	RO	Contains the number of 2-byte data format descriptors used. Upper nibble defines the number of column descriptors (1). The lower nibble defines the number of row descriptors (2)
0x0042	Hi	frame_format_descriptor_0	16C	55.10	RO	Pixel data code: 5 (Visible Columns) Number of pixels : readout dependent (Maximum of 1296) Number of pixels: 1296
0x0043	Lo					
0x0044	Hi	frame_format_descriptor_1	16C	10.02	RO	Pixel data code: 1 (Embedded data lines) Number of status lines:2
0x0045	Lo					
0x0046	Hi	frame_format_descriptor_2	16C	53.D0	RO	Pixel data code: 5 (Visible Lines) number of pixels: readout dependent (Maximum of 976) Number of pixels: 976
0x0047	Lo					

4.2.3 Analog gain description registers [0x0080 to 0x0093]

For a full description of the analog gain description registers refer to *Chapter 6: Video timing on page 39*.

Table 12. Analog gain description [0x0080 to 0x0093]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0080	Hi	analogue_gain_capability	16B	00.00	RO	Analog gain capability 0 – single global analog gain only
0x0081	Lo					
0x0084	Hi	analogue_gain_code_min	16UI	00.00	RO	Minimum recommended analog gain code, that is, 0 (x1 gain)
0x0085	Lo					
0x0086	Hi	analogue_gain_code_max	16UI	00.F0	RO	Maximum recommended analog gain code, that is, 240 (x16 gain)
0x0087	Lo					
0x0088	Hi	analogue_gain_code_step	16UI	00.10	RO	Analog gain code step size
0x0089	Lo					

Table 12. Analog gain description [0x0080 to 0x0093] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x008A	Hi	analogue_gain_type	16UI	00.00	RO	Analog gain type
0x008B	Lo					
0x008C	Hi	analogue_gain_m0	16SI	00.00	RO	Analog gain m0 constant. m0 = 0
0x008D	Lo					
0x008E	Hi	analogue_gain_c0	16SI	01.00	RO	Analog gain c0 constant. c0 = 256
0x008F	Lo					
0x0090	Hi	analogue_gain_m1	16SI	FF.FF	RO	Analog gain m1 constant. m1 =-1
0x0091	Lo					
0x0092	Hi	analogue_gain_c1	16SI	01.00	RO	Analog gain c1 constant c1 = 256
0x0093	Lo					

4.2.4 Data format description registers [0x00C0 to 0x00C7]

Table 13. Data format description registers [0x00C0 to 0x00C7]

Index	Byte	Register name	Data type	Default	Type	Comment
0x00C0		data_format_model_type	8UI	01	RO	2-byte generic data format model. Always 0x01
0x00C1		data_format_model_subtype	8UI	03	RO	Number of descriptors, that is, 3
0x00C2	Hi	data_format_descriptor_0	16UI	08.08	RO	Top 8-bits of internal pixel data transmitted as RAW8.
0x00C3	Lo					
0x00C4	Hi	data_format_descriptor_1	16UI	0A.0A	RO	Top 10-bits of internal pixel data transmitted as RAW 10.
0x00C5	Lo					
0x00C6	Hi	data_format_descriptor_2	16UI	0A.08	RO	Compress top 10-bits of internal pixel data to 8. Transmitted as RAW 8 mode.
0x00C7	Lo					

4.2.5 Setup registers [0x0100 to 0x01FF]

Table 14. Setup registers [0x0100 to 0x01FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0100		mode_select	8UI	00	RW	Mode select 0x00 - Software standby 0x01 - Streaming Refer to *Section 3.2: Device operating modes on page 14*
0x0101		image_orientation	8B	00	RW	Image orientation, that is, horizontal mirror and vertical flip. Bit 0: 0 - no mirror, 1 - horizontal mirror enable Bit 1: 0 - no flip, 1 - vertical flip enable
0x0103		software_reset	8UI	00	RW	Software reset. Setting this register to 1 resets the sensor to its power up defaults. The value of this bit is also reset 0x00 - normal 0x01 - soft reset Refer to *Section 3.2: Device operating modes on page 14*
0x0104		grouped_parameter_hold	8UI	00	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0x00 - consume parameters as normal 0x01 - hold parameters Refer to *Section 6.3.3: Integration and gain parameter retiming on page 46*
0x0105		mask_corrupted_frames	8UI	00	RW	Setting this register to 1 prevents the sensor outputing frames that have been corrupted by video timing parameter changes. 0x00 - normal 0x01 - mask corrupted frames
0x0110		csi_channel_identifier	8UI	00	RW	The DMA (CCP2) or Virtual (CSI2) channel identifier Valid range: 0-7 for CCP2 Valid range: 0-3 for CSI-2
0x0111		csi_signalling_mode	8UI	02	RW	0x00 - CCP2 Data/clock signalling: 0x01 - CCP2 Data/strobe signalling: 0x02 - CSI-2: This register should not be changed while the device is streaming data.

Table 14. Setup registers [0x0100 to 0x01FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0112	Hi	csi_data_format	16UI	0A.0A	RW	The MSB contains the bit width of the uncompressed pixel data. The LSB contains the bit width of the compressed pixel data. 0A.0A - RAW10 mode 0A.08 - 10-8 compressed mode 08.08 - RAW8 mode
0x0113	Lo					
0x0114		csi_lane_mode	8UI	00	RW	Number of data lanes in use 00 - 1-lane
0x0115		csi2_10_to_8_dt	8UI	30	RW	CSI-2 data type for 10-8 compression
0x0120		gain_mode	8UI	00	RO	0x00 – Global analog gain. VS6663CD supports only global gain modes.
0x0136	Hi	extclk_frequency_mhz	8.8UR	06.00	RW	Frequency of external crystal
0x0137	Lo					

4.2.6 Integration time and gain registers [0x0200 to 0x02FF]

These registers are used to control the image exposure. See *Section 6.3: Exposure and gain control on page 45* for more information.

Table 15. Integration time and gain registers [0x0200 to 0x02FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0200	Hi	fine_integration_time	16UI	01.4C	RW	Fine integration time (pixels)
0x0201	Lo					
0x0202	Hi	coarse_integration_time	16UI	00.00	RW	coarse integration time (lines).
0x0203	Lo					
0x0204	Hi	analogue_gain_code_global	16UI	00.00	RW	Global analog gain parameter (coded). See *Section 6.3.1: Gain model on page 45* for details of how to use this parameter.
0x0205	Lo					
0x020E	Hi	digital_gain_greenr	16UR	01.00	RW	Gain code for greenr channel
0x020F	Lo					
0x0210	Hi	digital_gain_red	16UR	01.00	RW	Gain code for red channel
0x0211	Lo					
0x0212	Hi	digital_gain_blue	16UR	01.00	RW	Gain code for blue channel
0x0213	Lo					
0x0214	Hi	digital_gain_greenb	16UR	01.00	RW	Gain code for greenb channel
0x0215	Lo					

4.2.7 Video timing registers [0x0300 to 0x03FF]

For a full description of the video timing registers refer to *Chapter 6: Video timing on page 39*.

Table 16. Video timing registers [0x0300 to 0x03FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0300	Hi	vt_pix_clk_div	16UI	00.0A	RW	Video timing clock divider Value: 10
0x0301	Lo					
0x0302	Hi	vt_sys_clk_div	16UI	00.01	RW	Video timing clock divider Value: 1
0x0303	Lo					
0x0304	Hi	pre_pll_clk_div	16UI	00.01	RW	Pre PLL clock divider value Value: 1
0x0305	Lo					
0x0306	Hi	pll_multiplier	16UI	00.85	RW	PLL multiplier value Value: 133
0x0307	Lo					
0x0340	Hi	frame_length_lines	16UI	03.F0	RW	Frame length Units: Lines Value: 1008
0x0341	Lo					
0x0342	Hi	line_length_pck	16UI	0A.50	RW	Line length Units: Pixel clocks Value: 2640
0x0343	Lo					
0x0344	Hi	x_addr_start	16UI	00.00	RW	X-address of the top left corner of the visible pixel data Units: Pixels Value: 0
0x0345	Lo					
0x0346	Hi	y_addr_start	16UI	00.00	RW	Y-address of the top left corner of the visible pixel data. **Must be** modulo 4 for correct operation of device. Units: Lines Value: 0
0x0347	Lo					
0x0348	Hi	x_addr_end	16UI	05.0F	RW	X-address of the bottom right corner of the visible pixel data Units: Pixels Value: 1295
0x0349	Lo					
0x034A	Hi	y_addr_end	16UI	03.CF	RW	Y-address of the bottom right corner of the visible pixel data Units: Lines Value = 975
0x034B	Lo					
0x034C	Hi	x_output_size	16UI	05.10	RW	Width of image data output from the sensor module Units: Pixels Value: 1296
0x034D	Lo					

Table 16. Video timing registers [0x0300 to 0x03FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x034E	Hi	y_output_size	16UI	03.D0	RW	Height of image data output from the sensor module Units: Lines Value: 976
0x034F	Lo					
0x0380	Hi	x_even_inc	16UI	00.01	RW	Increment for even pixels Units: Pixels
0x0381	Lo					
0x0382	Hi	x_odd_inc	16UI	00.01	RW	Increment for odd pixels Units: Pixels
0x0383	Lo					
0x0384	Hi	y_even_inc	16UI	00.01	RW	Increment for even pixels Units: Pixels
0x0385	Lo					
0x0386	Hi	y_odd_inc	16UI	00.01	RW	Increment for odd pixels Units: Pixels
0x0387	Lo					

4.2.8 Image compression registers [0x0500 to 0x0501]

Table 17. Image compression registers [0x0500 to 0x0501]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0500	Hi	compression_mode	16UI	00.01	RO	1 – DPCM/PCM compression (simple predictor)
0x0501	Lo					

4.2.9 Test pattern registers [0x0600 to 0x0611]

Table 18. Test pattern registers [0x0600 to 0x0611]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0600	Hi	test_pattern_mode	16C	00.00	RW	0 – normal operation (default) 1 – solid color bars 2 – 100% color bars 3 – fade to grey' color bars 4 - PN9 5 to 255 - reserved 256 to 65535 - manufacturer specific
0x0601	Lo					
0x0602	Hi	test_data_red	16UI	00.00	RW	The test data used to replace red pixel data. Range 0 to 1023.(1)
0x0603	Lo					
0x0604	Hi	test_data_greenR	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have red pixels. Valid range 0 to 1023.(1)
0x0605	Lo					

Table 18. Test pattern registers [0x0600 to 0x0611] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0606	Hi	test_data_blue	16UI	00.00	RW	The test data used to replace blue pixel data. Range 0 to 1023.(1)
0x0607	Lo					
0x0608	Hi	test_data_greenB	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have blue pixels. Range 0 to 1023.(1)
0x0609	Lo					
0x060A	Hi	horizontal_cursor_width	16UI	00.00	RW	Defines the width of the horizontal cursor (in pixels).
0x060B	Lo					
0x060C	Hi	horizontal_cursor_position	16UI	00.00	RW	Defines the top edge of the horizontal cursor.
0x060D	Lo					
0x060E	Hi	vertical_cursor_width	16UI	00.00	RW	Defines the width of the vertical cursor (in pixels).
0x060F	Lo					
0x0610	Hi	vertical_cursor_ position	16UI	00.00	RW	Defines the left hand edge of the vertical cursor. Maximum value = 0xFFFF A value of 0xFFFF switches the vertical cursor into automatic mode where it automatically advances every frame.
0x0611	Lo					

1. Some clipping of these values may occur to prevent false sync codes being generated

4.2.10 Binning registers [0x0900 to 0x0902]

Table 19. Binning registers [0x0900 to 0x0902]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0900		binning_mode	8UI	00	RW	Binning mode 0 - Disable 1 - Enable

4.2.11 Integration time and gain parameter limit registers [0x1000 to 0x10FF]

These registers are used to define exposure limits for the integration control registers (0x200 - 0x203). See *Section 6.3: Exposure and gain control on page 45* for more information.

Table 20. Integration time and gain parameter limit registers [0x1000 to 0x10FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1000	Hi	integration_time_capability	16UI	00.01	RO	This device supports coarse and fine integration.
0x1001	Lo					
0x1004	Hi	coarse_integration_time_min	16UI	00.00	RO	Minimum coarse integration time. Line periods.
0x1005	Lo					
0x1006	Hi	coarse_integration_time_max_margin	16UI	00.07	RO	Current frame length – current max coarse exposure. Line periods.
0x1007	Lo					
0x1008	Hi	fine_integration_time_min	16UI	01.4C	RO	Minimum fine integration time. 332 pixel periods.
0x1009	Lo					
0x100A	Hi	fine_integration_time_max_margin	16UI	06.DF	RO	Current line length - current max fine exposure. 1759 pixel periods.
0x100B	Lo					
0x1080	Hi	digital_gain_capability	16UI	00.01	RO	VS6663CD supports digital gain
0x1081	Lo					
0x1084	Hi	digital_gain_min	16UR	00.01	RO	0.0039 minimum
0x1085	Lo					
0x1086	Hi	digital_gain_max	16UR	01.FF	RO	1.996 maximum
0x1087	Lo					
0x1088	Hi	digital_gain_step_size	16UR	00.01	RO	0.0039 step size
0x1089	Lo					

4.2.12 Video timing parameter limit registers [0x1100 to 0x11FF]

For a full description of the video timing parameter limit registers refer to *Chapter 6: Video timing on page 39*.

Table 21. Video timing parameter limit registers [0x1100 to 0x11FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1100	Hi	min_ext_clk_freq_mhz	32SF	40.C0 00.00	RO	Minimum external clock frequency Units: MHz Value: 6.0
0x1101	3rd					
0x1102	2nd					
0x1103	Lo					
0x1104	Hi	max_ext_clk_freq_mhz	32SF	41.D8 00.00	RO	Maximum external clock frequency Units: MHz Value: 27.0
0x1105	3rd					
0x1106	2nd					
0x1107	Lo					
0x1108	Hi	min_pre_pll_clk_div	16UI	00.01	RO	Minimum Pre PLL divider value Value: 1
0x1109	Lo					
0x110A	Hi	max_pre_pll_clk_div	16UI	00.04	RO	Maximum Pre PLL divider value Value: 4
0x110B	Lo					
0x110C	Hi	min_pll_ip_freq_mhz	32SF	40.C0 00.00	RO	Minimum PLL input clock frequency Units: MHz Value: 6.0
0x110D	3rd					
0x110E	2nd					
0x110F	Lo					
0x1110	Hi	max_pll_ip_freq_mhz	32SF	41.40 00.00	RO	Maximum PLL input clock frequency Units: MHz Value: 12.0
0x1111	3rd					
0x1112	2nd					
0x1113	Lo					
0x1114	Hi	min_pll_multiplier	16UI	00.19	RO	Minimum PLL multiplier Value: 25
0x1115	Lo					
0x1116	Hi	max_pll_multiplier	16UI	00.85	RO	Maximum PLL multiplier Value: 133
0x1117	Lo					
0x1118	Hi	min_pll_op_freq_mhz	32SF	43.96 00.00	RO	Minimum PLL output clock frequency Units: MHz Value: 300.0
0x1119	3rd					
0x111A	2nd					
0x111B	Lo					

Table 21. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x111C	Hi	max_pll_op_freq_mhz	32SF	44.48 00.00	RO	Maximum PLL output clock frequency Units: MHz Value: 800.0
0x111D	3rd					
0x111E	2nd					
0x111F	Lo					
0x1120	Hi	min_vt_sys_clk_div	16UI	00.01	RO	Minimum video-timing system clock divider value Value: 1
0x1121	Lo					
0x1122	Hi	max_vt_sys_clk_div	16UI	00.04	RO	Maximum video-timing system clock divider value Value: 4
0x1123	Lo					
0x1124	Hi	min_vt_sys_clk_freq_mhz	32SF	42.96 00.00	RO	Minimum video-timing system clock frequency Units: MHz Value: 75.0 This value is 80 MHz in CSI2 mode.
0x1125	3rd					
0x1126	2nd					
0x1127	Lo					
0x1128	Hi	max_vt_sys_clk_freq_mhz	32SF	44.48 00.00	RO	Maximum video-timing system clock frequency Units: MHz Value: 800.0 The maximum value is 640 MHz in CCP mode.
0x1129	3rd					
0x112A	2nd					
0x112B	Lo					
0x112C	Hi	min_vt_pix_clk_freq_mhz	32SF	40.F0 00.00	RO	Minimum video-timing pixel clock frequency Units: MHz Value: 7.5
0x112D	3rd					
0x112E	2nd					
0x112F	Lo					
0x1130	Hi	max_vt_pix_clk_freq_mhz	32SF	42.A0 00.00	RO	Maximum video-timing pixel clock frequency Units: MHz Value: 80.0
0x1131	3rd					
0x1132	2nd					
0x1133	Lo					
0x1134	Hi	min_vt_pix_clk_div	16UI	00.08	RO	Minimum video-timing pixel clock divider Value: 8
0x1135	Lo					
0x1136	Hi	max_vt_pix_clk_div	16UI	00.0A	RO	Maximum video-timing pixel clock divider Value: 10
0x1137	Lo					
0x1140	Hi	min_frame_length_lines	16UI	00.D0	RO	Minimum frame length allowed. Value = 208 Units: Lines
0x1141	Lo					

Table 21. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x1142	Hi	max_frame_length_lines	16UI	FF.FF	RO	Maximum possible number of lines per frame. Value = 65535 Units: Lines
0x1143	Lo					
0x1144	Hi	min_line_length_pck	16UI	0A.50	RO	Minimum line length allowed. Value = 2640 Units: Pixel clocks
0x1145	Lo					
0x1146	Hi	max_line_length_pck	16UI	3F.FF	RO	Maximum possible number of pixel clocks per line. Value = 16383 Units: Pixel clocks
0x1147	Lo					
0x1148	Hi	min_line_blanking_pck	16UI	05.30	RO	Minimum line blanking time in pixel clocks Value = 1328 Units: Pixel clocks
0x1149	Lo					
0x114A	Hi	min_frame_blanking_lines	16UI	00.0E	RO	Minimum frame blanking in video lines = 14
0x114B	Lo					
0x114C	Hi	min_linelength_pck_step_size	16UI	00.01	RO	Minimum step size of line length pck
0x114D	Lo					
0x1180	Hi	x_addr_min	16UI	00.00	RO	Minimum X-address of the addressable pixel array Value: Always 0
0x1181	Lo					
0x1182	Hi	y_addr_min	16UI	00.00	RO	Minimum Y-address of the addressable pixel array Value: Always 0
0x1183	Lo					
0x1184	Hi	x_addr_max	16UI	05.0F	RO	Maximum X-address of the addressable pixel array Value = 1295
0x1185	Lo					
0x1186	Hi	y_addr_max	16UI	03.CF	RO	Maximum Y-address of the addressable pixel array Value = 975
0x1187	Lo					
0x1188	Hi	min_x_output_size	16UI	01.00	RO	Minimum x output size in pixels. Value: 256
0x1189	Lo					
0x118A	Hi	min_y_output_size	16UI	00.C0	RO	Minimum y output size in pixels. Value: 192
0x118B	Lo					
0x118C	Hi	max_x_output_size	16UI	05.10	RO	Maximum x output size in pixels. Value: 1296
0x118D	Lo					
0x118E	Hi	max_y_output_size	16UI	03.D0	RO	Maximum y output size in pixels: Value: 976
0x118F	Lo					

Table 21. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x11C0	Hi	min_even_inc	16UI	00.01	RO	Minimum Increment for even pixels
0x11C1	Lo					
0x11C2	Hi	max_even_inc	16UI	00.01	RO	Maximum increment for even pixels
0x11C3	Lo					
0x11C4	Hi	min_odd_inc	16UI	00.01	RO	Minimum Increment for odd pixels
0x11C5	Lo					
0x11C6	Hi	max_odd_inc	16UI	00.01	RO	Maximum Increment for odd pixels
0x11C7	Lo					

4.2.13 Binning capability registers [0x1700 to 0x1713]

Table 22. Binning capability registers [0x1700 to 0x1713]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1700	Hi	min_frame_length_lines_bin	16UI	00.D0	RO	Minimum frame length allowed in binning mode. Units: Lines
0x1701	Lo					
0x1702	Hi	max_frame_length_lines_bin	16UI	FF.FF	RO	Maximum possible number of lines per frame allowed in binning mode. Value = 65535 Units: Lines
0x1703	Lo					
0x1704	Hi	min_line_length_pck_bin	16UI	0A.50	RO	Minimum line length allowed in binning mode. Value = 2640 Units: Pixel clocks
0x1705	Lo					
0x1706	Hi	max_line_length_pck_bin	16UI	3F.FF	RO	Maximum possible number of pixel clocks per line allowed in binning mode. Units: Pixel clocks
0x1707	Lo					
0x1708	Hi	min_line_blanking_pck_bin	16UI	05.30	RO	Minimum line blanking time in pixel clocks allowed in binning mode. Value = 1328 Units: Pixel clocks
0x1709	Lo					
0x170A	Hi	fine_integration_time_min_bin	16UI	01.24	RO	Minimum fine integration time. Pixel periods allowed in binning mode.
0x170B	Lo					
0x170c	Hi	fine_integration_time_max_ margin_bin	16UI	07.EA	RO	Current line length – current max fine exposure allowed in binning mode. Pixel periods.
0x170d	Lo					

5 Video data interface

The video stream which is output from the VS6663CD through the compact camera port (CCP) or camera serial interface (CSI) contains both video data and other auxiliary information. This chapter describes the frame formats.

The VS6663CD is MIPI CSI-2 version 1.00 and D-PHY 1.0 compliant.

The selection of the video data format is controlled using the register CSI_SIGNALLING_MODE (0x0111):

0 - CCP2 Data/Clock

1 - CCP2 Data/Strobe

2 - CSI-2 (default)

Changing the video data format must be performed when the sensor is in software standby.

- The CSI-2 link supports the transmission of raw Bayer data at 1.3 Mpixel resolution up to 30 frame/s at 10-bit resolution.
- The CCP link supports the transmission of raw Bayer data at 1.3 Mpixel resolution up to 30 frame/s using10-8bit compressed data or 24 frame/s at 10-bit resolution.
- The VS6663CD has one CSI-2 data lane capable of transmitting at 800 Mbps.
- The VS6663CD CCP lane is capable of transmitting at 640 Mbps.
- The CSI-2 data lane transmitter supports:
  - unidirectional master
  - HS-TX
  - LP-TX (ULPS)
  - CIL-MUYN function
- The CSI-2 clock lane transmitter supports:
  - unidirectional master
  - HS-TX
  - LP-TX (ULPS)
  - CIL-MCNN function

5.1 Frame format

The frame format for the VS6663CD is described by the frame format description registers in *Table 11 on page 24*. For CCP2 this results in a frame as shown in *Figure 11* and for CSI-2 it results in a frame as shown in *Figure 12*.

Figure 11. VS6663CD CCP2 frame format

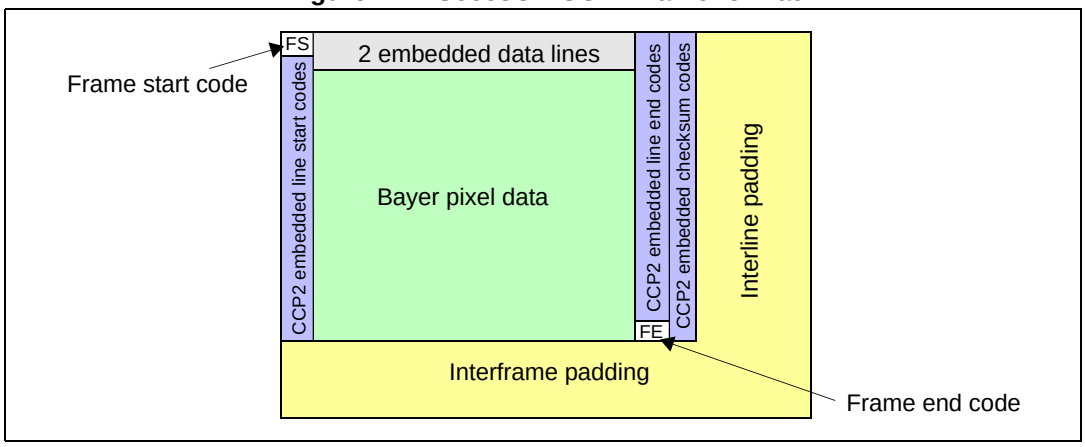
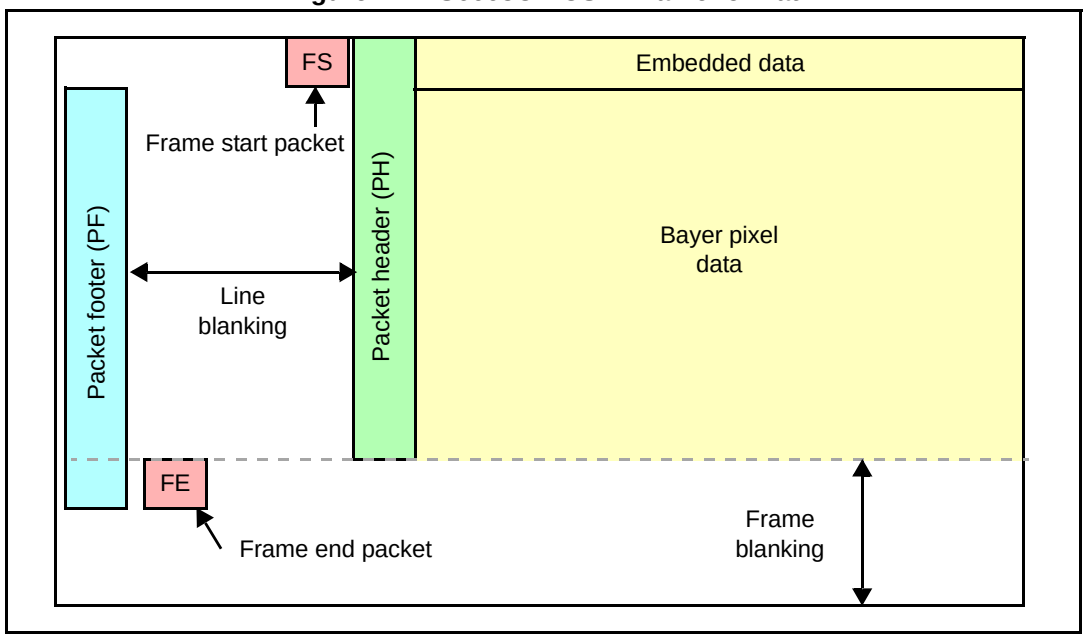


Figure 12. VS6663CD CSI-2 frame format



Embedded data lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details within the output data stream. The number of embedded data lines at the start and end of the frame is specified as part of the frame format description. VS6663CD has two embedded data lines.

Dummy pixel data

This is invalid pixel data. The receiver should always ignore dummy pixel data. The VS6663CD has 0 dummy columns.

Visible pixel data

The visible pixels contain valid image data.The correct integration time and analog gain for the visible pixels is specified in the blank lines at the start of the frame.The number of visible pixels can be varied with the requested frame size.

Dark pixel data (light shielded pixels)

The VS6663CD has 0 dark pixels.

Black pixel data (zero integration time)

The VS6663CD has 0 black pixels.

Manufacturer specific pixel data

The VS6663CD has 0 manufacturer specific pixels.

Interline padding/line blanking

During interline padding all bits in the data stream in a CCP2 frame are set to 1.

In a CSI-2 frame there is no concept of line blanking being transmitted, the sensor will simply spend a longer time in the LP state between active line data.

Interframe padding / frame blanking

During interframe padding all bits in the data stream in a CCP2 frame are set to 1.

In a CSI-2 frame there is no concept of frame blanking being transmitted, the sensor will simply spend a longer time in the LP state at the end of the active data for a frame.

6 Video timing

6.1 Output size

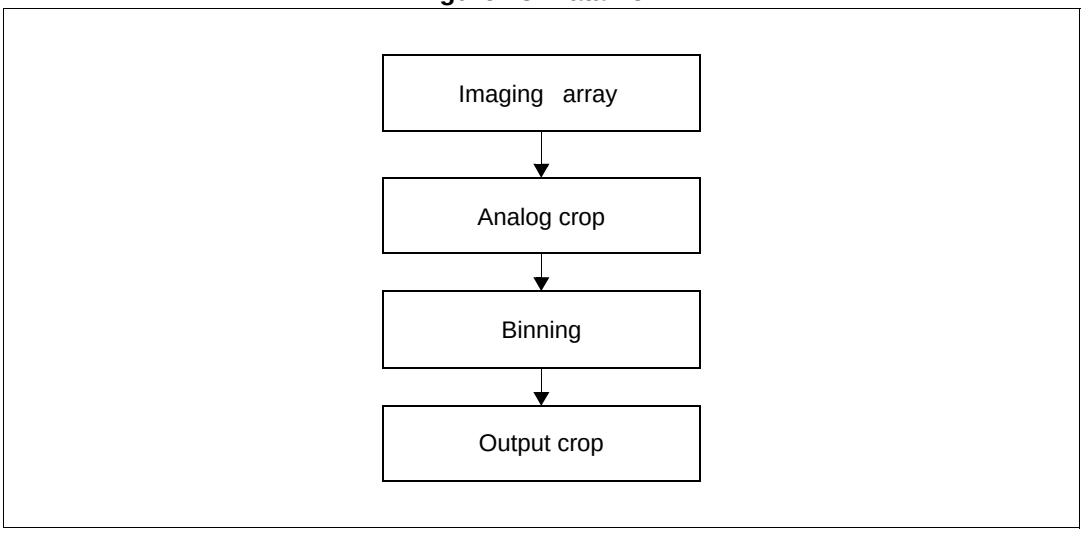
The VS6663CD has the following methods available to achieve the required output size, these can be used independently or in conjunction with any other:

- analog crop, see *Section 6.1.1*
- binning, see *Section 6.1.2*
- output crop, see *Section 6.1.3*

Note: The VS6663CD does not support subsampling.

The programmable image size and output size are independent functions. It is the responsibility of the host to ensure that these functions are programmed correctly for the intended application.

Figure 13. Data flow

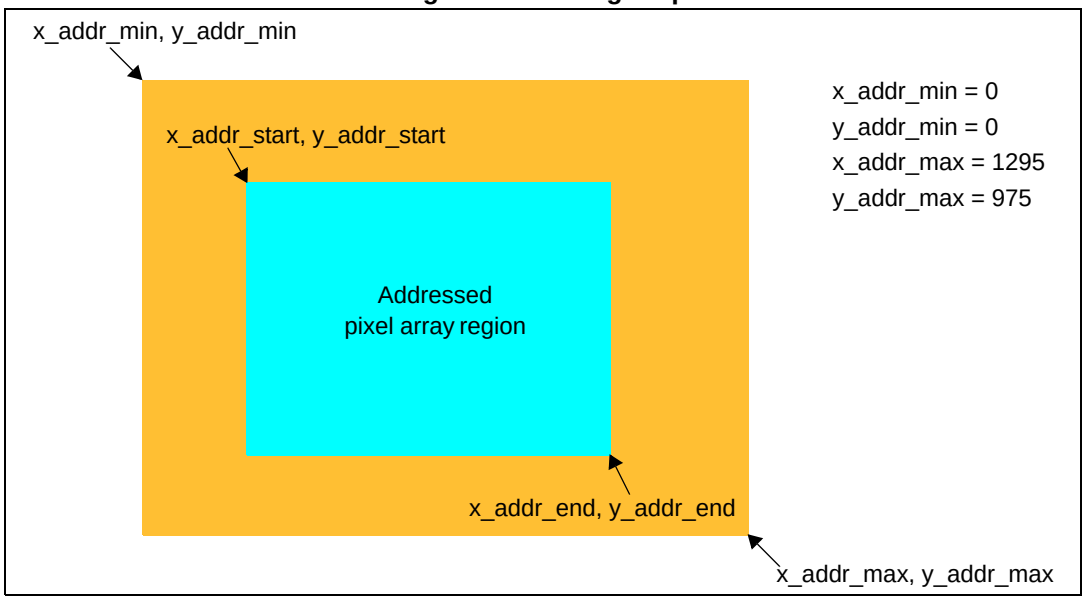


6.1.1 Analog crop

The native size for the VS6663CD is 1280x 960, the maximum addressable array is 1296 x 976 which gives eight border pixels for the color reconstruction algorithms to use at the edges of the array.

By programming the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers it is possible to use the full size of the array as you would do for a native size output or you can select a “window of interest”. The addressed region of the array is used in any subsequent binning operation.

Figure 14. Analog crop



The host must ensure the following rules are kept:

- the end address must be greater than the start address
- the x and y start addresses are restricted to even numbers only, and the x and y end addresses are restricted to odd numbers only, to ensure that there is always a even number of pixels read-out

6.1.2 Binning

The VS6663CD also has a binning mode that offers a reduced size full field of view image. The binning mode averages row and column pixel data.

The binning mode results in a reduced number of lines and so can be used to give a higher image frame rate. Compared to subsampling, binning makes use of the light gathered from the whole pixel array and it results in higher image quality.

The binning mode will scale by 2x2 in the X and Y direction. Entering and exiting binning mode may or may not be performed when the sensor is in software standby.

Table 23 summarizes the register setting for enabling binning mode. (The x/y_odd_inc registers are automatically set and do not require to be set by the user.)

Table 23. Binning register settings

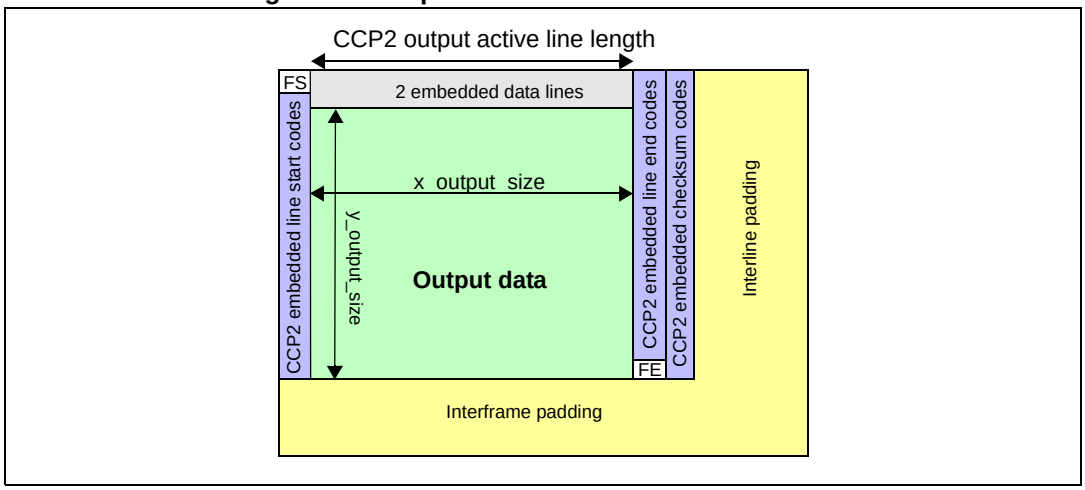
Register	Address	Normal	Binning 2x2
binning_mode	0x0900	0	1

6.1.3 Output crop

The x_output_size and y_output_size registers are not intended as the primary cropping controls.

They are intended to define the position of the LE/FE codes in the CCP2 data frame so that the sensor does not need to calculate this based on analog crop or binning settings. It should be expected that the host will set the output sizes to exactly enclose the output image data. If the host should not do this, the VS6663CD treats the output size as being calculated from the top left hand corner of the output array. So in the case where output sizes are smaller than the output data, the data shall be cropped from its right-hand and lower limits. In the case where larger than the output data, the lines shall be padded out to the defined output size with undefined data.

Figure 15. Output size within a CCP2 data frame



The number of pixels between the line start and the line end sync codes for:

- RAW8 is a multiple of 4 pixels
- RAW10 is a multiple of 4 pixels for CSI-2 and a multiple of 16 pixels for CCP2

The host must control the x_output_size to ensure that the above criteria is met.

6.2 Video timing

This section specifies the timing for the image data that is readout from the pixel array and the output image data. These are not necessarily the same size.

The application of all of the video timing read/write parameters must be re-timed to the start of frame boundary to ensure that the parameters are consistent within a frame. The video stream which is output from the VS6663CD contains both video data and other auxiliary information.

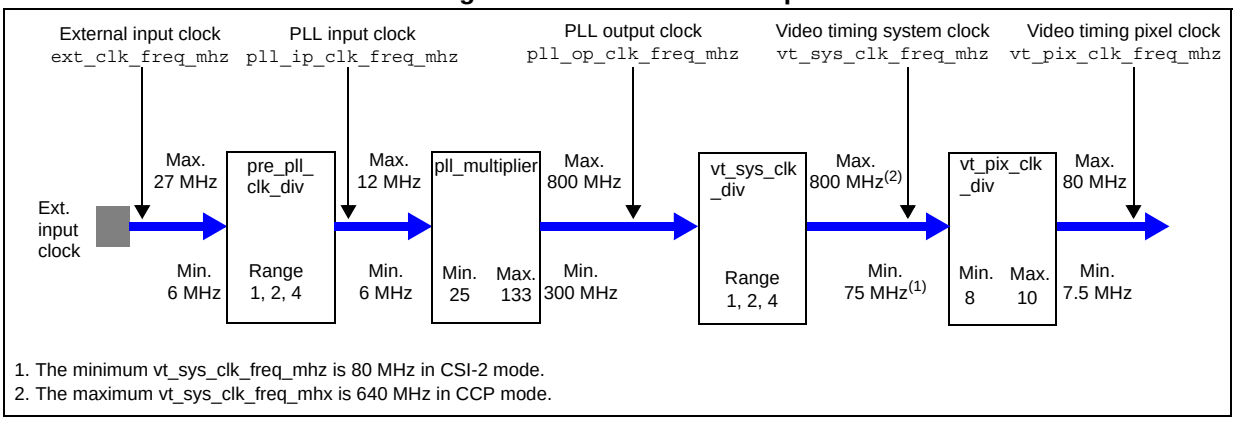
6.2.1 PLL block

The VS6663CD contains a phase locked loop (PLL) block, which generates all the necessary internal clocks from the external clock input. Changes to the PLL settings on the VS6663CD will only be consumed on the software standby to streaming mode transition.

Figure 16 shows the internal functional blocks, which define the relationship between the external input clock frequency and the pixel clock frequency.

The majority of the logic within the device is clocked by vt_sys_clk however the CCI block is clocked by the external input clock.

Figure 16. Clock relationship



1. The minimum vt_sys_clk_freq_mhz is 80 MHz in CSI-2 mode.
2. The maximum vt_sys_clk_freq_mhx is 640 MHz in CCP mode.

The equation relating the input clock frequency to pixel clock frequencies is:

$$vt_pix_clk_freq_mhz = \frac{ext_clk_freq_mhz \times pll_multiplier}{pre_pll_clk_div \times vt_sys_clk_div \times vt_pix_clk_div}$$

6.2.2 Framerate

The framerate of the array readout and therefore the output framerate is governed by the line length, frame length and the video timing pixel clock frequency.

- line length is specified as a number of pixel clocks, `line_length_pck`
- frame length is specified as a number of lines, `frame_length_lines`
- video timing pixel clock is specified in MHz, `vt_pix_clk_freq_mhz`

The equation relating the framerate to the line length, frame length and the video timing pixel clock frequency is:

$$\text{Framerate} = \frac{\text{vt_pix_clk_freq_mhz}}{\text{line_length_pck} \times \text{frame_length_line}}$$

Table 24 provides examples of frame timing for Raw10 CSI-2 mode for 30 fps at a variety of external clock frequencies.

Table 24. External clock frequency examples - 1.3 Mpixel resolution Raw10 30 fps

Ext clk freq	Pre-PLL clk div	PLL multiplier	VT sys clk div	VT pixel clk div	VT pixel clk freq	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Pixel clks	Lines (Dec)
9.60	1	83	1	10	79.68	2640	1006
12.00	2	133	1	10	79.80	2640	1007
13.00	2	123	1	10	79.95	2640	1009

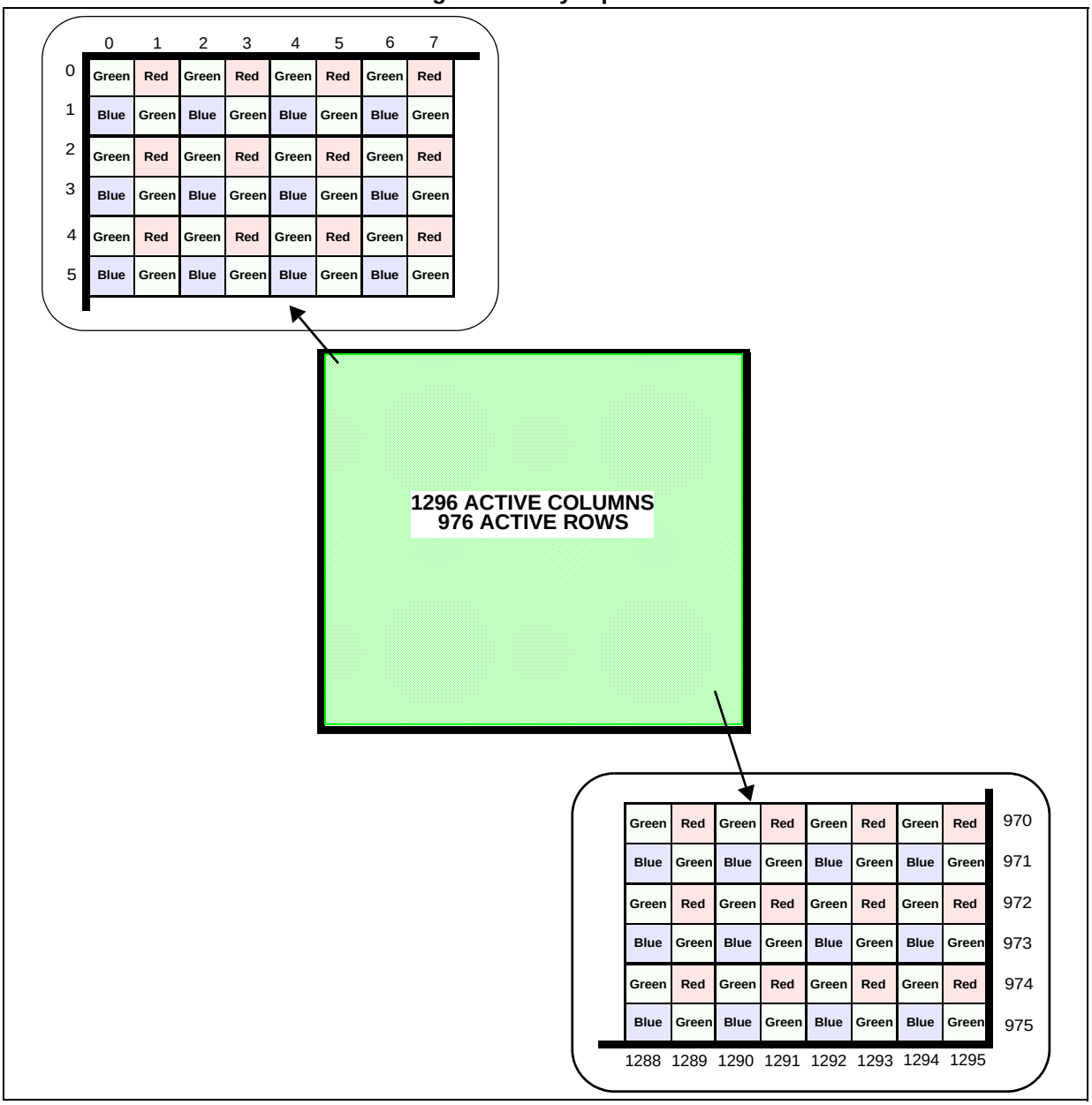
6.2.3 Bayer pattern

The three color (Red, Green, Blue) filters are arranged over the pixel array in a repeated 2x2 arrangement known as the Bayer Pattern. When the sensor array is read, the output order of red, green, blue depends on the settings of vertical flip and horizontal mirror.

Figure 17 shows the read-out order for the default settings of vertical flip and horizontal mirror turned off. Vertical flip changes the first line to be output from a green/red line to a blue/green line and horizontal mirror changes the sequence within a line, for example, green/red to red/green.

As shown in *Figure 17*, the first pixel to be readout from the imaging array will be green followed by red.

Figure 17. Bayer pattern



6.3 Exposure and gain control

VS6663CD does not contain any form of automatic exposure control. To produce a correctly exposed image the integration period and analog gain for the pixels must be calculated by an exposure control algorithm implemented externally. The parameters are then written to the VS6663CD through the CCI interface.

The exposure control parameters available on VS6663CD are:

- fine integration time
- coarse integration time
- analog gain
- digital gain

The exposure control parameter registers are defined in *Section 4.2.6: Integration time and gain registers [0x0200 to 0x02FF] on page 27*.

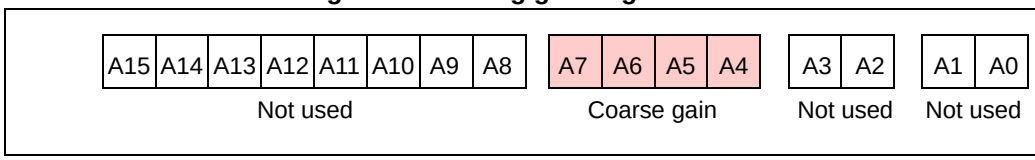
Integration time and analog gain capability registers should be used to determine the exposure control parameter limits for a given video timing configuration.

6.3.1 Gain model

VS6663CD only supports the single global analog gain mode.The gain is monotonic to avoid instabilities in the exposure loop VS6663CD has a 16-bit register (0x0204 and 0x0205) to control analog gain.

Figure 18 shows how the analog gain bits are used for VS6663CD.

Figure 18. Analog gain register format



The following generic equation describes VS6663CD gain behavior specified by the analog gain description registers 0x008A to 0x0093:

$$gain = c0/(m1 \cdot x + c1)$$

where:

$m_1 = -1$

$c_0 = 256$

$c_1 = 256$

Table 25 specifies the valid analog gain values for VS6663CD.

Table 25. Analog gain control

Gain value (0x0204/0x0205)	Coarse gain code [A7:A4]	Coarse analog gain
0x0000	0000	0.00 dB (x1.00)
0x0010	0001	0.6 dB (x 1.07)
0x0020	0010	1.1 dB (x1.14)
0x0030	0011	1.8 dB (x1.23)

Table 25. Analog gain control (continued)

Gain value (0x0204/0x0205)	Coarse gain code [A7:A4]	Coarse analog gain
0x0040	0100	2.5 dB (x1.33)
0x0050	0101	3.2 dB (x1.45)
0x0060	0110	4.1 dB (x1.60)
0x0070	0111	5.0 dB (x1.78)
0x0080	1000	6.0 dB(x2.00)
0x0090	1001	7.2 dB (x2.29)
0x00A0	1010	8.5 dB (x2.66)
0x00B0	1011	10.1 dB (x3.20)
0x00C0	1100	12.0 dB (x4.00)
0x00D0	1101	14.5 dB (x5.33)
0x00E0	1110	18.1 dB (x8.00)
0x00F0	1111	24.1 dB (x16.00)

6.3.2 Digital gain

To help compensate for the relatively coarse analogue gain steps, VS6663CD contains a digital multiplier to “fill” in the missing steps. By mixing analogue and digital gain it is possible to implement 3% gain steps across the full 1x to 16x gain range

The details of the digital gain implementation are listed below:

- four individual 16-bit digital channel gains - one per Bayer channel
  - digital_gain_greenR (0x020E and 0x020F)
  - digital_gain_red (0x0210 and 0x0211)
  - digital_gain_blue (0x0212 and 0x0213)
  - digital_gain_greenB (0x0214 and 0x0215)
- The digital gain range for each channel is 0.0039 to 1.996 in steps of 0.0039 (1/256)
  - digital_gain_min {0x1084:0x1085} = 0x0001 (0.0039)
  - digital_gain_max {0x1086:0x1087} = 0x01FF (1.996)
  - digital_gain_step {0x1088:0x1089} = 0x0001 (0.0039)

6.3.3 Integration and gain parameter retiming

The modification of exposure parameter (coarse integration time or gain) register values does not take effect immediately.

The exact time at which changes to certain parameters take effect is controlled both to ensure that each frame of image data produced has consistent settings and that changes in groups of related parameters can be synchronized.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain setting, if the serial interface communications extends over a frame boundary, the internal retiming of exposure and gain data is disabled while writing data to the serial interface register map. Therefore if the 4 bytes of exposure and gain data is sent as an auto-

increment CCI sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

However if it is not possible for the host to use auto-increment CCI register accesses and only discrete register accesses are possible then the VS6663CD has a mechanism to temporarily suspend the automatic application of updated exposure register values.

A group of parameter changes is marked by the host using a dedicated Boolean control parameter, grouped_parameter_hold (register 0x0104). Any changes made to ‘retimed’ parameters while the grouped_parameter_hold signal is in the ‘hold’ state will be considered part of the same group. Only when the grouped_parameter_hold control signal is moved back to the default ‘no-hold’ state will the group of changes be executed by VS6663CD.

7 Electrical characteristics

All parameter values quoted in this outline product specification are design targets and will be confirmed by evaluation of initial samples and device characterization.

Typical values quoted for nominal voltage, process and temperature. Maximum values are quoted for worst case conditions (process, voltage and functional temperature) unless otherwise specified.

7.1 Absolute maximum ratings

Table 26. Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DIGMAX}	Digital power supply	-0.3	2.2	V
V_{ANAMAX}	Analog power supply	-0.3	3.2	V
$V_{IP(DIG)}$	Digital input voltage(1)	-0.3	V_{ANA} + 0.3	V
T_{STO}	Storage temperature	-40	+ 85(2)	^{o}C
V_{ESD}	Electrostatic discharge model Human body model(3) Charge device model(4)	 -2 -500	 2 500	 KV V

1. Digital input: EXTCLK, XSHUTDOWN, SCL, SDA
2. This is a maximum long term standard storage temperature, see soldering profile for short term high temperature tolerance
3. HBM tests are performed in compliance with JESD22-A114F
   MM test is performed in compliance with JESD22-A115A Class B if HBM pass level is less than 1000V.
4. CDM ESD tests are performed in compliance with JESD22-C101D

Caution: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating conditions

Table 27. Operating conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Voltage					
VDIG	Digital power supply	1.68	1.8	1.92	V
VANA	Analog power supply	2.6	2.8	2.9	V
Temperature					
T_{AS}	Temperature (storage[1])	-40	-	+85	°C
T_{AF}	Temperature (functional operating[2])	-30	-	+70	°C
T_{AN}	Temperature (normal operating[3])	-25	-	+55	°C
T_{AO}	Temperature (optimal operating[4])[5]	+5	-	+40	°C
T_{AT}	Temperature (test[6])	+21	-	+25	°C

1. Camera has no permanent degradation.
2. Camera is electrically functional.
3. Camera produces “acceptable” images.
4. Camera produces optimal optical performance.
5. Camera surface temperature.
6. 100% tested parameters are measured at this temperature.

7.3 Power supply - VDIG, VANA

Table 28. Power supplies VDIG, VANA

Parameter	Digital		Analogue		Unit
	Typical	Maximum	Typical	Maximum	
Hardware standby	2	20	2	10	µA
Streaming[1]	18	50	40	55	mA

1. Full resolution, 10-10data, 30 fps, CSI-2

7.3.1 Peak current

The peak current consumption of the sensor module is defined as any current pulse >=10 µs. Peak current is assumed to be <1.33 x maximum average current for the stated operating mode and worst case conditions. The duty cycle of the peak to the low part of the current profile is 33% with a worst-case period of 500 µs.

7.4 System clock - EXTCLK

Table 29. System clock - EXTCK

Symbol	Parameter	Minimum	Maximum	Unit
f_{EXTCLK}	Clock frequency input	6.0 - 1%(1)	27 + 1%(1)	MHz
	Leakage current	4(2)	30(3)	µA

1. Nominal frequencies are 6.0 to 27 MHz with a 1% centre frequency tolerance.
2. With DC coupled square wave clock.
3. With DC VDIG applied.

7.5 Power down control - XSHUTDOWN

Table 30. Power down control - XSHUTDOWN

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	0	-	0.3 VDIG	V
V_{IH}	High level input voltage	0.7 VDIG	-	VANA	V

7.6 CCI interface - SDA, SCL

7.6.1 CCI interface - DC specification

Table 31. CCI interface - DC specification

Symbol	Parameter	Minimum	Maximum	Unit
V_{IL}	Low level input voltage	0	0.3 * VDIG	V
V_{IH}	High level input voltage	0.7 * VDIG	VDIG	V
V_{OL}	Low level output voltage(1)	0	0.2 * VDIG	V
I_{IL}	Low level input current	-	-10	µA
I_{IH}	High level input current	-	10	µA

1. V_{OH} not valid for CCI. 3mA drive strength

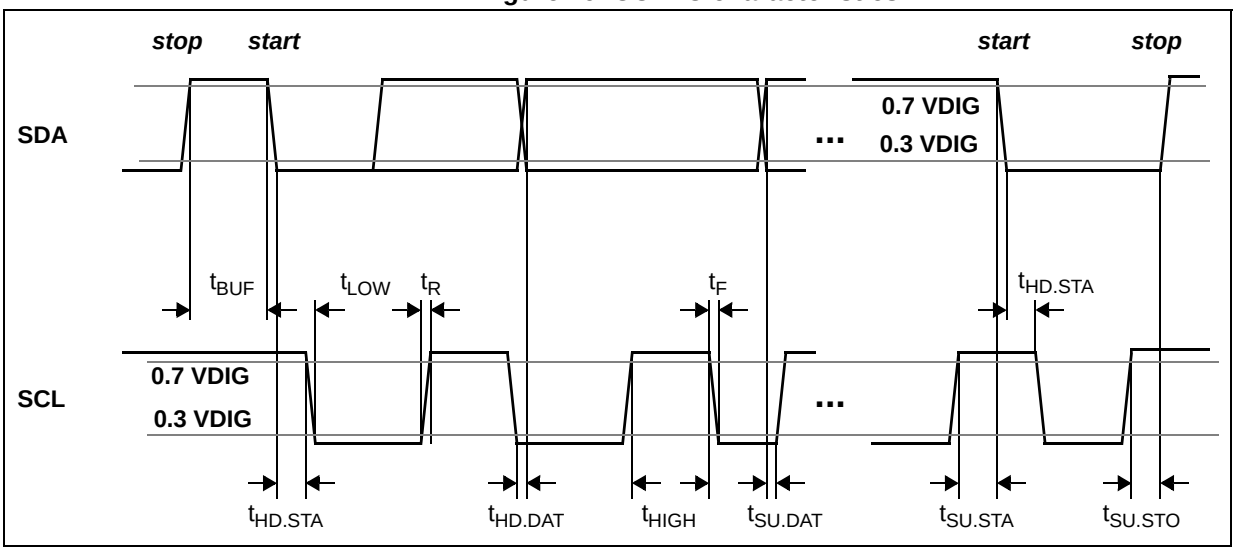
7.6.2 CCI interface - timing characteristics

Table 32. CCI interface - timing characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	Clock pulse width low	1.3	-	-	µs
t_{HIGH}	Clock pulse width high	0.6	-	-	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	0	-	50	ns
t_{BUF}	Bus free time between transmissions	1.3	-	-	µs
$t_{HD.STA}$	Start hold time	0.6	-	-	µs
$t_{SU.STA}$	Start set-up time	0.6	-	-	µs
$t_{HD.DAT}$	Data in hold time	0	-	0.9	µs
$t_{SU.DAT}$	Data in set-up time	100	-	-	ns
t_R	SCL/SDA rise time	20+0.1 Cb(1)	-	300	ns
t_F	SCL/SDA fall time	20+0.1 Cb(1)	-	300	ns
$t_{SU.STO}$	Stop set-up time	0.6	-	-	µs
Ci/o	Input/output capacitance (SDA)	-	-	8	pF
Cin	Input capacitance (SCL)	-	-	6	pF

1. Cb = total capacitance of one bus line in pF

Figure 19. CCI AC characteristics



All timings are measured from either 0.3 VDIG or 0.7 VDIG.

7.7 CCP2 interface

7.7.1 CCP2 interface - DC specification

Table 33. CCP2 interface - DC specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{OD}	Differential voltage swing(1)	100	150	200	mV
V_{CM}	Common mode voltage (self biasing)	0.8	0.9	1.0	V
R_O	Output Impedance	40		140	Ω
I_{DR}	Drive current range (internally set by bias circuit)	0.5	1.5	2	mA
PSRR(2)	0 - 100MHz	-	-	30	dB
	100 - 1000MHz	-	-	10	dB

1. Measured over a 100 Ω load
2. Nominal value for the interference at V_{CM} voltage through digital supply relative to the interference at digital supply over the 0-1 GHz operating range. PSRR = 20*log10 (V_{DIG} interference (peak-to-peak) / V_{CM} interference (peak-to-peak))

7.7.2 CCP2 interface - timing characteristics

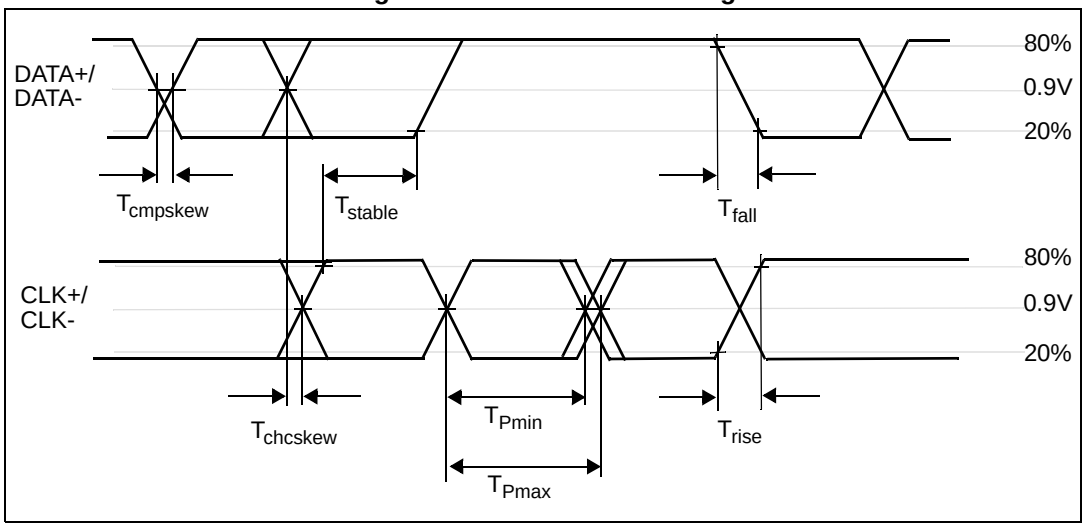
The parameters in *Table 34* are measured across a terminated 100 Ω transmission line, in data/strobe mode.

Table 34. CCP2 interface - timing characteristics

Symbol	Parameter	Min.	Max.	Unit
F_p	Average data frequency	-	640	Mbits/s
T_p	Average data period	1.56	-	ns
T_{jitter}(1)	Data period Jitter	-	200	ps
t_{stable}	Both data and clock at the stable level	780	-	ps
T_{rise}	Rise time of DATA+/DATA- ,CLK+/CLK-	300	400	ps
T_{fall}	Fall time of DATA+/DATA-, CLK+/CLK-	300	400	ps
T_{skew}(2)	Total skew between signals	-	225	ps
t_{PWR}	Power up/down time	-	20	µs

1. T_{Pmax}-T_{Pmin}
2. T_{skew} =$T_{cmpskew}$ + $T_{chcskew}$

Figure 20. SubLVDS AC timing



7.8 CSI-2 interface

7.8.1 CSI-2 interface - DC specification

Table 35. CSI-2 interface - high speed mode - DC specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage(1)	140	200	270	mV
V_{OHHS}	HS output high voltage(1)			360	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω

1. Value when driving into load impedance anywhere in the Z_{ID} range (80-125Ω).

Table 36. CSI-2 interface - low power mode - DC specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{OH}	Output high level	1.1	1.2	1.3	V
V_{OL}	Output low level	-50		50	mV
Z_{OLP}	Output impedance of LP transmitter	110			Ω

7.8.2 CSI-2 interface - AC specification

Table 37. CSI-2 interface - high speed mode - AC specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit
	Data rate	80	-	800	Mbits/s
t_r and t_f	20% - 80% rise time and fall time	150		0.3UI(1)	ps
t_{skew}	Data to clock skew	-0.15UI	-	0.15UI	ps

1. UI is equal to 1/(2*fh) where fh is the fundamental frequency of the transmission for a certain bit rate. For example, for 800 Mbps, fh is 400 MHz.

Table 38. CSI-2 interface - low power mode - AC specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_r and t_f	15% - 85% rise time and fall time			25	ns

Note: For further information on the D-PHY please refer to the following specification document: MIPI Alliance Standard for D_PHY version 1.00.

8 Optical specification

8.1 Lens characteristics

Table 39. Lens design characteristics for first source lens supplier

Parameter	Value					
2-element plastic lens	-					
F/number	2.8					
Effective focal length	2.31mm (paraxial)					
Horizontal FOV	50.7°					
Nominal focusing distance	15 cm					
Stray-light	No undesirable stray-light artefact's to be present in image at contrast of: 1:10^5 out of scene 1:10^4 in scene					
Spectral weighting: Wavelength (nm) Weight	656.28 151	587.56 318	546.07 312	486.13 157	435.84 49	404.66 13
Lateral chromatic aberration from blue (λ=435nm) to red (λ=640nm)	< |3.8 um|					
Coating reflectance - All surfaces are coated. At least 50% of all surfaces must fulfil this specification.	< 400 nm 400 - 670 nm >670 nm		No limitation ≤ 1.0% absolute, 0.35% avg Straight line with a slope of < 3% / 100nm			
Maximum chief ray angle	29°					

8.2 User precaution

As is common with many CMOS image modules the camera should not be pointed at bright static objects for long periods of time as permanent damage to the sensor may occur.

9 On-chip image optimization

9.1 Mapped couplet correction (Bruce filter)

The mapped couplet defect correction filter is designed to intelligently correct the first defect in a couplet thereby changing a couplet into a single pixel defect. Single pixel correction is achieved either by the median filter or by the host (coprocessor, MMP or baseband). The mapped couplet correction filter operates in both full resolution, and in binned mode.

The mapped couplet correction filter requires exact coordinate information for each of the couplets to be repaired. The couplet coordinates are stored in non-volatile-memory (NVM) during production test.

The mapped couplet correction is controlled by register 0x0B05:

0 - Disable

1 - Enable

9.2 Median filter

This is a simple 1-D median filter defect correction which replaces every pixel value by the median of itself, its predecessor and its successor (respecting the color pattern). The median filter operates in both full resolution, and in binned mode. It is suggested that this filter is only used for viewfinder images or other non stored images. (Note that the median filter will not correct any defective pixels which occur in either the first two or the last two columns).

The selection of the median filter is controlled using register (0x0B06)

0 - Disable

1 - Enable

9.3 Lens shading correction

The VS6663CD has an adaptive (four color temperature) lens shading correction function which can be used to reduce the effect of roll off in the optical system. Correction is carried out individually for all four color planes, each gain is calculated based on the distance from the image centre to the pixel in question using a two factor polynomial (R^2 and R^4). The lens shading filter operates in both full resolution, and in binned mode. The correction applied is 75%.

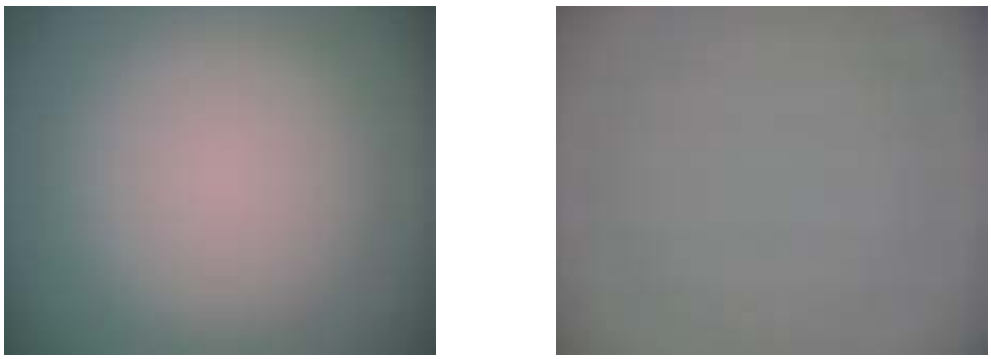
In order to optimize the AV algorithm, the coefficients for each device are calculated under D65 (Fluorescent Philips Graphica Pro 965) lighting conditions and programmed in the NVM memory at production test. (The coefficients from the NVM can be overwritten).

Settings for three other color temperatures (Cool White, U30, and Horizon) are calculated from characterization data and these are stored in the NVM memory.

The calculation of the color temperature is performed by the sensor using the white balance gains. The white balance gains can either be calculated internally by the sensor or they can be calculated by the host and written back to the sensor.

Figure 21 provides an example of lens shading correction.

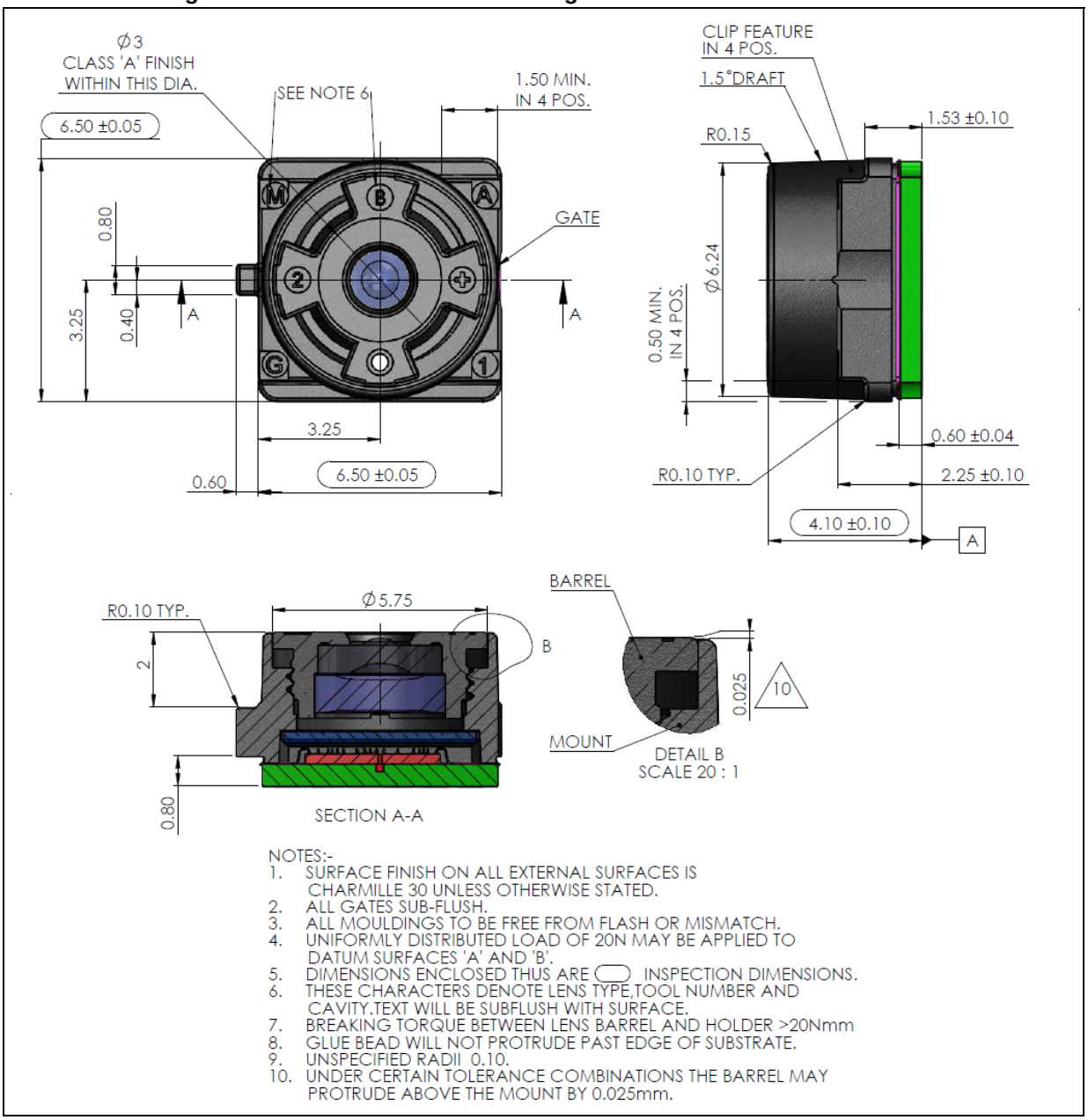
Figure 21. Lens shading images



Original image Corrected image

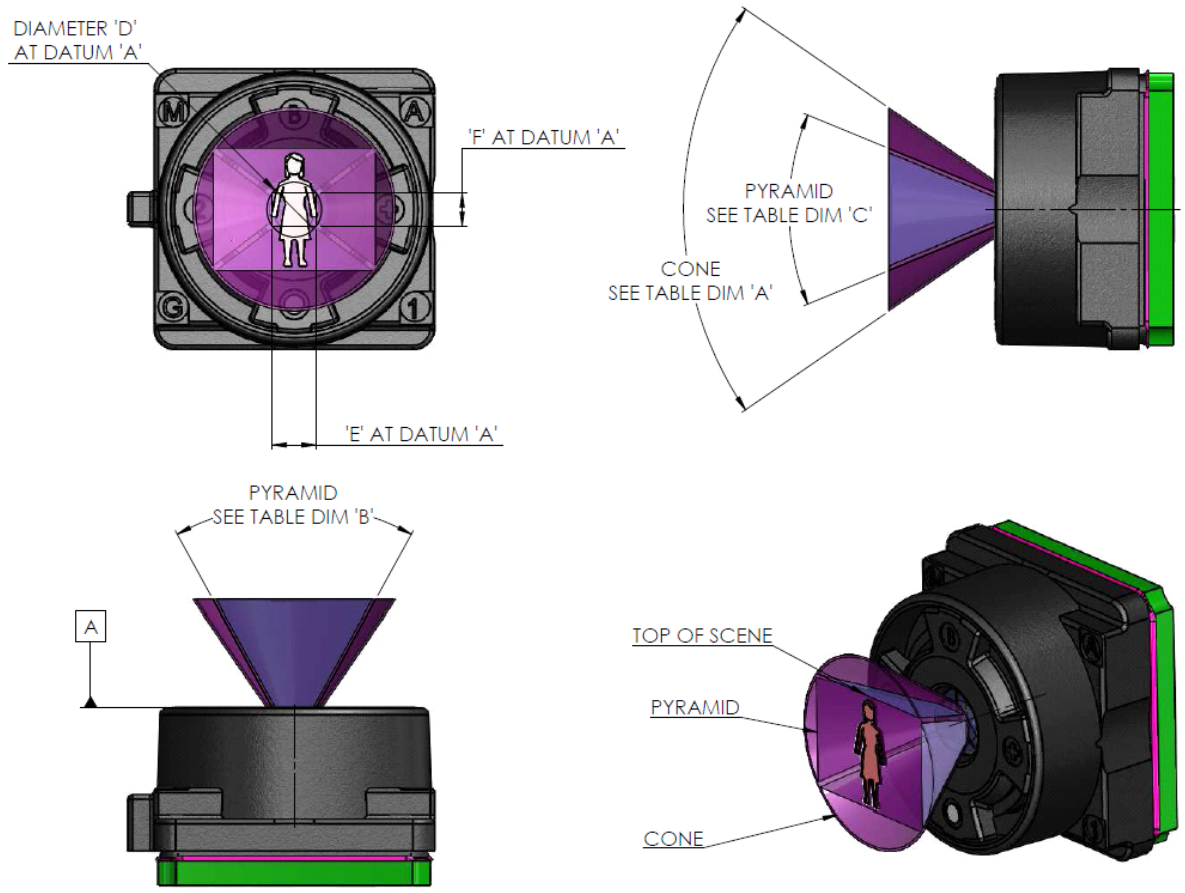
10 Mechanical

Figure 22. VS6663CD outline drawing - 1 of 3 - All dimensions in mm



NOTES:-
1. SURFACE FINISH ON ALL EXTERNAL SURFACES IS CHARMILLE 30 UNLESS OTHERWISE STATED.
2. ALL GATES SUB-FLUSH.
3. ALL MOULDINGS TO BE FREE FROM FLASH OR MISMATCH.
4. UNIFORMLY DISTRIBUTED LOAD OF 20N MAY BE APPLIED TO DATUM SURFACES 'A' AND 'B'.
5. DIMENSIONS ENCLOSED THUS ARE ( ) INSPECTION DIMENSIONS.
6. THESE CHARACTERS DENOTE LENS TYPE,TOOL NUMBER AND CAVITY.TEXT WILL BE SUBFLUSH WITH SURFACE.
7. BREAKING TORQUE BETWEEN LENS BARREL AND HOLDER >20Nmm
8. GLUE BEAD WILL NOT PROTRUDE PAST EDGE OF SUBSTRATE.
9. UNSPECIFIED RADII 0.10.
10. UNDER CERTAIN TOLERANCE COMBINATIONS THE BARREL MAY PROTRUDE ABOVE THE MOUNT BY 0.025mm.

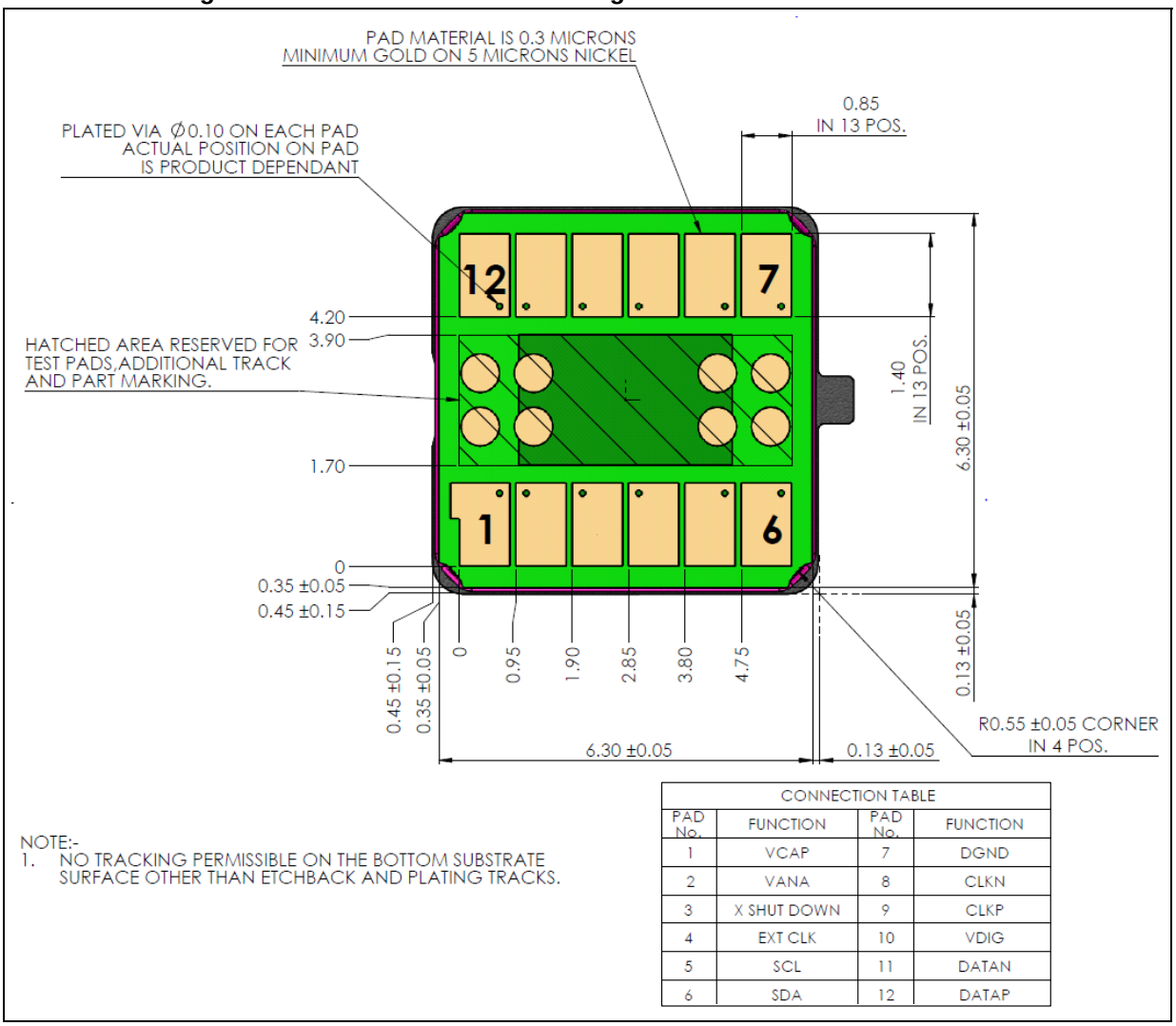
Figure 23. VS6663CD outline drawing - 2of 3 - All dimensions in mm



EXCLUSION ZONE NOTES:-
1. EDGES OF CIRCULAR HOLES IN CUSTOMER'S EQUIPMENT MUST NOT INTRUDE INTO THE CONE.
2. EDGES OF RECTANGULAR HOLES MUST NOT PROTRUDE INTO THE PYRAMID.
3. DIMENSIONS SHOWN ARE MAXIMUM.

EXCLUSION ZONE DIMENSIONS						
MODULE/ SILICON	A	B	C	D	E	F
1.3mPixel	69°	57.6°	44.8°	1.27	1.02	0.76

Figure 24. VS6663CD outline drawing - 3 of 3 - All dimensions in mm



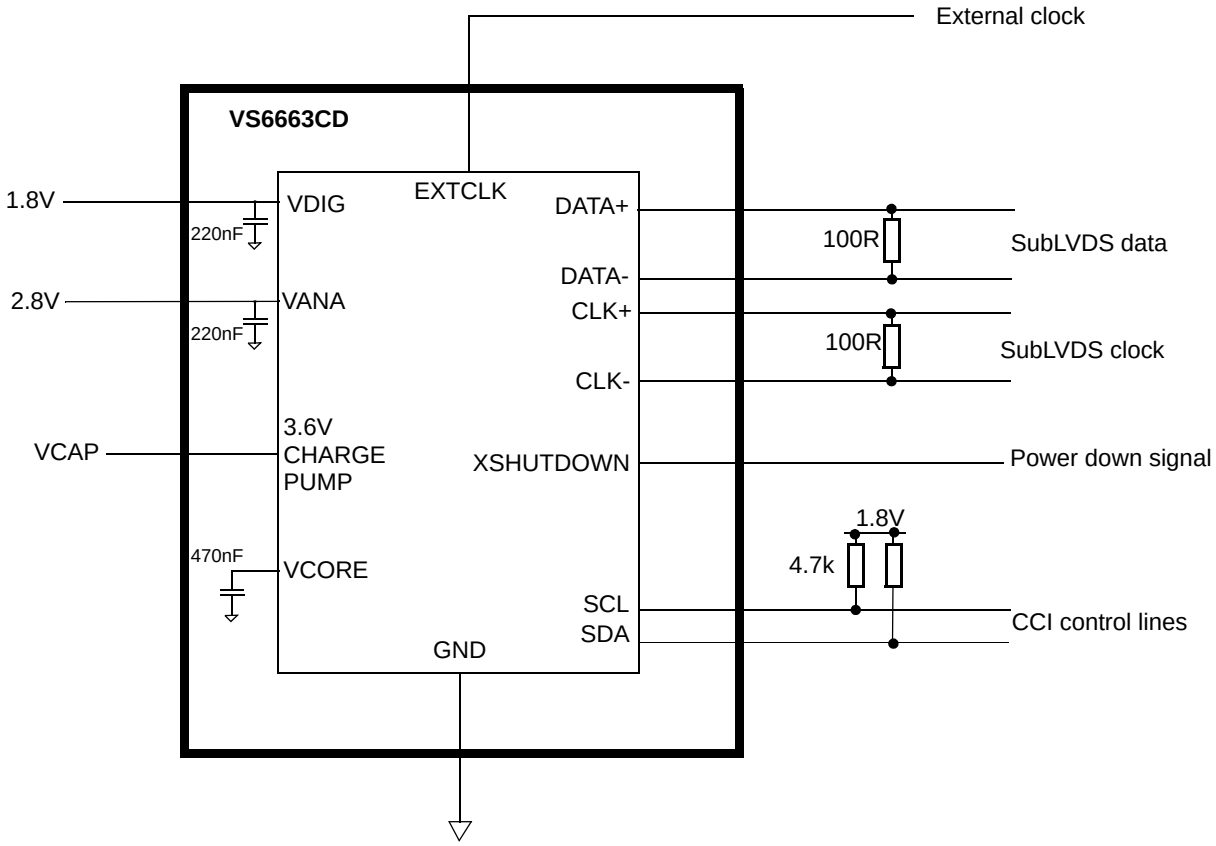
NOTE:-
1. NO TRACKING PERMISSIBLE ON THE BOTTOM SUBSTRATE SURFACE OTHER THAN ETCHBACK AND PLATING TRACKS.

CONNECTION TABLE			
PAD No.	FUNCTION	PAD No.	FUNCTION
1	VCAP	7	DGND
2	VANA	8	CLKN
3	X SHUT DOWN	9	CLKP
4	EXT CLK	10	VDIG
5	SCL	11	DATAN
6	SDA	12	DATAP

11 Application

11.1 Schematic

Figure 25. Mobile camera application



Notes:

No connection should be made to VCAP.

CCCP2 100R termination may be internal to subLVDS receiver. For CSI-2, the receiver is mandated to have an internal termination which is dynamically switched in and out depending on whether the link is in HIGH SPEED or LOW POWER mode. This transition occurs every line.

12 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

13 Revision history

Table 40. Document revision history

Date	Revision	Changes
19-Jan-2015	1	Initial release.
09-Sep-2015	2	Updated disclaimer

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