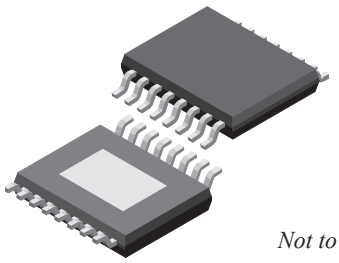
Automotive, High-Current LED Controller

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Constant-current LED drive
- 4.2 to 50 V supply
- 53.3 V maximum LED string voltage
- Boost, buck-boost, buck, and SEPIC switching converters
- Programmable switching frequency 70 to 700 kHz
- PWM-controlled PMOS driver allows accurate LED current control at low duty cycles
- Dimming via external PWM, internal PWM and/or analog dimming
- Frequency dither scheme for effective spread spectrum to reduce EMI
- Comprehensive fault protection and fault flag

PACKAGE:

16-Pin eTSSOP (LP)
with Exposed Thermal Pad



Not to scale

DESCRIPTION

The A6271-1 is a DC-DC converter controller, providing a programmable constant-current output for driving high-power LEDs in series. The controller is based on a programmable fixed-frequency, peak current-mode control architecture. The DC-DC converter can be configured in a myriad of different switching configurations including boost, buck-boost, buck (ground-referenced switch), and SEPIC.

The A6271-1 provides a cost-effective solution using an external logic-level MOSFET and minimum additional external components. The maximum LED current is set with a single external sense resistor and can be accurately modulated using a current reference input (analog control). External PWM dimming is possible via the PWMIN input, which also provides a shutdown mode. As an alternative, an internal PWM dimming circuit can be used by programming the PWMIN and DR pins. Either PWM scheme controls the PWMOUT output which drives an external p-channel MOSFET connected in series with the LED string. This MOSFET is also used to isolate the load during certain fault conditions, including output shorts to ground.

Continued on next page...

APPLICATIONS

- Automotive high-power LED lighting systems
- Fog lights, reversing lights, daytime running lights, position lights, headlights

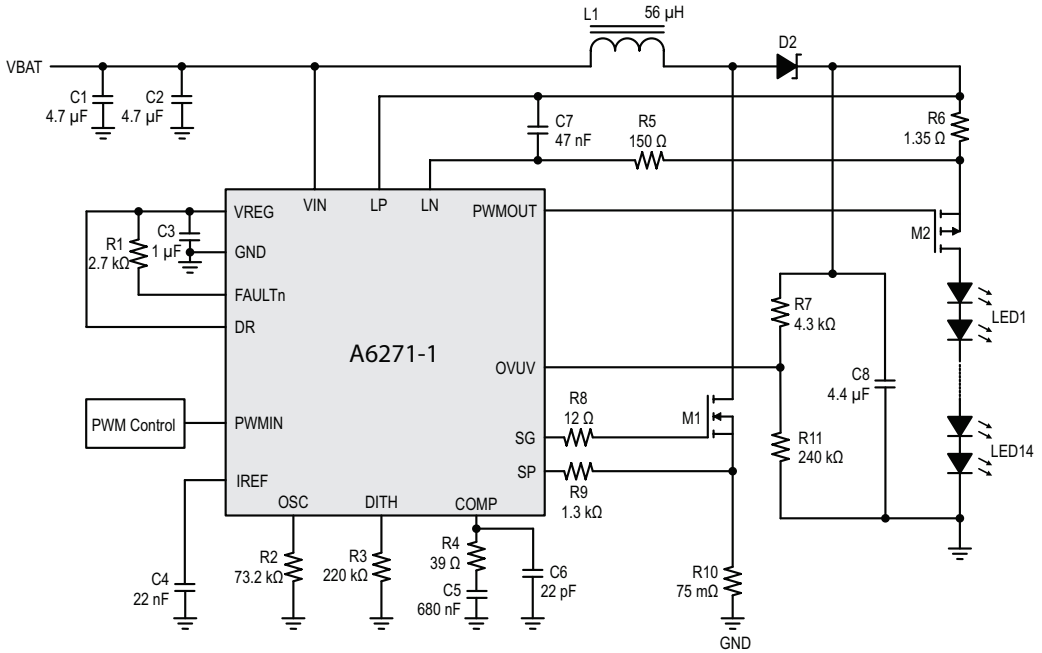


Figure 1: Boost Switcher Driving 14 LEDs at 150 mA

DESCRIPTION (continued)

The A6271-1 has been carefully designed to minimize electromagnetic emissions through distributed decoupling and an externally programmable frequency dither circuit configured for the EMI specification CISPR 25. It is also possible to program the fundamental switching frequency below 150 kHz where most EMI standards begin.

The A6271-1 has a comprehensive set of integrated protection features to protect the IC, the LED driver system, and the LED string against faults. Fixed-output overvoltage protection ensures no maximum voltage rating violations, even under a single point failure of the programmable-output overvoltage protection circuit. Other protection features include: LED overload (boost), output undervoltage (buck or buck-boost), input supply (VIN) undervoltage, 5 V regulator (VREG) output undervoltage, high-side supply (PWM PMOS) undervoltage, and thermal protection.

SELECTION GUIDE

Part Number	Packing [1]	Package
A6271KLPTR-T-1	4000 pieces per 13-in. reel	16-pin eTSSOP with exposed thermal pad

[1] Contact Allegro™ for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{IN}		–0.3 to 55	V
PWMOUT, LP, LN, OVUV			–0.3 to 58	V
OSC, DITH, COMP, FAULTn, SG, SP, IREF, PWMIN, DR, VREG			–0.3 to 6.5	V
LP	V_{LP}	With respect to LN	–0.5 to 0.5	V
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[2] With respect to GND.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [3]	Value	Unit
eTSSOP Package	$R_{\theta JA}$	4-layer PCB based on JEDEC standard JESD51-7	34	°C/W
		2-layer PCB with 3.8in^2 of copper area each side	43	°C/W
	$R_{\theta JC}$	Junction to thermal pad	2	°C/W

[3] Additional thermal information available on the Allegro website.

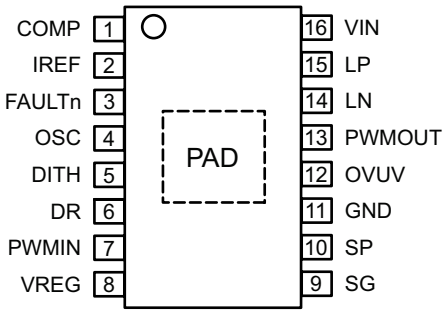
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PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP, 16-Pin eTSSOP Pinout Diagram

Terminal List Table

Symbol	Number	Function
COMP	1	Compensation pin for output of GM error amplifier.
IREF	2	Analog dimming input. With a capacitor connected to this pin, provides a soft-start period when coming out of sleep mode.
FAULTn	3	Open drain. Logic low indicates detection of a fault. Faults include: LED overload (boost), output undervoltage (buck or buck-boost), output overvoltage, programmable overvoltage, input supply (VIN) undervoltage, 5 V Regulator (VREG) output undervoltage.
OSC	4	Oscillator input for setting switching frequency and for external synchronization.
DITH	5	Dither frequency range set. Connect resistor from this pin to GND. Connect to VREG if not used.
DR	6	A voltage applied to this pin programs the duty cycle of PWM internal mode.
PWMIN	7	Used for either putting the device into sleep mode or analog dimming control. Can also be used for external or internal PWM control.
VREG	8	5 V regulator output. Connect filter capacitor from VREG to GND.
SG	9	Switch gate drive output.
SP	10	Switch current sense and slope compensation.
GND	11	Ground.
OVUV	12	Programmable-output overvoltage and undervoltage protection input.
PWMOUT	13	PWM gate drive for external p-channel MOSFET (active low).
LN	14	LED current sense -ve.
LP	15	LED current sense +ve.
VIN	16	Main supply.
PAD	–	Exposed pad provides both electrical contact to the ground and good thermal contact to the PCB. This pad must be soldered to the ground plane preferably by multiple through-hole vias.

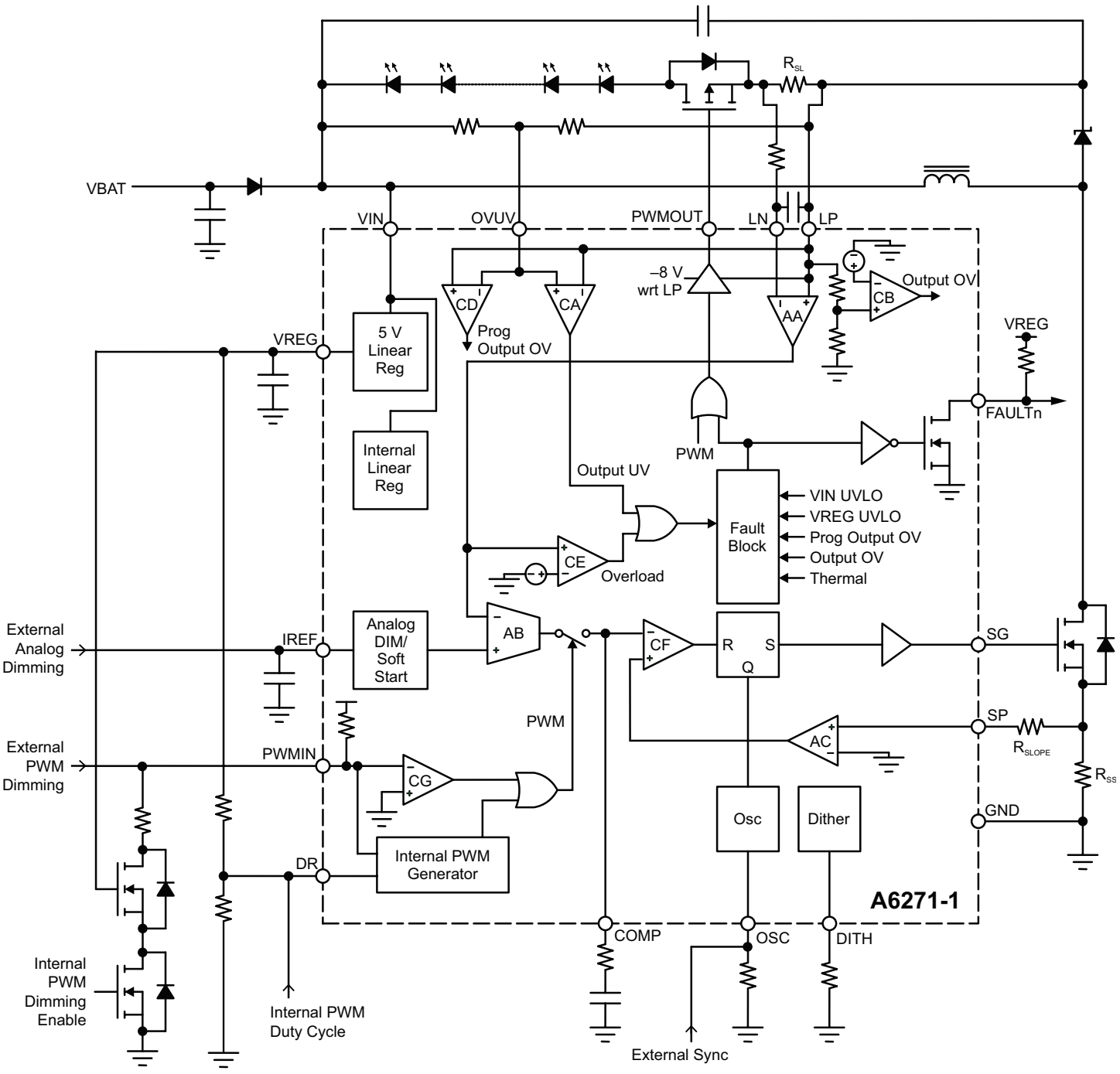


Figure 2: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{IN} = 5 to 45 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY and REFERENCE						
V_{IN} Functional Operating Range [2]	V_{IN}	VIN undervoltage turn off plus VIN undervoltage hysteresis cleared; PWMOUT undervoltage turn-on cleared	4.2	–	50	V
V_{IN} Quiescent Current	I_{INQ}	SG Open Circuit	–	3.5	5	mA
	I_{INS}	PWMIN = GND > disable time	–	6	20	µA
VREG Output Voltage	V_{REG}	I_{REG} = 0 to 2 mA, V_{IN} ≥ 5.3 V	4.85	5.04	5.15	V
		I_{REG} = 2 mA, V_{IN} = 5 V	4.65	–	–	V
VREG Output Voltage [3]	V_{REG}	I_{REG} = 2 mA, V_{IN} = 9 to 45 V, T_J = –40°C to 125°C	4.95	5.05	5.15	V
VREG Current Limit	I_{REGCL}		70	–	–	mA
GATE OUTPUT DRIVE						
Turn-On Time	t_r	C_{LOAD} = 1 nF, 20% to 80%	–	30	–	ns
Turn-Off Time	t_f	C_{LOAD} = 1 nF, 80% to 20%	–	30	–	ns
Minimum Off-Time	$t_{off(MIN)}$		–	135	165	ns
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –100 mA	–	1.7	–	Ω
		T_J = 150°C, I_{GHx} = –100 mA	–	–	3.6	Ω
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 100 mA	–	0.75	–	Ω
		T_J = 150°C, I_{GLx} = 100 mA	–	–	2	Ω
Output High Voltage	V_{SGH}	I_{SG} = –100 µA	V_{REG} – 0.1	–	V_{REG}	V
Output Low Voltage	V_{SGL}	I_{SG} = 100 µA	–	–	0.1	V
LOGIC INPUTS AND OUTPUTS						
FAULTn Output (Open Drain)	V_{OL}	I_{OL} = 1 mA, fault asserted	–	–	0.4	V
FAULTn Output Leakage Current [1]	I_{OH}	V_O = 5.5 V, fault not asserted	–1	–	1	µA
PWMIN Low Voltage	V_{PWMINL}		–	–	0.3	V
PWMIN High Voltage	V_{PWMINH}		2	–	–	V
Input Hysteresis	V_{Ihys}		150	180	–	mV
PWMIN Sleep Pull-Up Current [1]	$I_{PWMSLEEP}$		–	–1.5	–	µA
OSCILLATOR						
Oscillator Frequency	f_{OSC}	R_{OSC} = 51 kΩ	–	500	–	kHz
		R_{OSC} = 73.4 kΩ	315	350	385	kHz
Oscillator Frequency Range [3]	f_{OSC}		70	–	700	kHz
OSC Input Low Voltage	V_{OIL}		–	–	0.8	V
OSC Input High Voltage	V_{OIH}		2	–	–	V
OSC Watchdog Period	t_{OSWD}	Between successive rising edges	17	–	–	µs

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued): **Valid at T_J = –40°C to 150°C, V_{IN} = 5 to 45 V, unless noted otherwise**

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
LED CURRENT SENSE							
Input Bias Current LN	I_{LN}	V_{LP} = V_{LN} = 12 V		–	5	–	µA
Input Bias Current LP	I_{LP}	V_{LP} = V_{LN} = 12 V		–	200	–	µA
Differential Sense Voltage	V_{IDL}	PWMIN = high, V_{IDL} = V_{LP} – V_{LN}, I_{REF} > 1.2 V		200	204	208	mV
Input Common-Mode Range	V_{CMLH}	V_{LP} = V_{LN}		5	–	53.3	V
ANALOG DIMMING							
Disable Time	t_{DISAN}	PWMIN = low		24.8	29	35	ms
Differential Sense Voltage	V_{IDL}	V_{IREF} = 0.5 V		–	102	–	mV
		V_{IREF} = 0.25 V		47	51	55	mV
IREF Maximum Voltage	$V_{IREFMAX}$	Corresponds to sense voltage = 200 mV		–	1	–	V
IREF Minimum Voltage	$V_{IREFMIN}$	Corresponds to sense voltage = 0 mV		–	0	–	V
PWM DIMMING: INTERNAL AND EXTERNAL							
PWMIN to LED Turn-On Time	t_{DIMON}	C_L = 2 nF between PWMOUT and LN		–	270	–	ns
PWMIN to LED Turn-Off Time	t_{DIMOFF}	C_L = 2 nF between PWMOUT and LN		–	210	–	ns
PWMOUT Low Voltage	V_{PWMLO}	LED on, PWMOUT wrt LP, V_{IN} = 10 V		–9	–	–6.5	V
Peak Pull-Up Current [1]	I_{PULLUP}	PWMIN = low, PWMOUT wrt LP = 0 V		–	–25	–	mA
Peak Pull-Down Current	$I_{PULLDOWN}$	PWMIN = high, PWMOUT wrt LP = –8 V		–	50	–	mA
PWM DIMMING: EXTERNAL							
Disable Time	$t_{DISEPWM}$	PWMIN = low		24.8	29	35	ms
PWM DIMMING: INTERNAL							
Maximum PWM Dimming Frequency	f_{PWM}			–	1000	–	Hz
Minimum PWM Dimming Frequency	f_{PWM}			–	200	–	Hz
PWM Dimming Frequency	f_{PWM}	70 kΩ between PWMIN and GND		180	200	220	Hz
PWM Duty Cycle	D_{PWM90}	V_{DR} = 3.24 V, f_{PWM} = 200 Hz	T_J = 25°C	87	90	93	%
			T_J = 150°C	–	90	–	%
	D_{PWM5}	V_{DR} = 180 mV, f_{PWM} = 200 Hz	T_J = 25°C	4.5	5	5.5	%
			T_J = 150°C	–	5	–	%
	D_{PWM0}	V_{DR} = 0 V, f_{PWM} = 200 Hz	T_J = 25°C	–	0.3	–	%
	$V_{DRDCMAX}$	Minimum voltage on DR for 100% duty cycle		–	3.6	–	V
Disable Time	$t_{DISIPWM}$	PWMIN = low		12.4	14.5	17.5	ms
SOFT-START							
Startup Ramp Up Source Current [1]	I_{SOURCE}	Coming out of sleep mode		–	–1	–	µA
Ramp Up Threshold	V_{RAMPUP}	Voltage at IREF pin for 100% LED current		–	1	–	V
Ramp Down Threshold	$V_{RAMPDOWN}$	Voltage at IREF pin for 10% LED current		–	100	–	mV
SWITCH CURRENT SENSE AND AMPLIFIER							
Input Bias Current [1]	I_{BIASS}	V_{SP} = 300 mV, R_{SLOPE} = 1.5 kΩ		–20	–	–	µA
Switch Current Overload Threshold Voltage [3]	V_{IDS}			370	400	440	mV
Voltage Gain	A_{CS}			–	2.25	–	V/V

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued): **Valid at T_J = –40°C to 150°C, V_{IN} = 5 to 45 V, unless noted otherwise**

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SLOPE COMPENSATION						
Peak Current [1]	I_{SLOPE}	Sawtooth current waveform added to current-sense input (SP)	–116	–	–93	µA
GM AMPLIFIER						
Open Loop DC Gain	A_{VEA}		–	62	–	dB
Transconductance	g_{mCOMP}		1100	1500	1900	µA/V
COMP Sink Current [1]	I_{COMP}		–	290	–	µA
COMP Source Current [1]	I_{COMP}		–	–105	–	µA
COMP Leakage Current [1]	I_{LCOMP}		–	±200	–	nA
DITHER GENERATOR						
Dither Modulation Frequency	f_{DITH}		7.9	9.6	11.2	kHz
Maximum Switching Frequency	f_{OSCMAX}	R_{OSC} = 72 kΩ, R_{DITH} = 110 kΩ	348	400	452	kHz
Minimum Switching Frequency	f_{OSCMIN}	R_{OSC} = 72 kΩ, R_{DITH} = 110 kΩ	261	300	339	kHz
PROTECTION FEATURES						
Fault Blank Timer [4]	t_{FB}	Startup	–	3	–	ms
VIN Undervoltage Turn-Off	V_{INUV}	Decreasing V_{IN} , I_{REG} = 2 mA	3.9	–	4.2	V
VIN Undervoltage Hysteresis	ΔV_{INUV}		250	–	380	mV
VREG Undervoltage Turn-Off	V_{REGUV}	Decreasing V_{REG}	3.25	–	3.5	V
VREG Undervoltage Hysteresis	ΔV_{REGUV}		–	300	–	mV
LED Overcurrent Threshold	V_{OCLED}	LP wrt LN	260	320	380	mV
Fixed-Output Overvoltage Threshold	V_{FOOV}	Monitored at LP pin with respect to GND	53.3	55.5	57	V
Programmable-Output Overvoltage Threshold	V_{POOV}	OVUV wrt LP	–1.24	–1.1	–1	V
Output Undervoltage Threshold	V_{OUV}	OVUV wrt LP	–110	–85	–60	mV
Switch Current Overload Period	t_{SCOP}	Inner loop switch current	–	64	–	clock cycles
LED Overcurrent Period	t_{OPI}		–	2	–	clock cycles
LED Output Undervoltage Period	t_{OPV}		–	30	–	clock cycles
Hiccup Shutdown Period	t_{HIC}	LED overcurrent, or output undervoltage, or overvoltage, or switch overload	22	26.5	31.75	ms
PWMOUT Undervoltage Turn-On	$V_{PWMUVON}$	Measured at LP wrt GND	–	–	6	V
PWMOUT Undervoltage Turn-Off	$V_{PWMUVOFF}$	Measured at LP wrt GND	3.7	–	5.8	V
Overtemperature Shutdown Threshold	T_{JF}	Temperature increasing	155	170	–	°C
Overtemperature Hysteresis	ΔT_J	Recovery = $T_{JF} - \Delta T_J$	–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2] Function is correct, but some parameters may not meet specification.
[3] Parameters guaranteed by design and characterization.
[4] Fault blank timer only enabled for either output undervoltage or switch current overload.

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FUNCTIONAL DESCRIPTION

The A6271-1 is a DC-DC converter controller designed to drive series-connected high-power LEDs in automotive applications. The A6271-1 can be configured in a variety of switching topologies, including: boost, buck-boost, SEPIC, and buck (ground-referenced switch). For each switching configuration, the appropriate loop compensation (COMP) and slope compensation (SLOPE) passive components are selected for optimal performance.

The A6271-1 integrates all the necessary control elements to provide a cost-effective solution using an external logic-level, n-channel MOSFET (switching device), p-channel MOSFET (PWM device), and minimum additional external passive components. The maximum LED current is set with a single external sense resistor and can be accurately modulated using a current reference input (analog control). Direct PWM control is possible via the PWMIN input, which also provides a shutdown mode.

Circuit Operation

CONVERTER

The controller is based on a fixed-frequency, peak current-mode control architecture. There are two loops within the controller. The inner loop, formed by the amplifier AC (refer to Functional Block Diagram), the slope generator, the comparator, CF, and the RS bistable, controls the inductor current as measured through the switching MOSFET by the sense resistor R_{SS}. The outer loop, formed by the amplifier AA and the integrating GM amplifier AB, controls the average LED current by providing the current demand signal for the inner loop.

The LED current is measured by the sense resistor, R_{SL}, and is averaged and amplified to a level where it is compared to the internal reference current to produce an error signal at the output of the GM amplifier, AB. This error signal is effectively the current demand signal and determines the amount of energy transferred to the LEDs on a cycle-by-cycle basis via the inner loop.

The control loops work together as follows: at the beginning of each oscillator cycle, the bistable is set and the switching MOSFET is on. The switch current builds up due to the voltage developed across the inductor, and when the corresponding signal produced at the output of amplifier AC reaches the current demand level on the output of amplifier AB, the bistable is reset and the switching MOSFET is turned off. The cycle is repeated on the next oscillator cycle.

If the current through the LEDs increases, the output of AA increases, causing the current demand signal to decrease. This reduces the amount of energy transferred to the LED load by terminating the switch current sooner and reducing the LED current.

EXTERNAL PULSE-WIDTH MODULATION DIMMING

An external logic signal can be applied to PWMIN pin to control the on/off of LED current. Average brightness of the LED is directly proportional to the duty cycle of the control signal. This technique is commonly known as PWM dimming.

During PWM operation, when PWMIN is pulled low, the LED stack PWMOUT is pulled high with respect to LP, turning off the external p-channel MOSFET, isolating the LED string. In addition, the GM output (amplifier AB) is 'parked' (COMP components disconnected) at the new level and the gate drive (SG) is disabled. As the output capacitance is isolated from the LED string, there is no loss of charge.

When PWMIN goes high impedance, or is pulled high, the COMP components are reconnected (with the previous 'parked' value'), the gate drive (SG) is enabled, PWMOUT is pulled to around –8 V with respect to LP turning on the external MOSFET and allowing current to flow through the LED string.

INTERNAL PULSE-WIDTH MODULATION DIMMING

Where an external PWM signal is not available, the internal PWM generator can be used for controlling the LED brightness. A resistor connected between the PWMIN pin and GND sets the PWM frequency according to the following formula:

$$R_{FREQ} = \frac{14{,}000}{f_{PWM}}$$

where R_{FREQ} is in kΩ and f_{PWM} is in Hz.

The duty cycle is controlled by applying a voltage to the DR pin. The VREG can be used for the supply voltage and a potential divider can be used to set the DR voltage. An additional resistor can be added in parallel via a MOSFET switch between DR and GND to change the duty cycle between two levels.

The relationship between the DR voltage and the duty cycle is as follows:

$$PWM\ Duty\ cycle\ (\%) = 27.81 \times DR\ voltage$$

So, for example, with a DR voltage = 1.8 V, the programmed duty cycle = 50%.

In terms of the control of the external MOSFET via the PWM-

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OUT pin, the control is identical as the external PWM scheme. If no internal PWM is required, the DR pin should be connected to VREG. Also note that whenever an external PWM signal is applied to the PWMIN pin, it overrides the internal PWM operation.

When using the internal PWM scheme, an n-channel MOSFET is required to open the ground connection of the resistor connected between PWMIN and GND to ensure that startup occurs. The gate of the MOSFET is connected to VREG as shown in Figure 11 and Figure 13, or to an external control signal as shown in Figure 12 and Figure 14.

As the PWMIN input has a pull-up of only 1.1 µA in sleep mode, it is essential that the zero gate voltage, drain current (leakage) of the MOSFET does not exceed this number at maximum ambient temperatures.

ANALOG DIMMING

The IREF pin can then be used for full analog control. The LED current can be linearly adjusted from zero to full (100%) LED current (I_{LED}) by changing the IREF pin from 0 to ≥ 1 V.

This feature is useful in applications where PWM control is either not required or not available and the LEDs require some dynamic correction for brightness adjustment.

Analog dimming can be used along with either pulse-width-modulation technique, internal or external. This is useful for applications where some color correction is required along with brightness control.

Soft-start can be provided via the analog dim signal when either coming out of sleep or hiccup mode. The internal 1 µA internal source current on the IREF node can be overridden by applying a ramp signal to IREF. The soft-start duration is controlled by the signal on IREF as it is ramped from 0 to 1 V.

If no soft-start is required, the IREF pin should be connected to VREG.

SOFT-START

When the A6271-1 comes out of sleep mode, soft-start is required to bring the output voltage up in a controlled open-loop fashion. This minimizes the possibility of the control loop saturating during the startup phase and subsequent output voltage overshoot, which can induce high transient peak currents in the LED string prior to the loop being brought back into linear control.

The soft-start period can be programmed by the selection of the appropriate capacitor between IREF pin and GND pin according to the following formula:

$$C_{soft} = \frac{t_{soft} \times 1 \times 10^{-6}}{1.2}$$

where t_{soft} is the desired soft-start period.

If analog dimming is applied, the equivalent current source from this circuit will add to the internal 1 µA source current on the IREF node. Generally speaking, when using analog dimming via VREG and a potential divider, no soft-start or negligible soft-start is provided as shown in the example below. References are taken from Figure 9 on page 23:

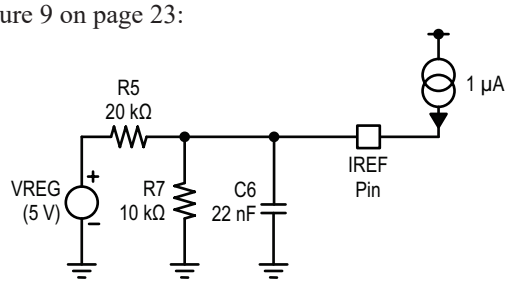


Figure 3: Charging Of Soft-Start Cap During Power Up

From the above diagram, VREG, R5, and R7 can be simplified using Norton's Theorem.

The equivalent resistance can be found:

$$R_T = \frac{20 \times 10}{20 + 10} = 6.67\ k\Omega$$

The current source can be found:

$$I_{source} = \frac{5}{R_T} = 750\ \mu A$$

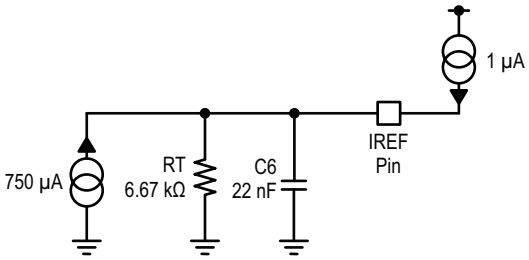


Figure 4: Equivalent Circuit Of The Previous Diagram

From the above schematic, it is clear that the 750 µA current source will dominate and almost no soft-start will be provided. In this particular case, the only option is to resize C6, or increase the values of R5 and R7, or both.

LED CURRENT-SENSE RESISTOR

The LED current is programmed by the LED sense resistor, R_{SL}, according to:

$$I_{LED} = \frac{V_{IDL}}{R_{SL}}$$

where the loop typically regulates V_{IDL} to 200 mV when in either internal or external PWM modes.

The power loss of the resistor should be taken into account to ensure the correct package size is selected.

The power loss of the LED current-sense resistor, R_{SL} is:

$$P = I_{LED}^2 \times R_{SL}$$

It is advisable to insert a 150 Ω resistor in series with the LN pin, as shown below, to protect the internal ESD structures between LN and LP under certain fault conditions. The 150 Ω value is selected as a balance between limiting the fault current and minimizing the LED current error caused by the bias current flowing into the LN pin. A small cap (such as 47 nF) may be added between LP and LN pin. It helps to filter switching noises from current sense signal.

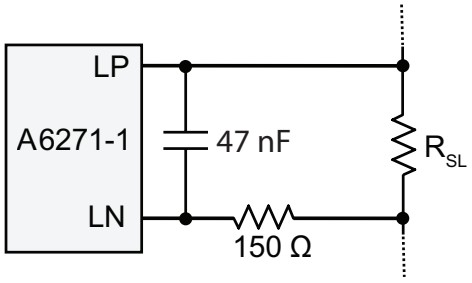


Figure 5: Recommended Current Sensing Network

SLEEP MODE

If PWMIN is held low for longer than the disable time, t_{DIS1} or t_{DIS2}, then the A6271-1 will shut down and put the majority of the circuitry into a low-power sleep mode.

When internal PWM dimming is used, the disable time, t_{DIS1}, is 14.5 ms.

When either external PWM dimming or analog dimming is used, the disable time, t_{DIS2} is 29 ms.

5 V REGULATOR, VREG

To provide a filtered output and to ensure the regulator is stable, a 1 µF ceramic capacitor is required to be connected between VREG and GND. The ceramic type should be a quality type such as X5R, X7R, or X8R.

The 5 V regulator is sized for driving the external switching MOSFET. However, it can be used for functions that require minimal current, e.g. pulling up the FAULTn output and providing a reference for the DR, the IREF pin, or both.

To check the load that the MOSFET provides, it is necessary to check the total gate charge required for a 5 V drive. This can be derived from the gate charge, Q_G, versus gate drive voltage, V_{GS}, from the MOSFET datasheet. Once the gate charge is found, the regulator load current can be determined:

$$I_{LOAD} = (Q_G \times f_{SW}) + I_{external}$$

where $I_{external}$ is the additional circuitry added to the VREG output.

The I_{LOAD} should not exceed the VREG external current limit (I_{REGCL}).

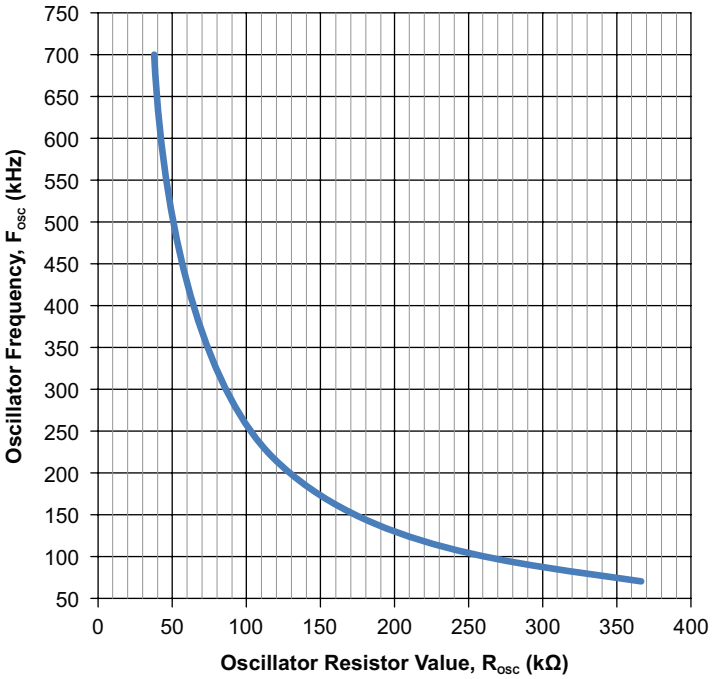


Figure 6: R_{OSC} Required for a Particular Oscillator Frequency

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OSCILLATOR

The main oscillator may be configured as a clock source or it may be driven by an external clock signal. The oscillator is designed to run between 70 and 700 kHz.

When the oscillator is configured as a clock source, the frequency is programmed via an external resistor between OSC pin and GND pin. The appropriate resistor can be found:

$$R_{OSC} = \frac{25{,}690}{f_{OSC}}$$

where R_{OSC} is in kΩ and f_{OSC} is in kHz.

Figure 4 shows the resulting R_{OSC} for various frequencies.

When the OSC pin is driven by an external clock source, a number of A6271-1s can be synchronized together. If the clock period is greater than or equal to 17 µs, a watchdog circuit causes the running frequency to default to the internal oscillator, which runs at 350 kHz.

If the oscillator pin goes either open circuit or short circuits to GND, the running frequency defaults to 350 kHz.

FREQUENCY DITHERING

To assist in minimizing EMI emissions, the main oscillator can be dithered so that the energy is spread over a defined frequency band. The defined frequency band is effectively the minimum and maximum switching frequency selected. This frequency is varied above and below the selected oscillator frequency and is set via a resistor connected between Dither pin and GND pin. The frequency band can be selected as follows:

$$\Delta f = \pm 22 \times \frac{R_{OSC}}{R_{DITH}}$$

where Δf is a plus/minus percentage change with respect to the oscillator frequency.

For example, if an oscillator frequency of 350 kHz and a dithered frequency band of ±50 kHz was selected, given a minimum switching frequency of 300 kHz and a maximum switching frequency of 400 kHz, the R_{OSC} and R_{DITHER} can be found:

$$R_{OSC} = \frac{25{,}690}{f_{OSC}}$$

$$R_{OSC} = \frac{25{,}690}{350} = 73.4\ k\Omega,\ say\ 72\ k\Omega$$

Δf as a percentage of the delta with respect to the oscillator frequency is (50 / 350) × 100% = 14.3%.

Therefore, R_{DITH} can be found from:

$$\Delta f = \pm 22 \times \frac{R_{OSC}}{R_{DITH}}$$

$$R_{DITH} = 22 \times \frac{72}{14.3} = 110\ k\Omega$$

The switching frequency is modulated at a rate of 10 kHz via a triangular waveform. This means in one modulation cycle, the switching frequency varies linearly from a minimum to a maximum to a minimum again.

If the dither feature is not required, the DITH pin should be tied to VREG.

PROTECTION

The A6271-1 includes a number of safety features to ensure the controller, the external power components, and the LED string are protected.

The Fault Flag becomes active (pulled low) for any fault.

When the device recovers from a fault, a soft-start is performed unless analog dimming is selected and the DR pin is tied to VREG.

After the LED current has returned to regulation for 1 ms, the FAULT pin is then released. This allows the FAULT flag to be used as a 'Power Good' signal.

Note: If IREF pin is held below 0.1 V (corresponding to <10% analog dimming) at startup, the IC cannot reliably determine whether LED current has reached regulation. Therefore FAULT flag may remain low even though LED current is being regulated.

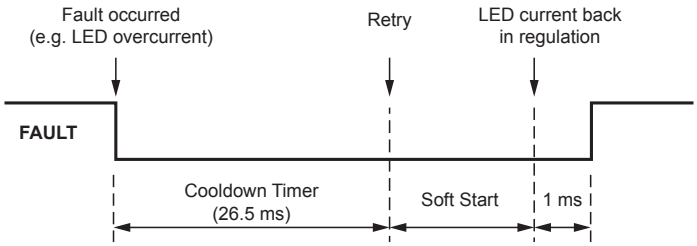


Figure 7: Fault Recovery

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At initial startup, when coming out of sleep mode, or when the hiccup period terminates, a fault blank period, t_{FB}, of 3 ms is applied for two fault conditions: low-side switch current limit (inner loop), and LED overload (caused by an undervoltage), before the fault circuitry becomes active. This period allows steady-state conditions to occur before fault monitoring takes place.

Output Overvoltage Protection

Two overvoltage protection circuits exist: an internal fixed circuit and an externally programmable circuit. In the majority of applications, the externally programmable circuit will provide the protection. The internal circuit is present in the event that the external feedback resistor chain of the programmable circuit goes open circuit. This feature is particularly desirable in systems that require high levels of reliability and the ability to withstand failure modes. Another advantage is the possibility, in lower voltage applications, to select reduced operating voltages for the switching MOSFET, PWM MOSFET, recirculation diode, and output filter capacitors with confidence.

If an overvoltage occurs in either of the two circuits, the high-side MOSFET drive (PWMOUT) and the low-side MOSFET drive (SG) are immediately disabled and FAULTn is active. After one fault mask switching cycle, the hiccup timer, t_{HIC}, is initiated for a period of 26.5 ms. At the beginning of the hiccup period, the IREF node (soft-start) capacitor is discharged immediately. After the hiccup period, an auto-restart is performed under control of the soft-start capacitor.

A potential divider is set up between the LP node (output of the converter) and the cathode end of the LED stack. The output of the potential divider is monitored by a comparator referenced to the LP node. Once this voltage decreases below –1 V(max), an overvoltage condition is reported.

It is recommended that the impedance of the potential divider is kept relatively high, especially in high-voltage LED strings, to minimize the current draw. It should be noted that there is negligible bias current drawn by the comparator monitor circuit.

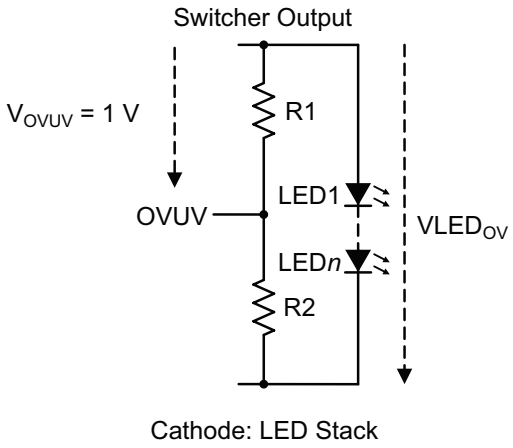


Figure 8: Setting the OVUV Resistor Network

As an example, consider an LED string which has a maximum LED string voltage of 45 V and an output overvoltage ($VLED_{OV}$) is to be reported at a minimum of 15% above this value.

R2 can be found:

$$R2 = \frac{R1 \times (VLED_{OV} - V_{OVUV})}{V_{OVUV}}$$

Assume resistor R1 is selected to be 4.3 kΩ.

$VLED_{OV}$ is 1.15 × 45 = 52 V.

V_{OVUV} is a minimum of 1 V.

From the above formula:

$$R2 = \frac{4.3 \times (52 - 1)}{1} = 219\ k\Omega, \text{ select } 220\ k\Omega$$

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Overload Protection

There are two circuits:

1. LED overcurrent threshold
2. Output undervoltage threshold

In the case of a LED overcurrent fault, the high-side MOSFET drive (PWMOUT) and the low-side MOSFET drive (SG) are disabled after two fault mask switching cycles, FAULTn is active, the IREF node (soft-start) capacitor is discharged, then the hiccup timer, t_{HIC}, is initiated for a period of 26.5 ms. After the hiccup period, an auto-restart is performed under control of the soft-start capacitor.

In the case of an output undervoltage fault, the high-side MOSFET drive (PWMOUT) is immediately disabled and FAULTn is active. After thirty fault mask switching cycles, the low-side MOSFET drive (SG) is disabled, IREF node (soft-start) capacitor is discharged, and the hiccup timer, t_{HIC}, is initiated for a period of 26.5 ms. After the hiccup period, an auto-restart is performed under control of the soft-start capacitor.

Low-Side Switch Current Limit (inner loop)

At startup, a 3 ms blank period is applied before the circuitry becomes active. Cycle-by-cycle current protection is provided through the low-side MOSFET. If an overcurrent occurs for longer than 64 switching clock cycles, the high-side MOSFET drive (PWMOUT) and the low-side MOSFET drive (SG) are disabled, FAULTn is active, and the hiccup timer, t_{HIC}, is initiated for a period of 26.5 ms. During the hiccup period, the IREF node (soft-start) capacitor is discharged immediately. After the hiccup period, an auto-restart is performed under control of the soft-start capacitor.

Input Undervoltage or VREG Undervoltage Protection

If either condition occurs, the low-side MOSFET drive (SG) is disabled and FAULTn is active (assuming VREG is high enough, if FAULTn is pulled to VREG). In the case of the input undervoltage, the high-side MOSFET drive (PWMOUT) is also disabled.

Both the input voltage and the VREG voltage must rise above their respective turn-on thresholds before a restart is possible. In the case of startup through the input voltage turn-on threshold, the system is brought up under control of the soft-start. In the case of startup through the VREG turn-on threshold, no soft-start is provided.

PWM Output Undervoltage

During startup, the output (LP node) must increase above 6 V to ensure the high-side MOSFET turns on. This is generally not a problem with switching topologies that can boost the output voltage with respect to the input voltage. In the case of the buck topology, the LN/LP node is referenced to VIN; therefore, the input voltage has to be equal to or greater than 6 V to guarantee a successful startup. In SEPIC, the output needs to be at least 6 V, while the input may be as low as 4.2 V.

Overtemperature Shutdown

If the chip exceeds the overtemperature shutdown threshold, the low-side MOSFET drive (SG) is immediately disabled, FAULTn is active, and the IREF node (soft-start) capacitor is discharged immediately. An auto-restart is performed under control of the soft-start capacitor once the temperature drops below the overtemperature minus the hysteresis level.

The table on the following page summarizes the above faults along with other pin specific faults.

Table 1: Fault Table

Fault	Action
Low-Side Switch Current Limit	When fault occurs, cycle-by-cycle current limit operates. If fault >64 counts: low-side MOSFET (SG) and PWM MOSFET (PWMOUT) off and FAULTn active, hiccup period, then auto-restart with soft-start. Note: fault blanked for 3 ms during startup.
LED Overcurrent	Low-side MOSFET (SG) and PWM MOSFET (PWMOUT) immediately off and FAULTn active, hiccup period after 2 counts, then auto-restart with soft-start.
Output Undervoltage	PWM MOSFET (PWMOUT) immediately off. FAULTn active. Low-side MOSFET (SG) continues switching for 30 cycles. If fault still exist after 30 cycles, IC stops switching and enters hiccup period, then auto-restart with soft-start. Note: this undervoltage fault detection is blanked for 3 ms during startup.
Fixed-Output Overvoltage	Low-side MOSFET (SG) off and PWM MOSFET (PWMOUT) immediately turns off and FAULTn active, hiccup period after 1 count, then auto-restart with soft-start.
Programmable-Output Overvoltage	Low-side MOSFET (SG) off and PWM MOSFET (PWMOUT) immediately turns off and FAULTn active, hiccup period after 1 count, then auto-restart with soft-start.
Input Undervoltage	Low-side MOSFET (SG) and PWM MOSFET (PWMOUT) immediately turns off and FAULTn active assuming there is sufficient drive to the flag. Once input voltage is above the VIN undervoltage threshold, plus hysteresis, auto-restart with soft-start occurs.
VREG Undervoltage	Low-side MOSFET (SG) immediately turns off and FAULTn active assuming there is sufficient drive to the flag. Once VREG voltage is above the VREG undervoltage threshold, plus hysteresis, then auto-restart.
Thermal Shutdown	Low-side MOSFET (SG) immediately turns off and FAULTn active. Auto-restart with soft start occurs after the temperature drops below the overtemperature minus hysteresis level.
PWMOUT Undervoltage	PWM MOSFET (PWMOUT) off immediately and FAULTn active. Low-side MOSFET (SG) continues switching to pump up output voltage. Once LP rises above $V_{PWMUVON}$, PWMOUT is re-activated.
OSC Pin Fault	The oscillator will switch to default frequency of 350 kHz.
COMP Short to GND	Force regulator to minimum duty cycle.

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COMPONENT SELECTION

Inductor

The main factor in selecting the inductor value is to target a certain ripple current to ensure the peak current-mode control works correctly. A reasonable figure is a peak-to-peak ripple current of around 15% of the average inductor current. The maximum inductor current occurs at minimum input voltage and maximum duty cycle.

BOOST INDUCTOR SELECTION

The maximum duty cycle can be found:

$$D_{MAX} = \frac{V_{LED} + (V_f - V_{IN(MIN)})}{V_{LED} + V_f}$$

where V_{LED} is the LED output voltage, V_f is the forward voltage drop of the recirculation diode, and $V_{IN(MIN)}$ is the minimum input voltage.

The maximum average inductor current can be determined:

$$I_{AVE} = \frac{I_{LED}}{(1 - D_{MAX})}$$

The ripple current, $\Delta I = 0.15 \times I_{AVE}$.

The minimum inductance can now be found:

$$L = \frac{(V_{LED} + V_f - V_{IN(MIN)}) \times (1 - D_{MAX})}{\Delta I \times f_{SW}}$$

where f_{SW} is the switching frequency.

The peak current in the inductor is:

$$I_{LPK} = I_{AVE} + \frac{\Delta I}{2}$$

BUCK-BOOST INDUCTOR SELECTION

The maximum duty cycle can be found:

$$D_{MAX} = \frac{V_{LED} + V_f}{V_{LED} + V_f + V_{IN(MIN)}}$$

where V_{LED} is the LED output voltage, V_f is the forward voltage drop of the recirculation diode, and $V_{IN(MIN)}$ is the minimum input voltage.

The maximum average inductor current can be determined:

$$I_{AVE} = \frac{I_{LED}}{1 - D_{MAX}}$$

The ripple current, $\Delta I = 0.15 \times I_{AVE}$.

The minimum inductance can now be found:

$$L = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta I \times f_{SW}}$$

where f_{SW} is the switching frequency.

The peak current in the inductor is:

$$I_{LPK} = I_{AVE} + \frac{\Delta I}{2}$$

When selecting an inductor from manufacturers' datasheets, there are often two current ratings given:

1. Saturation current. This is the current level that causes the inductance to drop by between 10 and 40% depending on the manufacturer.
   The saturation current should be greater than the peak current, I_{LPK}, with some margin to allow for overload conditions.
2. RMS or average current. This is the current level that determines a certain temperature rise in the inductor with a given ambient temperature. This is normally presented as a single figure: operating temperature.
   The RMS or average inductor current rating should be greater than the estimated maximum average current, I_{AVE}.

Recommended inductor manufacturers:

- Coilcraft: MSS1278T or MSS1078T Range
- TDK: SLF12575 type H

SWITCH CURRENT SENSE

The switch current sense of the 'inner loop' is measured by the external sense resistor, R_{SS}, and the switch sense amplifier, AC. As well as providing the peak current information to determine the duty cycle, it also provides pulse-by-pulse current limiting through the switching MOSFET and slope compensation to prevent subharmonic oscillations at duty cycles greater than 50%.

The current limit of the inner loop is set by the input limit of the sense amplifier, V_{IDS}, the maximum switch current that has been determined, and the effects of the slope compensation have to be taken into account. The operating duty cycle has to be calculated at maximum load and minimum operating input voltage. The amount of slope compensation can be calculated for this operating point and can then be added to the actual current-sense signal to determine the maximum signal amplitude before cycle-by-cycle current limiting takes effect. Refer to Slope Compensation Section to find di_L/dt then di_{SLOPE}/dt.

$$R_{SS} = \frac{0.32}{1.2 \times \left(I_{LP} + \left(\frac{di_{SLOPE}}{dt} \times \frac{D_{MAX}}{F_{SW}} \right) \right)}$$

Note that the minimum value of V_{IDS} is used with an additional 20% to allow for margin.

I_{LP} is the peak current in the inductor.

The power loss of the switch current-sense resistor, R_{SS}, can be found:

Boost R_{SS} Power Loss

Using the D_{MAX} and I_{AVE} from the boost part of the inductor section, the power loss of R_{SS} can be found:

$$P_{loss} = I_{AVE}^2 \times D_{MAX} \times R_{SS}$$

Buck-Boost R_{SS} Power Loss

Using the D_{MAX} and I_{AVE} from the buck-boost part of the inductor section, the power loss of R_{SS} can be found:

$$P_{loss} = I_{AVE}^2 \times D_{MAX} \times R_{SS}$$

Resistor manufacturers typically derate the devices from an ambient temperature of around 70°C. The power rating including derating of the sense resistor should exceed the maximum power loss at maximum ambient temperature.

SLOPE COMPENSATION

Slope compensation can be added to the MOSFET current-sense signal on pin SP to prevent subharmonic oscillations where the peak-to-average control error becomes increasingly larger at duty cycles in excess of 50%. A current source is provided at the SP pin as a sawtooth from 0 to 100 µA. An external resistor, R_{SLOPE}, connected between the SP pin and the source connection of the MOSFET, is used to program the appropriate voltage level to scale the slope compensation for correct use with the appropriate topology and set up conditions that have been adopted.

Boost Slope Resistor

The inductor down slope is:

$$\frac{di_L}{dt} = \frac{V_{LED} + V_f - V_{IN(MIN)}}{L}$$

Buck-Boost Slope Resistor

The inductor down slope is:

$$\frac{di_L}{dt} = \frac{V_{LED} + V_f}{L}$$

The optimum down slope as illustrated by Ridley can be found from:

$$\frac{di_{SLOPE}}{dt} = \frac{di_L}{dt} \times \left(1 - \frac{0.18}{D_{MAX}}\right)$$

The slope compensation resistor can be found:

$$R_{SLOPE} = \frac{\frac{di_{SLOPE}}{dt} \times R_{SS}}{100 \times 10^{-6} \times 1 \times 10^{-6} \times f_{SW}}$$

where R_{SLOPE} is in ohms (Ω).

CONTROL LOOP COMPENSATION

The recommended way of closing the control loop is to remove the influence of the right-hand plane zero (RHPZ) in both boost and buck-boost topologies. The reason for this is that the RHPZ increases the gain by 20 dB/decade and at the same time introduces a 90-degree phase lag.

The minimum frequency that the RHPZ occurs at is:

For boost mode:

$$f_{RHPZ} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED}}$$

For buck-boost mode:

$$f_{RHPZ} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED} \times D_{MAX}}$$

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It is recommended that the 0 dB crossover point is approximately:

$$f_{CROSS} = \frac{f_{RHPZ}}{5}$$

With effective peak current-mode control, it can be assumed that the second power pole is pushed high enough in the frequency domain to have no influence on the overall loop response. It is reasonable to assume the overall loop response is effectively a single pole set by the GM amplifier (COMP node). The error amp zero is set at the same frequency as the output power pole to ensure the loop is closed at a rate of 20 dB/decade.

The open-loop DC gain of the system can be found:

Boost:

$$DC\ Gain = \frac{5 \times 1{,}259 \times R_{SL} \times (1 - D_{MAX}) \times \left(\frac{V_{LED}}{I_{LED}}\right)}{R_{SS} \times \left(\left(\frac{V_{LED}}{I_{LED}}\right) + (n \times R_{dyn}) + R_{SL}\right)}$$

Buck-Boost:

$$DC\ Gain = \frac{5 \times 1{,}259 \times R_{SL} \times (1 - D_{MAX}) \times \left(\frac{V_{LED}}{I_{LED}}\right)}{R_{SS} \times \left(\left(\frac{V_{LED}}{I_{LED}}\right) + D_{MAX} \times ((n \times R_{dyn}) + R_{SL})\right)}$$

where n = number of LEDs and R_{dyn} = LED dynamic resistance.

Note that the LED dynamic resistance may be given in the LED datasheet. If it is not, it can be derived by a simple measurement. Set up a power supply with a current limit at the operating point (I_{LED1}). Apply the current to an individual LED and measure the voltage drop (V_{LED1}). Change the current limit by a small amount, say 5% (I_{LED2}), and measure the voltage drop (V_{LED2}). The dynamic resistance can be estimated:

$$R_{dyn} = \frac{V_{LED1} - V_{LED2}}{I_{LED1} - I_{LED2}}$$

The RC constant required to achieve 0 dB with a slope of 20 dB/decade at the crossover frequency, f_{CROSS}:

$$RC = \frac{1}{2 \times \pi \times f_{CROSS}}$$

The frequency of the first GM amplifier pole can be found:

$$f_{p1} = \frac{1}{2 \times \pi \times RC \times DC\ Gain}$$

Capacitor on the output of the GM amplifier (COMP node) required to achieve the above pole position:

$$C_{comp} = \frac{750 \times 10^{-6}}{2 \times \pi \times f_{p1} \times 1{,}258}$$

The frequency position of the power stage pole and the GM amplifier zero is:

Boost:

$$f_{p2}\ and\ f_{z1} = \frac{V_{LED} + I_{LED} \times ((n \times R_{dyn}) + R_{SL})}{2 \times \pi \times V_{LED} \times C_{OUT} \times ((n \times R_{dyn}) + R_{SL})}$$

Buck-Boost:

$$f_{p2}\ and\ f_{z1} = \frac{V_{LED} + D_{MAX} \times I_{LED} \times ((n \times R_{dyn}) + R_{SL})}{2 \times \pi \times V_{LED} \times C_{OUT} \times ((n \times R_{dyn}) + R_{SL})}$$

The resistor (R_{comp}) in series with the compensation capacitor (C_{comp}) on the COMP node can be found:

$$R_{comp} = \frac{1}{2 \times \pi \times f_{p2} \times C_{comp}}$$

LOW-SIDE SWITCHING MOSFET

A logic-level n-channel MOSFET is used as the switch for the DC-DC converter.

In the boost configuration, the maximum voltage across the drain-source connection is:

$$V_{DS} = V_{LED} + V_f$$

In the buck-boost configuration, the maximum voltage across the drain-source connection is:

$$V_{DS} = V_{LED} + V_f + V_{INMAX}$$

The actual rating of the MOSFET selected should be greater than the maximum voltage plus some margin. It is recommended that the minimum margin should be no less than 20% of the maximum voltage.

In the case of buck-boost mode, the maximum rating should factor in load-dump conditions.

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In terms of the current rating, the MOSFET is generally selected for a low R_{DS} rating to minimize the power dissipation. This means the current rating is well in excess of the actual maximum current used in the application.

The power loss in the MOSFET is determined by the static loss and the switching losses.

Static Loss

Using the D_{MAX} and I_{AVE} from the boost or buck-boost part of the inductor section, the power loss of R_{DS} can be found:

$$P_{loss} = I_{AVE}^2 \times D_{MAX} \times R_{DS}$$

Note that the R_{DS} figures are generally presented at 25°C room ambients. The actual R_{DS} can be determined by considering the normalized R_{DS} versus temperature graph.

Another consideration of the static loss is cold-crank situations. It is important to ensure the gate-drive amplitude (derived from VREG) at the minimum input voltage provides sufficient drive that the R_{DS} does not increase by much, therefore minimizing any increase in losses. A good quality logic-level MOSFET should have good R_{DS} performance at drive voltages of less than 4 V.

The VREG load can be determined by estimating the gate losses. From the MOSFET datasheet, the total gate charge can estimated with a gate drive of 5 V using the appropriate graph. In addition, any other circuitry that VREG is powering should also be factored. The current drawn from VREG due to the MOSFET drive can be determined:

$$VREG_{MOSFETload} = Q_{TOTALGate} \times f_{SW}$$

Switching Losses

The switching losses in the MOSFET are determined by the length of time of the Miller region. To minimize conducted and radiated EMI emissions, this region is deliberately extended by adding series resistance between the gate drive (SG) and the gate of the device. It is assumed that the turn-off loss is similar to the turn-on loss.

In the case of the boost converter, the switching loss:

$$P_{switch} = (V_{LED} + V_f) \times I_{AVE} \times t_{miller} \times f_{SW}$$

In the case of the buck boost converter, the switching loss:

$$P_{switch} = (V_{LED} + V_f + V_{IN(MIN)}) \times I_{AVE} \times t_{miller} \times f_{SW}$$

RECIRCULATION DIODE

The diode should have a low forward voltage to reduce conduction losses and a low capacitance to reduce switching losses and minimize EMI. Schottky diodes can provide both features if carefully selected. The forward voltage drop is a natural advantage for Schottky diodes and reduces as the current rating increases. However, as the current rating increases, the diode capacitance also increases, so the optimum selection is usually the lowest current rating above the required maximum, in this case I_{LPK}.

In the boost configuration, the maximum reverse voltage across the diode is:

$$V_{RRM} = V_{LED} + V_f$$

In the buck-boost configuration, the maximum reverse voltage across the diode is:

$$V_{RRM} = V_{LED} + V_f + V_{IN(MAX)}$$

The actual rating of the diode selected should be greater than the maximum voltage plus some margin. It is recommended that the minimum margin should be no less than 20% of the maximum voltage. In the case of buck-boost mode, the maximum rating should factor in load-dump conditions.

HIGH-SIDE PWM MOSFET

A p-channel MOSFET is used as the PWM switch for the LED stack.

In both boost and buck-boost modes, the maximum voltage across the drain-source connection is V_{LED}. The actual rating of the MOSFET selected should be greater than the maximum voltage plus some margin. It is recommended that the minimum margin should be no less than 20% of the maximum voltage.

The power loss of this MOSFET is dominated by the static loss. The switching losses can largely be ignored as the PWM frequencies are relatively low.

The power loss of the MOSFET R_{DS} can be found:

$$P_{loss} = I_{LED}^2 \times R_{DS}$$

The gate drive for the PWM MOSFET is derived from the LED output rail (LP pin). In boost and buck-boost modes, this node is boosted with respect to the input voltage (V_{IN}), so there should be sufficient negative gate drive.

In other operating modes such as buck, where the output voltage is less than the input voltage, it may be necessary to use low threshold p-channel MOSFETs to ensure adequate overdrive during cold-crank situations.

OUTPUT CAPACITOR

There are several points to consider when selecting the output capacitor.

Due to the switching topology used, the ripple current for this circuit is high since the output capacitor provides the LED current when the DC-DC converter switch is active in both boost and buck-boost modes. The capacitor is then recharged each time the inductor passes energy to the output. The ripple current on the output capacitor will be equal to the peak inductor current. The corresponding output ripple can be derived from the amount of charge transferred to the output during the switch on time.

To minimize heating effects and voltage ripple, the equivalent series resistance (ESR) and the equivalent series inductance (ESL) should be kept as low as possible. This can be achieved by multilayer ceramic chip (MLCC) capacitors. To reduce performance variation over temperature, low drift types such as X7R and X5R should be used.

The value of the output capacitor will typically be in the range of 3.3 to 10 µF, and it should be rated above the maximum LED stack voltage, V_{LED}. There is an E-field effect with ceramic capacitors that causes the capacitance to fall at elevated voltages. It is therefore recommended that a good margin is selected to minimize this effect.

One potential issue of ceramic capacitors is audible noise during pulse-width modulation (PWM). This is caused by the piezoelectric effect of the ceramic substrate. To minimize the effects of this, it is recommended to use multiple physically smaller capacitors. If this is still an issue, it is recommended that either low-impedance electrolytic or polymer capacitors be used.

INPUT CAPACITOR

The function of the input filter capacitor is to provide a low-impedance shunt path for the current drawn by the A6271-1 when the switching MOSFET turns on. The objective is to minimize the ripple current reflected back into the source supply. This approach helps to minimize conducted emissions into the power source. Additional line impedance in the form of chokes can be added to improve the emissions further.

In a correctly designed system, with a quality capacitor or capacitors positioned adjacent to the power train circuitry, these capacitors should supply the ripple current.

The amount of capacitance required at the input is dictated by the EMI performance. This is usually distributed with series ferrite beads and either differential-mode chokes, or common-mode chokes, or both.

Layout

The following layout guidelines should be followed to ensure satisfactory electrical and EMI performance.

Ground planes should be used on as many layers as possible. This is essential in minimizing ‘ground bounce’ (differential voltage across the ground connection). ‘Ground bounce’ can lead to radiated noise which can then be picked up on both input and output connections and manifest as common-mode noise. Any ground planes on different layers should be connected using multiple vias in an attempt to minimize ground impedances. The ground tab under the A6271-1 should also have multiple vias connecting to the ground plane or planes.

The drain connection of the switching MOSFET, PWM MOSFET, and cathode terminal of the recirculation diode are used for thermal heatsinking. It is advised to use sufficient copper around these connections on the component layer of the PCB only. The areas directly under these connections on the PCB should form part of the ground plane. The reason for restricting the copper area on these nodes is because they can radiate noise due to the nature of the dv/dt and di/dt power signals that appear.

The area of the switching power loops should be minimized as much as possible. In addition, the trace connections should be as wide as possible to minimize parasitic leakage inductances, but at the same time not compromising the power loop area. There are two power loops:

Loop 1: formed by the input filter, main switching MOSFET, power inductor, and inner loop sense resistor.

Loop 2: formed by the power inductor, recirculation diode, LED sense resistor, PWM MOSFET, and the output capacitor or capacitors.

Where practical, keep input or output filter magnetics as far away from the power-switching inductor (L1) as possible. This is to avoid or at least minimize the effects of magnetic crosstalk.

One of the major noise contributors is the switching MOSFET (M1). Slowing down the gate drive without compromising the thermal solution will help to minimize noise.

To comply with CISPR 25, a common-mode choke is typically required as part of the input filter.

Reducing EMI

It is essential that good layout practice as defined in the Layout Section should be adopted. The following techniques are also recommended.

SNUBBER

Adding a low-loss R-C snubber network between the drain of the main switching MOSFET and ground helps to suppress the resonant ringing on the switching node. The process for selecting these components involves some 'trial and error' on the actual printed circuit board.

Step 1: Measure the voltage resonance frequency on the LX node.

Step 2: Add an additional capacitance between LX and ground until the resonant frequency is halved. Note that this capacitance should be around 1 nF.

Step 3: Two equations with two unknowns are now obtained:

$$F_{RES} = \frac{1}{2 \times \pi \times \sqrt{L_{leak} \times C_{leak}}}$$

$$\frac{F_{RES}}{2} = \frac{1}{2 \times \pi \times \sqrt{L_{leak} \times C_{new}}}$$

where $C_{new} = C_{leak} + C_{add}$.

C_{add} = additional capacitance added.

C_{leak} = parasitic capacitance.

L_{leak} = parasitic inductance.

Now to halve the frequency, $C_{leak} + C_{add} = 4 \, x \, C_{leak}$

Therefore, $$C_{leak} = \frac{C_{add}}{3}$$

With C_{leak} solved, L_{leak} can also be solved.

The characteristic impedance of the parasitic components can be found:

$$R_O = \sqrt{\frac{L_{leak}}{C_{leak}}}$$

R_O can be selected as the damping resistor. Typically, either an 0805 or 0603 resistor case size is adequate.

INPUT FILTER

The selection of the components that form the input filter depends on the noise that is present in the system in terms of the frequency and whether it is common mode or differential mode. In addition, the common automotive standards that exist define onerous specification limit lines for the emissions in the AM band (approximately 530 kHz to 1.7 MHz) and the FM band (approximately 70 to 108 MHz). Some consideration must be given to these frequency bands to understand how to filter these regions.

At the lower frequencies, below a few 10s of MHz, the noise is generally dominated by differential noise with some common mode noise. At frequencies above a few 10s of MHz, the noise is dominated by common mode noise with some differential noise.

To address the differential noise, a differntial inductor can be used along with differential capacitance to form an L-C filter. One problem in using standard differential inductors is that the self-resonance frequency (SRF) is typically in the region of a few 10s of MHz, even with a modest few microhenries (µH) (note: the higher the inductance, the lower the SRF). This means that above the self-resonant frequency points, these components actually amplify the noise and make matters worse.

Some differential-mode inductive filtering is always necessary. Ferrite beads can be used for this function. Although ferrite beads are designed to act as a lossy resistor at particular frequency bands, they do have an inherent inductive element which can be in the region of several µH. The inductance of a ferrite bead can be extracted from the reactance information graph (refer to Figure 7). At a particular frequency, the reactance can be found and then the inductance can be derived.

As a single ferrite bead may not be effective enough, a two-stage ferrite bead filter approach can be taken. These components, along with input differential-mode capacitors, can form L-C filter stages. For the best result, the first L-C filter should be placed as close to the power stage as possible.

At higher frequencies, the majority of the noise problems is associated with common-mode noise. This noise is induced by

ground-referenced differential noise radiating through the ground plane. This noise can be picked up on the input stage forming common-mode noise on the positive and negative power supply connections to the battery. Even with excellent layout, this noise is always present.

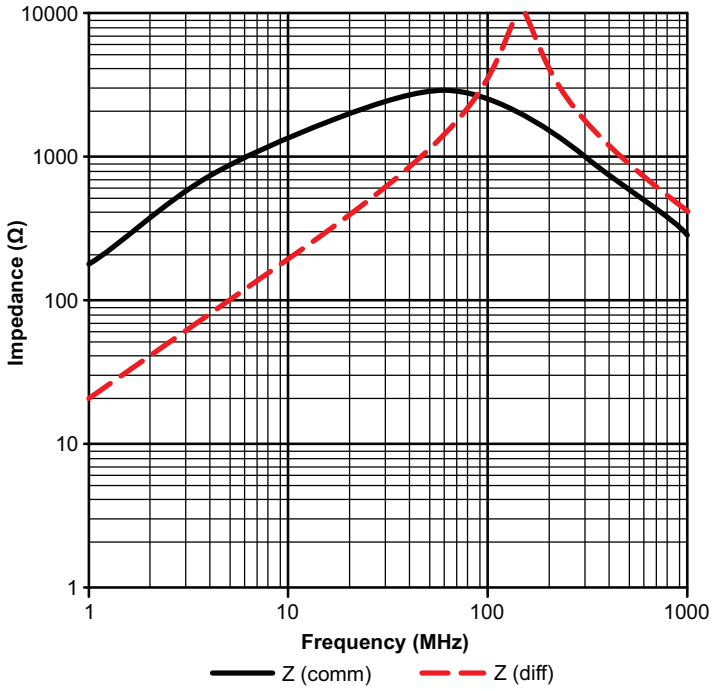


Figure 9: Common-Mode (CM) Choke Impedance

To address this problem, a common-mode inductor is required. This inductor is selected to present a high impedance around the FM region. An example of a common-mode (CM) choke with a high impedance around the FM region is shown below in Figure 9.

Another important consideration is the relative positioning of the common-mode choke with respect to the switching inductor. Magnetic crosstalk can occur between these components which can degrade the effectiveness of the CM choke. Even the use of a magnetically-screened switching inductor is not sufficient to avoid this problem. It is important to physically separate these two components as far as possible. Another advantage of a good physical separation is that any 'ground bounce' induced CM noise will couple onto the input power traces. The strength of the coupling will reduce with distance. The further the CM choke is away from the switching circuit, the more likely it will be to filter this noise.

All filter capacitors should be a quality ceramic: X7R or X8R.

FREQUENCY DITHERING

Further improvements to the differential-mode performance can be made by the use of frequency dithering techniques.

The A6271-1 contains a dither circuit which changes the switching oscillator frequency on a cycle-by-cycle basis across a defined frequency band.

As the noise in a switcher is typically narrow-band noise, both the peak and average signals are similar in amplitude. When a frequency dither scheme is introduced, it 'spreads' the noise, converting it from narrow band into broad band. While the peak noise reduces across the majority of the spectrum, the reduction in the average measurement is a lot more effective. This effect is particularly helpful in the conducted emissions for the average measurement between 76 and 108 MHz. This region is unusual, as typically the peak and average limit lines track one another, but in this area, while the peak limit line increases, the average limit line reduces (refer to Figure 10 below). Note the red limit lines are peak and the pink limit lines are average.

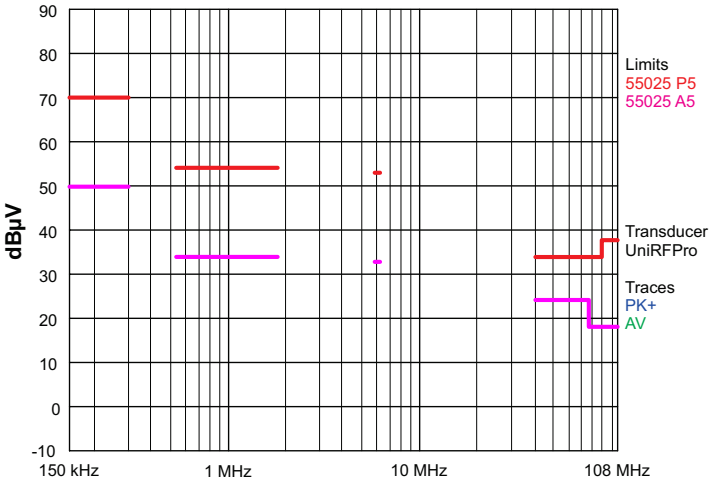


Figure 10: CISPR 25 Class 5 Limit Lines

The reason that the average limit line is relatively low (making it challenging to pass) is that average weighted signals have an adverse effect on FM radio signals.

Minimizing the noise at the high end of the conducted emission frequency spectrum also benefits the radiated noise at this frequency band and above.

Note that a modulation frequency of 10 kHz was chosen, since this aligns with the resolution bandwidth of the measurement receiver as defined in CISPR 25. The resolution bandwidth is effectively the ‘measurement window’ at each measurement step.

Another consideration when optimizing the frequency dithering is the depth of frequency. This is the maximum and minimum switching frequency that the converter operates, effectively the ‘spread range’. The wider the spread range is, the more effective the dithering is. However, there is a trade-off with switching losses and sizing of the power inductor in terms of inductance value and the corresponding physical size.

APPLICATION CIRCUITS

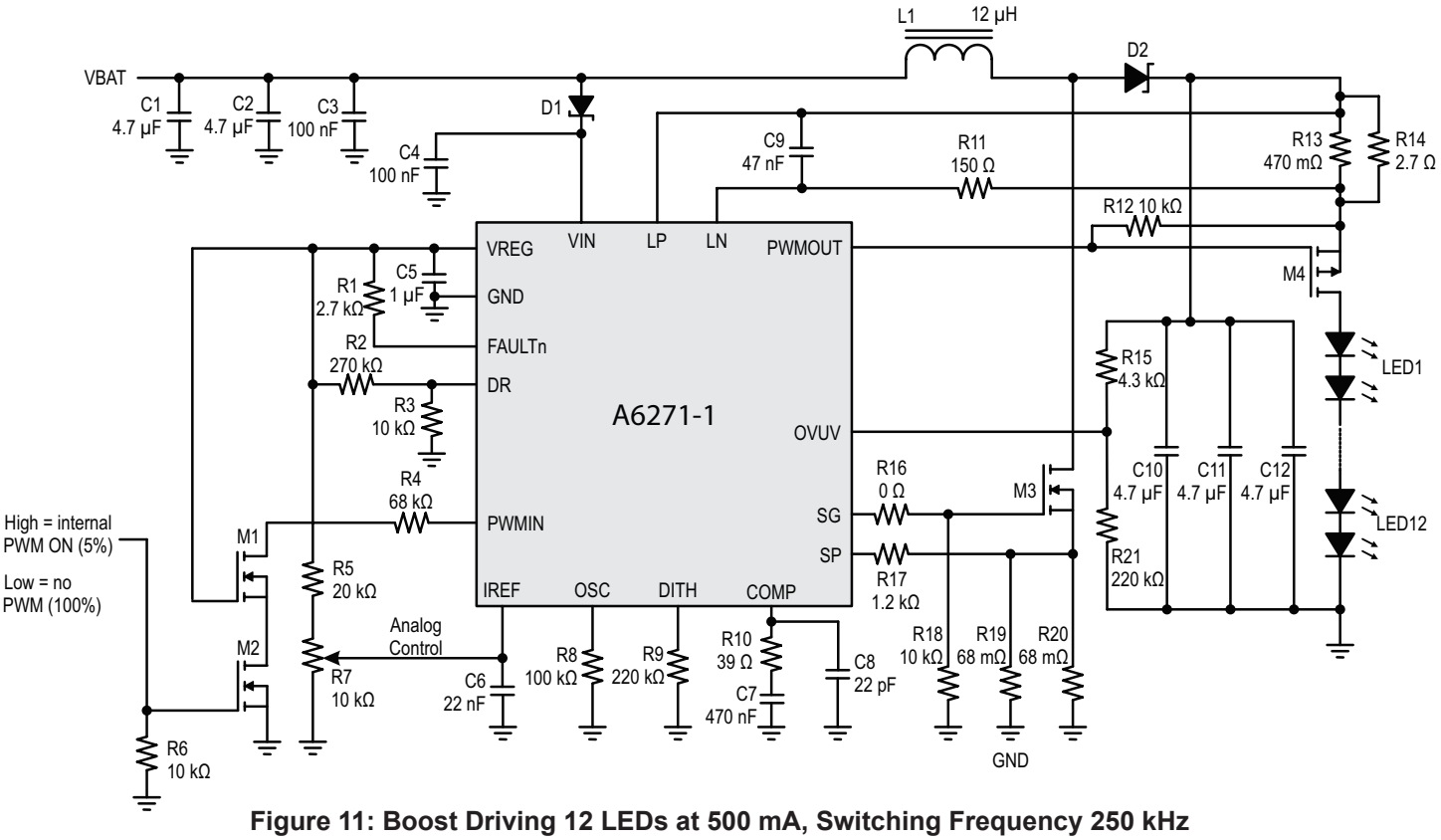


Figure 11: Boost Driving 12 LEDs at 500 mA, Switching Frequency 250 kHz

Internal PWM (5%) and/or analog dimming, no soft-start, and frequency dither on.

Table 2: Application Circuit 1 Bill of Materials

Reference	Description	Manufacturer/Part Number
C1,C2,C10,C11,C12	4.7 µF, ceramic capacitor, X7R, 50 V	TDK, MuRata
C3,C4	100 nF, ceramic capacitor, X7R, 50 V	
C5	1 µF, ceramic capacitor, X7R, 16 V	
C6	22 nF, ceramic capacitor, X7R, 50 V	
C7	470 nF, ceramic capacitor, X7R, 50 V	
C8	22 pF, ceramic capacitor, X7R, 50 V	
C9	47 nF, ceramic capacitor, X7R, 16 V	
D1	200 mA, 40 V Schottky diode	ST / BAT54
D2	10 A, 60 V Schottky diode	Vishay / SS10P6
L1	22 µH, high current shielded construction	Vishay / IHLP-5050FDER220M-5A
M1,M2	N-channel signal MOSFET	2N7000 or equivalent
M3	N-channel 50 A, 100 V MOSFET	Vishay / SQD50N10

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Table 2: Application Circuit 1 Bill of Materials (continued)

Reference	Description	Manufacturer/Part Number
M4	P-channel 15 A, 100 V MOSFET	Infineon / SPD15P10PL G
	Heatsink for M3 (TO-252)	AAVID Thermalloy / 573100D00010G
R1	2.7 kΩ, 1%, 0603 or 0805	
R2	270 kΩ, 1%, 0603 or 0805	
R3,R6,R12,R18	10 kΩ, 1%, 0603 or 0805	
R4	68 kΩ, 1%, 0603 or 0805	
R5	20 kΩ, 1%, 0603 or 0805	
R7	10 kΩ, potentiometer	
R8	100 kΩ, 1%, 0603 or 0805	
R9	220 kΩ, 1%, 0603 or 0805	
R10	39 Ω, 1%, 0603 or 0805	
R11	150 Ω, 1%, 0603 or 0805	
R13	470 mΩ, 1%, 0805 or 1206	
R14	2.7 Ω, 1%, 0603 or 0805	
R15	4.3 kΩ, 1%, 0603 or 0805	
R16	0 Ω, 0603 or 0805	
R17	1.2 kΩ, 1%, 0603 or 0805	
R19,R20	68 mΩ, 1%, 2010	
R21	220 kΩ, 1%, 0603 or 0805	

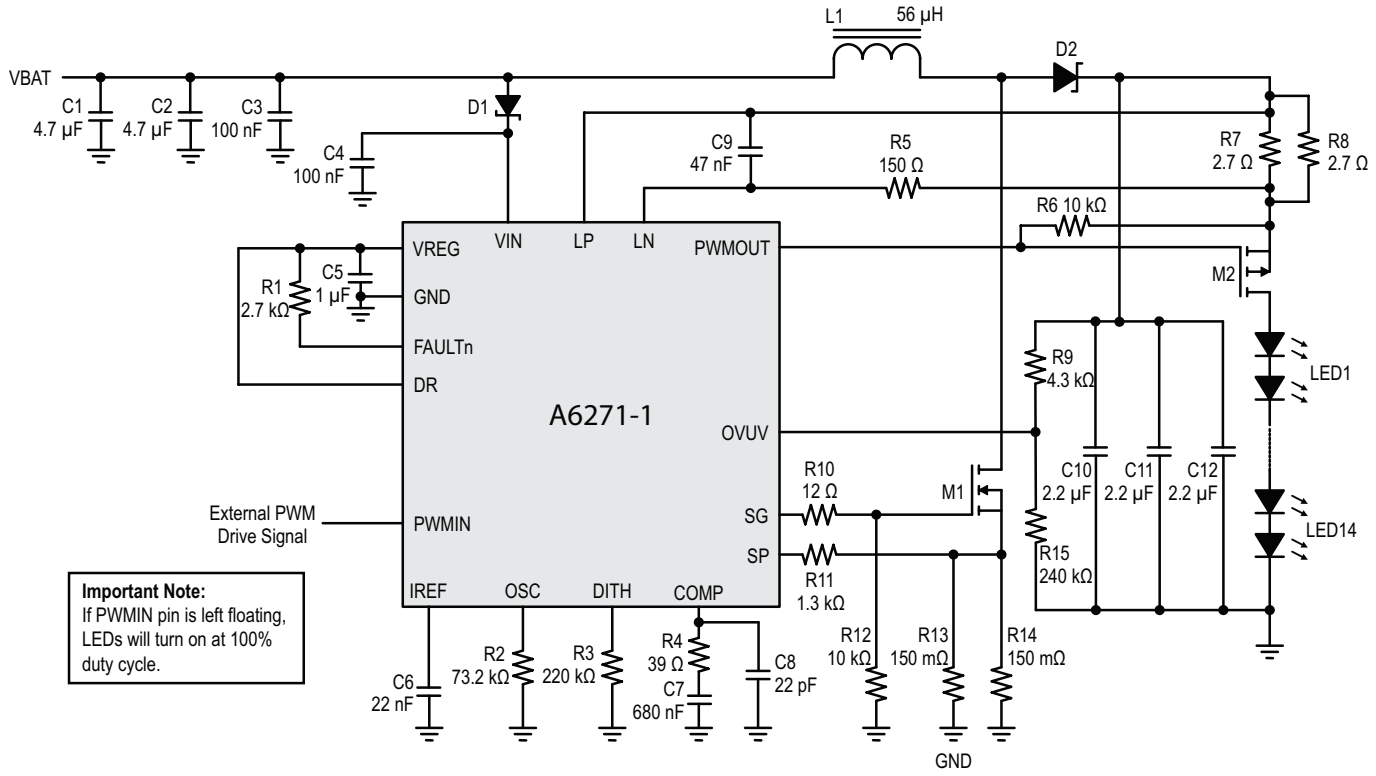


Figure 12: Boost Driving 14 LEDs at 150 mA, Switching Frequency 350 kHz

External PWM, no analog dimming, soft-start, and frequency dither on.

Table 3: Application Circuit 2 Bill of Materials

Reference	Description	Manufacturer/Part Number
C1,C2	4.7 µF, ceramic capacitor, X7R, 50 V	TDK, MuRata
C3,C4	100 nF, ceramic capacitor, X7R, 50 V	
C5	1 µF, ceramic capacitor, X7R, 16 V	
C6	22 nF, ceramic capacitor, X7R, 50 V	
C7	680 nF, ceramic capacitor, X7R, 50 V	
C8	22 pF, ceramic capacitor, X7R, 50 V	
C9	47 nF, ceramic capacitor, X7R, 16 V	
C10,C11,C12	2.2 µF, ceramic capacitor, X7R, 100 V	TDK, MuRata
D1	200 mA, 40 V Schottky diode	ST / BAT54
D2	2 A, 100 V Schottky diode	Vishay, ST / SS2H10
L1	56 µH, power inductor shielded construction	Coilcraft / MSS1048T-563ML
M1	N-channel, 30 A, 100 V MOSFET	NXP / PSMN038-100YLX

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Table 3: Application Circuit 2 Bill of Materials (continued)

Reference	Description	Manufacturer/Part Number
M2	P-channel 15 A, 100 V MOSFET	Infineon / SPD15P10PL G
R1	2.7 kΩ, 1%, 0603 or 0805	
R2	73.2 kΩ, 1%, 0603 or 0805	
R3	220 kΩ, 1%, 0603 or 0805	
R4	39 Ω, 1%, 0603 or 0805	
R5	150 Ω, 1%, 0603 or 0805	
R6,R12	10 kΩ, 1%, 0603 or 0805	
R7,R8	2.7 Ω, 1%, 0805 or 1206	
R9	4.3 kΩ, 1%, 0603 or 0805	
R10	12 Ω, 1%, 0603 or 0805	
R11	1.3 kΩ, 1%, 0603 or 0805	
R13,R14	150 mΩ, 1%, 1206	
R15	240 kΩ, 1%, 0603 or 0805	

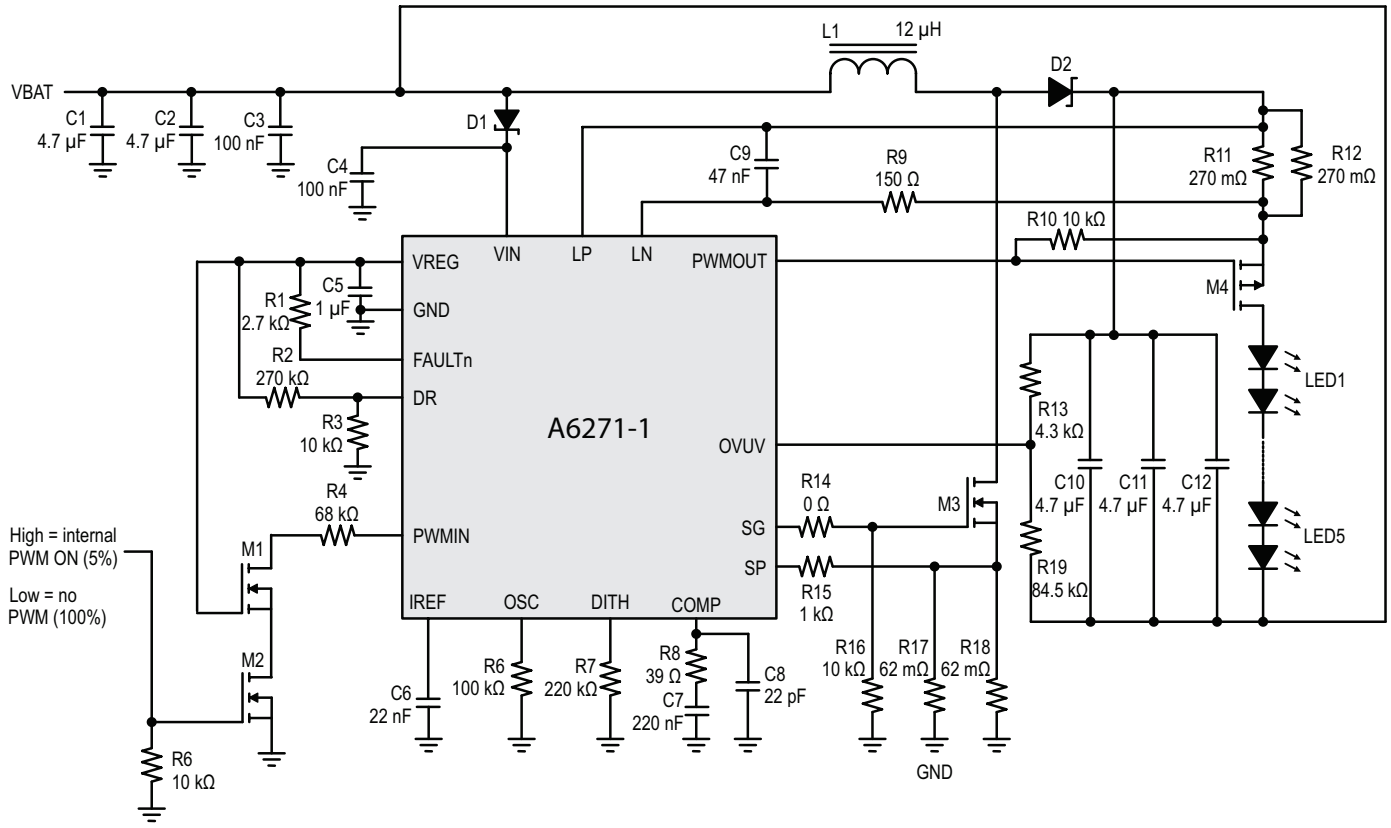


Figure 13: Buck-Boost Driving 5 LEDs at 1.5 A, Switching Frequency 250 kHz

Internal PWM (5%), no analog dimming, soft-start, and frequency dither on.

Table 4: Application Circuit 3 Bill of Materials

Reference	Description	Manufacturer/Part Number
C1,C2,C10,C11,C12	4.7 µF, ceramic capacitor, X7R, 50 V	TDK, MuRata
C3,C4	100 nF, ceramic capacitor, X7R, 50 V	
C5	1 µF, ceramic capacitor, X7R, 16 V	
C6	22 nF, ceramic capacitor, X7R, 50 V	
C7	220 nF, ceramic capacitor, X7R, 50 V	
C8	22 pF, ceramic capacitor, X7R, 50 V	
C9	47 nF, ceramic capacitor, X7R, 16 V	
D1	200 mA, 40 V Schottky diode	ST / BAT54
D2	10 A, 60 V Schottky diode	Vishay / SS10P6
L1	12 µH, high current shielded construction	Vishay / IHLP-5050FDER120M-5A
M1,M2	N-channel signal MOSFET	2N7000 or equivalent
M3	N-channel 50 A, 100 V MOSFET	Vishay / SQD50N10

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Table 4: Application Circuit 3 Bill of Materials (continued)

Reference	Description	Manufacturer/Part Number
M4	P-channel 15 A, 100 V MOSFET	Infineon / SPD15P10PL G
	Heatsink for M3 (TO-252)	AAVID Thermalloy / 573100D00010G
R1	2.7 kΩ, 1%, 0603 or 0805	
R2	270 kΩ, 1%, 0603 or 0805	
R3,R5,R10,R16	10 kΩ, 1%, 0603 or 0805	
R4	68 kΩ, 1%, 0603 or 0805	
R6	100 kΩ, 1%, 0603 or 0805	
R7	220 kΩ, 1%, 0603 or 0805	
R8	39 Ω, 1%, 0603 or 0805	
R9	150 Ω, 1%, 0603 or 0805	
R11, R12	270 mΩ, 1%, 0805 or 1206	
R13	4.3 kΩ, 1%, 0603 or 0805	
R14	0 Ω, 0603 or 0805	
R15	1 kΩ, 1%, 0603 or 0805	
R17,R18	62 mΩ, 1%, 2010	
R19	84.5 kΩ, 1%, 0603 or 0805	

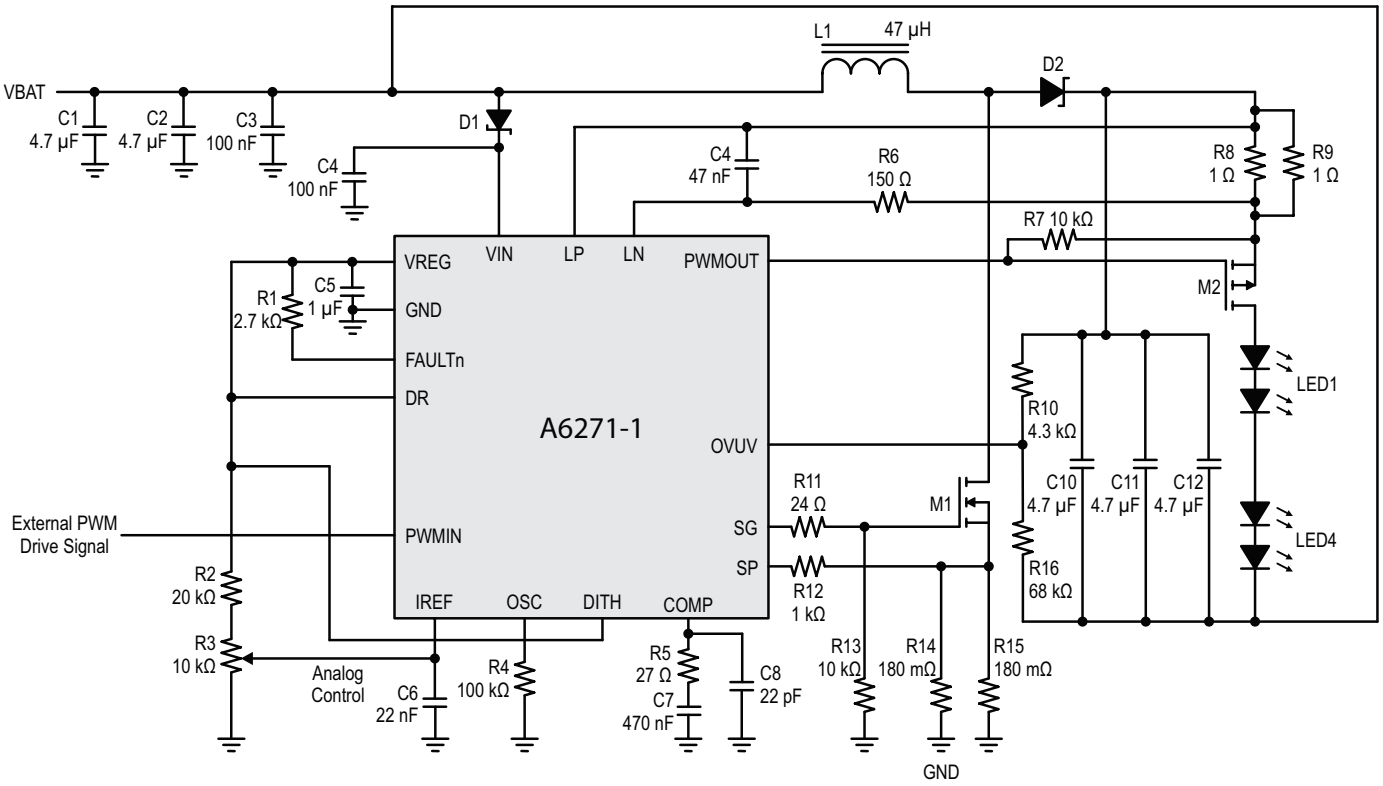


Figure 14: Buck-Boost Driving 4 LEDs at 400 mA, Switching Frequency 250 kHz

External PWM and/or analog dimming, no soft-start, and frequency dither off.

Table 5: Application Circuit 4 Bill of Materials

Reference	Description	Manufacturer/Part Number
C1,C2,C10,C11,C12	4.7 µF, ceramic capacitor, X7R, 50 V	TDK, MuRata
C3,C4	100 nF, ceramic capacitor, X7R, 50 V	
C5	1 µF, ceramic capacitor, X7R, 16 V	
C6	22 nF, ceramic capacitor, X7R, 50 V	
C7	470 nF, ceramic capacitor, X7R, 50 V	
C8	22 pF, ceramic capacitor, X7R, 50 V	
C9	47 nF, ceramic capacitor, X7R, 16 V	
D1	200 mA, 40 V Schottky diode	ST / BAT54
D2	2 A, 60 V Schottky diode	ON Semiconductor / MBRS260T3
L1	47 µH, power inductor shielded construction	Coilcraft / MSS1048T-473ML
M1	N-channel, 30 A, 100 V MOSFET	NXP / PSMN038-100YLX
M2	P-channel 15 A, 100 V MOSFET	Infineon / SPD15P10PL G

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Table 5: Application Circuit 4 Bill of Materials (continued)

Reference	Description	Manufacturer/Part Number
R1	2.7 kΩ, 1%, 0603 or 0805	
R2	20 kΩ, 1%, 0603 or 0805	
R3	10 kΩ, potentiometer	
R4	100 kΩ, 1%, 0603 or 0805	
R5	27 Ω, 1%, 0603 or 0805	
R6	150 Ω, 1%, 0603 or 0805	
R7, R13	10 kΩ, 1%, 0603 or 0805	
R8, R9	1 Ω, 1%, 0805 or 1206	
R10	4.3 kΩ, 1%, 0603 or 0805	
R11	24 Ω, 1%, 0603 or 0805	
R12	1 kΩ, 1%, 0603 or 0805	
R14, R15	180 mΩ, 1%, 1206	
R16	68 kΩ, 1%, 0603 or 0805	

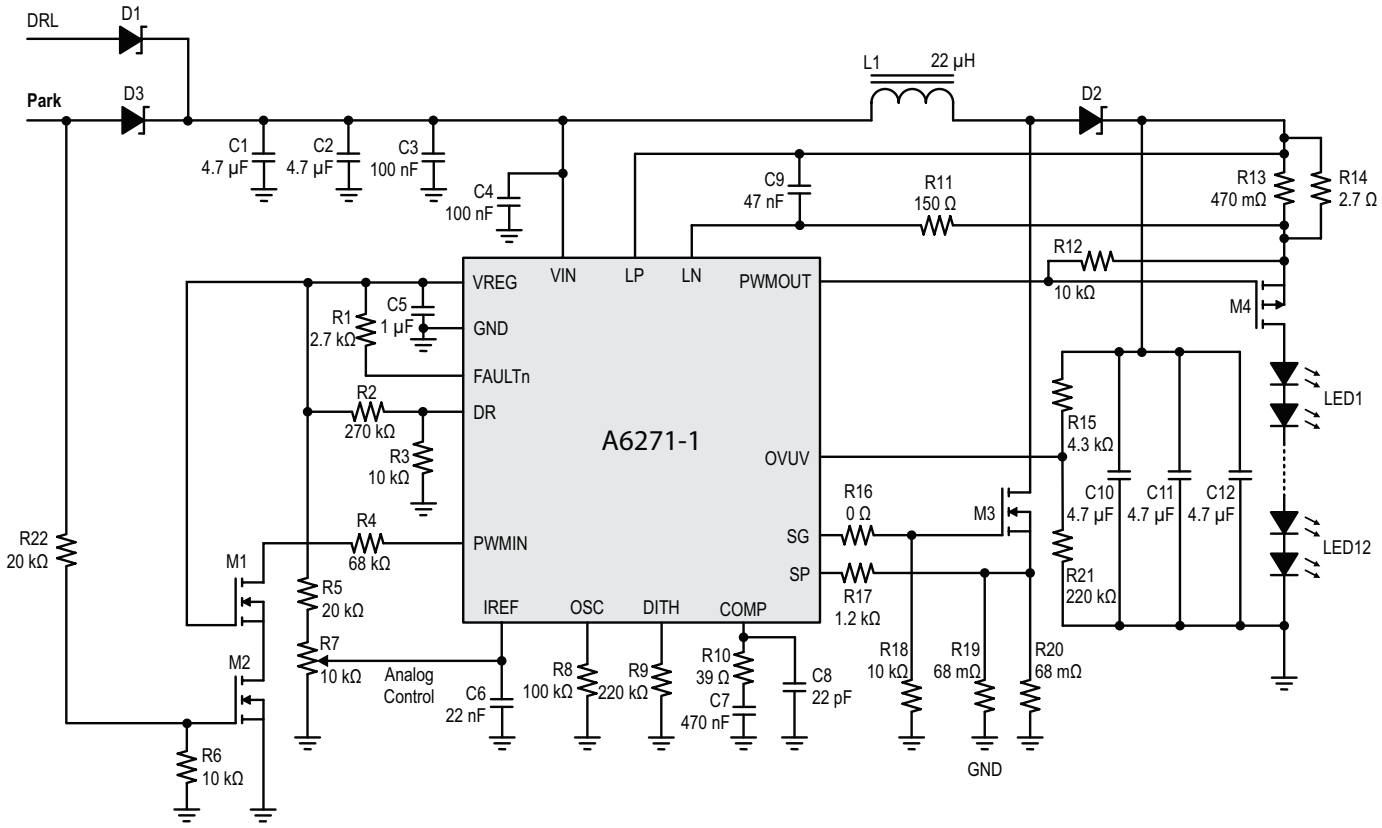


Figure 15: Park / DRL Application (Park-Dominant)

Boost Driving 12 LEDs at 500 mA, Switching Frequency 250 kHz.
Park Mode: Internal PWM (5%) and analog dimming, no soft start, and frequency dither on.
Daylight Running Light (DRL) Mode: 100% LED current and analog dimming, no soft start, and frequency dither on.
Battery voltage applied either at Park terminal or DRL terminal. Note that Park Mode is dominant.

Table 6: Application Circuit 5 Bill of Materials

Reference	Description	Manufacturer/Part Number
C1,C2,C10,C11,C12	4.7 µF, ceramic capacitor, X7R, 50 V	TDK, MuRata
C3,C4	100 nF, ceramic capacitor, X7R, 50 V	
C5	1 µF, ceramic capacitor, X7R, 16 V	
C6	22 nF, ceramic capacitor, X7R, 50 V	
C7	470 nF, ceramic capacitor, X7R, 50 V	
C8	22 pF, ceramic capacitor, X7R, 50 V	
C9	47 nF, ceramic capacitor, X7R, 16 V	
D1, D3	3 A, 100 V Schottky diode	ON Semiconductor / NRVBS3100T3G
D2	10 A, 60 V Schottky diode	Vishay / SS10P6
L1	22 µH, high current shielded construction	Vishay / IHLP-5050FDER220M-5A
M1, M2	N-channel signal MOSFET	2N7000 or equivalent

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Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 6: Application Circuit 5 Bill of Materials (continued)

Reference	Description	Manufacturer/Part Number
M3	N-channel, 50 A, 100 V MOSFET	Vishay / SQD50N10
M4	P-channel, 15 A, 100 V MOSFET	Infineon / SPD15P10PL G
	Heatsink for M3 (TO-252)	AAVID Thermalloy / 573100D00010G
R1	2.7 kΩ, 1%, 0603 or 0805	
R2	270 kΩ, 1%, 0603 or 0805	
R3,R6,R12,R18	10 kΩ, 1%, 0603 or 0805	
R4	68 kΩ, 1%, 0603 or 0805	
R5, R22	20 kΩ, 1%, 0603 or 0805	
R7	10 kΩ, potentiometer	
R8	100 kΩ, 1%, 0603 or 0805	
R9	220 kΩ, 1%, 0805 or 1206	
R10	39 Ω, 1%, 0603 or 0805	
R11	150 Ω, 1%, 0603 or 0805	
R13	470 mΩ, 1%, 0805 or 1206	
R14	2.7 Ω, 1%, 0603 or 0805	
R15	4.3 kΩ, 1%, 0603 or 0805	
R16	0 Ω, 0603 or 0805	
R17	1.2 Ω, 1%, 0603 or 0805	
R19, R20	68 mΩ, 1%, 2010	
R21	220 kΩ, 1%, 0603 or 0805	

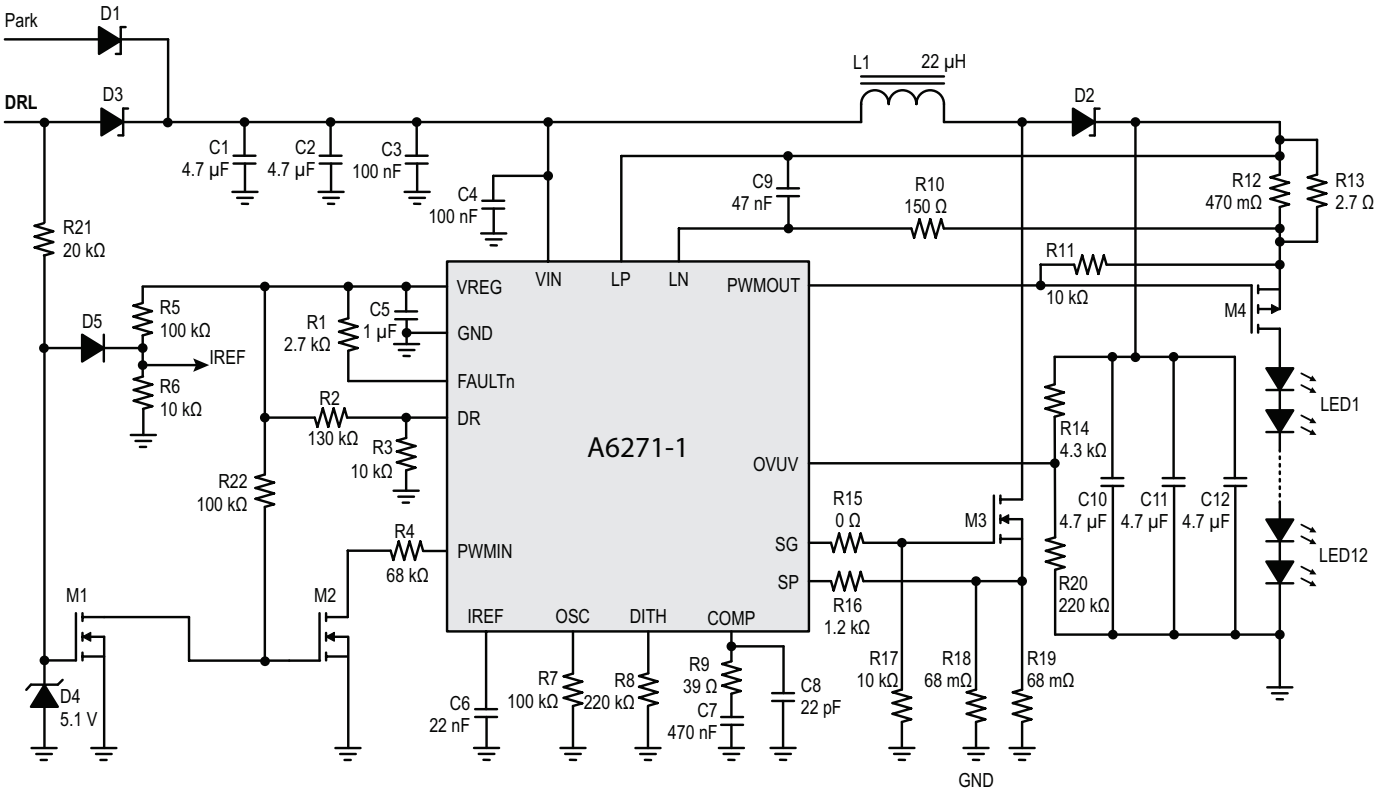


Figure 16: Park / DRL Application (DRL-Dominant)

Boost Driving 12 LEDs at 500 mA, Switching Frequency 250 kHz.
Park Mode: Internal PWM (10%) and analog dimming at 45% of target level, no soft start, and frequency dither on.
Daylight Running Light (DRL) Mode: 100% LED current, no analog dimming, no soft start, and frequency dither on.
Battery voltage applied either at Park terminal or DRL terminal. Note that DRL Mode is dominant.

Table 7: Application Circuit 6 Bill of Materials

Reference	Description	Manufacturer/Part Number
C1,C2,C10,C11,C12	4.7 µF, ceramic capacitor, X7R, 50 V	TDK, MuRata
C3,C4	100 nF, ceramic capacitor, X7R, 50 V	
C5	1 µF, ceramic capacitor, X7R, 16 V	
C6	22 nF, ceramic capacitor, X7R, 50 V	
C7	470 nF, ceramic capacitor, X7R, 50 V	
C8	22 pF, ceramic capacitor, X7R, 50 V	
C9	47 nF, ceramic capacitor, X7R, 16 V	
D1, D3	3 A, 100 V Schottky diode	ON Semiconductor / NRVBS3100T3G
D2	10 A, 60 V Schottky diode	Vishay / SS10P6
D4	5.1 V, Zener diode	ON Semiconductor / SZBZX84C5V1
D5	Signal diode	1N4148WS
L1	22 µH, high current shielded construction	Vishay / IHLP-5050FDER220M-5A

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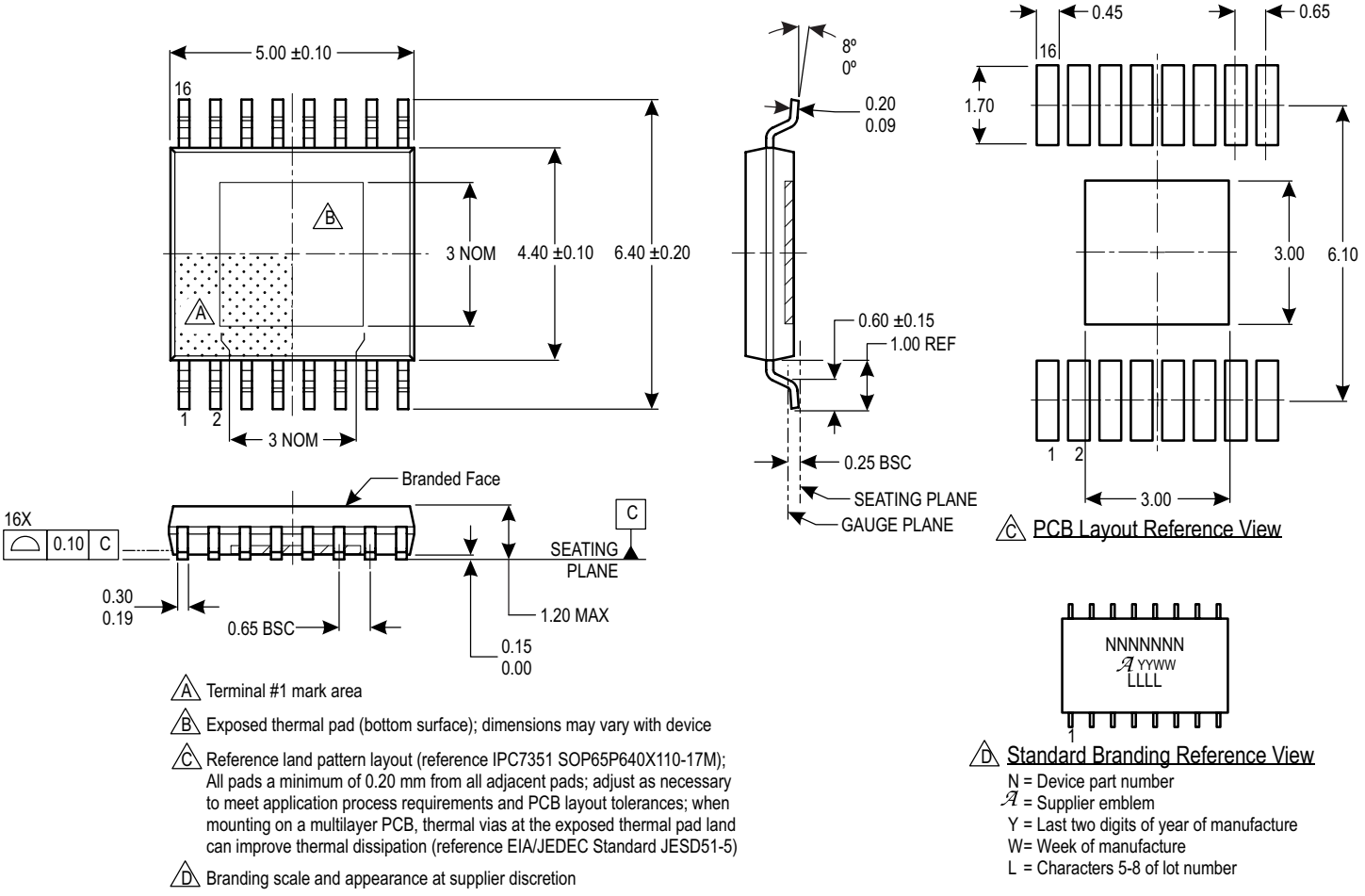
Table 7: Application Circuit 6 Bill of Materials (continued)

Reference	Description	Manufacturer/Part Number
M1, M2	N-channel signal MOSFET	ON Semiconductor, IR / NTR4003N
M3	N-channel, 50 A, 100 V MOSFET	Vishay / SQD50N10
M4	P-channel, 15 A, 100 V MOSFET	Infineon / SPD15P10PL G
	Heatsink for M3 (TO-252)	AAVID Thermalloy / 573100D00010G
R1	2.7 kΩ, 1%, 0603 or 0805	
R2	130 kΩ, 1%, 0603 or 0805	
R3,R6,R11,R17	10 kΩ, 1%, 0603 or 0805	
R4	68 kΩ, 1%, 0603 or 0805	
R5, R7, R22	100 kΩ, 1%, 0603 or 0805	
R8	220 kΩ, 1%, 0805 or 1206	
R9	39 Ω, 1%, 0603 or 0805	
R10	150 Ω, 1%, 0603 or 0805	
R12	470 mΩ, 1%, 0805 or 1206	
R13	2.7 Ω, 1%, 0603 or 0805	
R14	4.3 kΩ, 1%, 0603 or 0805	
R15	0 Ω, 0603 or 0805	
R16	1.2 kΩ, 1%, 0603 or 0805	
R18, R19	68 mΩ, 1%, 2010	
R20	220 kΩ, 1%, 0603 or 0805	
R21	110 kΩ, 1%, 0603 or 0805	

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MO-153 ABT)
Dimensions in millimeters. NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W= Week of manufacture
L = Characters 5-8 of lot number

Figure 17: Package LP, 16-Pin eTSSOP with Exposed Thermal Pad

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Revision Table

Number	Date	Description
–	May 5, 2017	Initial release
1	January 2, 2018	Updated Figures 1, 11, 12, 13, 15, 16, and A-2; added Table of Contents
2	January 24, 2018	Updated Ramp Up and Ramp Down Threshold test conditions (page 7), and Protection section (page 12-13)
3	July 9, 2018	Note added to Figure 12 (page 26).

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APPENDIX A: SPECIAL NOTES ON A6271-1 OPERATING IN SEPIC MODE

In automotive lighting applications, SEPIC (Single-Ended Primary-Inductor Converter) is an attractive alternative to the traditional Boost and Buck-Boost topologies. As can be seen in the following comparison diagram, the SEPIC configuration looks very similar to the Boost configuration, except for the additional inductor L2 and DC-blocking capacitor C_{FLY}.

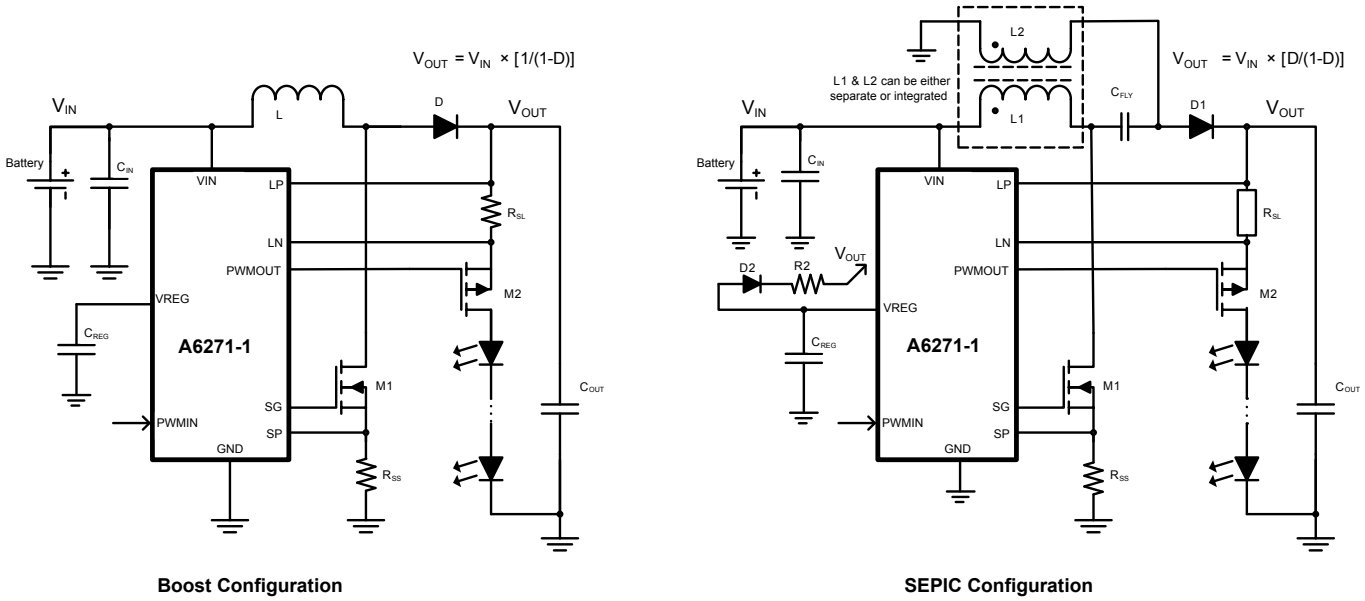


Figure A-1: Comparison of A6271-1 in Boost and SEPIC configurations

The main advantages of using SEPIC configuration are:

- V_{OUT} (V_{LED}) can be either higher or lower than V_{IN}. This allows the converter to handle both Cold-Crank (V_{IN} down to ~5 V) and Load-Dump (V_{IN} up to 40 V) situations.
- There is a DC-blocking capacitor between V_{IN} and V_{OUT}. This naturally protects the power supply against Output-Shorted-to-GND fault.

On the other hand, several limitations of SEPIC must be considered, namely:

- Need to use either two inductors, or one dual-winding coupled inductor.
- The switching MOSFET and diode are subjected to higher voltage stress of $V_{IN} + V_{LED}$. This means higher switching loses compared to Boost configuration. Note that in Buck-Boost configuration the same voltage stress applies.
- At power up, a 'bleeder' circuit is needed to help the IC bypass undervoltage protection (since initially the output is at 0 V).
- A minimum output voltage of around 6 V (two WLEDs in series) is required, for the PWMOUT gate driver to turn on the external PMOS.

The next application diagram shows the A6271-1 configured in SEPIC mode, for driving 5 LEDs at 1.5 A.

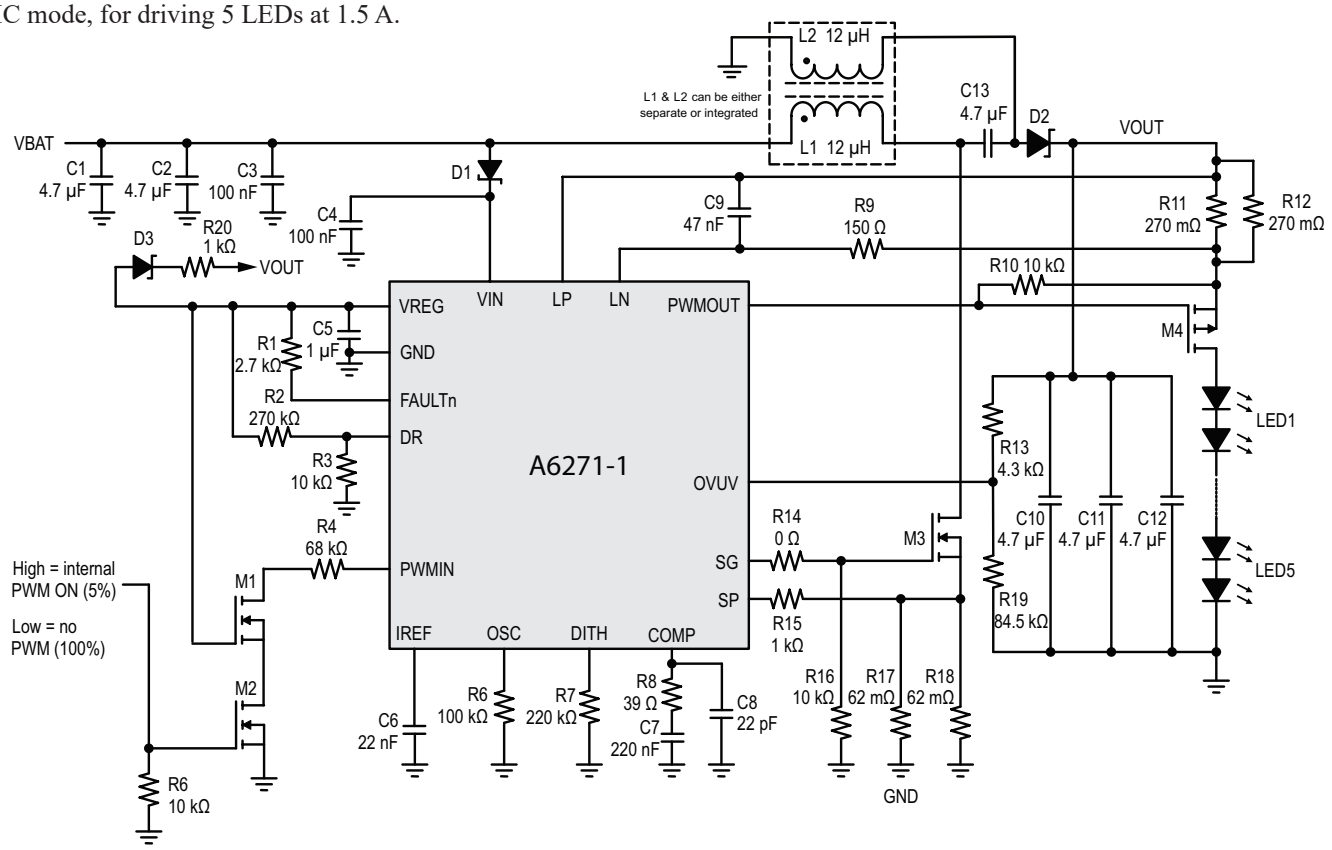


Figure A-2: SEPIC Driving 5 LEDs at 1.5 A, Switching Frequency 250 kHz

Internal PWM (5%), no analog dimming, soft-start, and frequency dither on.

Table 8: Application Circuit 7 Bill of Materials

Reference	Description	Manufacturer/Part Number
C1,C2,C10,C11,C12,C13	4.7 µF, ceramic capacitor, X7R, 50 V	TDK, MuRata
C3,C4	100 nF, ceramic capacitor, X7R, 50 V	
C5	1 µF, ceramic capacitor, X7R, 16 V	
C6	22 nF, ceramic capacitor, X7R, 50 V	
C7	220 nF, ceramic capacitor, X7R, 50 V	
C8	22 pF, ceramic capacitor, X7R, 50 V	
C9	47 nF, ceramic capacitor, X7R, 16 V	
D1, D3	200 mA, 40 V Schottky diode	ST / BAT54
D2	10 A, 60 V Schottky diode	Vishay / SS10P6
L1, L2	12 µH, high-current shielded construction	Vishay / IHLP-5050FDER120M-5A
M1,M2	N-channel signal MOSFET	2N7000 or equivalent
M3	N-channel 50 A, 100 V MOSFET	Vishay / SQD50N10

Continued on next page...

Table 8: Application Circuit 7 Bill of Materials (continued)

Reference	Description	Manufacturer/Part Number
M4	P-channel 15 A, 100 V MOSFET	Infineon / SPD15P10PL G
	Heatsink for M3 (TO-252)	AAVID Thermalloy / 573100D00010G
R1	2.7 kΩ, 1%, 0603 or 0805	
R2	270 kΩ, 1%, 0603 or 0805	
R3,R5,R10,R16	10 kΩ, 1%, 0603 or 0805	
R4	68 kΩ, 1%, 0603 or 0805	
R6	100 kΩ, 1%, 0603 or 0805	
R7	220 kΩ, 1%, 0603 or 0805	
R8	39 Ω, 1%, 0603 or 0805	
R9	150 Ω, 1%, 0603 or 0805	
R11,R12	270 mΩ, 1%, 0805 or 1206	
R13	4.3 kΩ, 1%, 0603 or 0805	
R14	0 Ω, 0603 or 0805	
R15	1 kΩ, 1%, 0603 or 0805	
R17,R18	62 mΩ, 1%, 2010	
R19	84.5 kΩ, 1%, 0603 or 0805	
R20	1 kΩ, 1%, 0603 or 0805	