data sheet



Package on Package (PoP) Family

PSvfBGA

Package Stackable Very Thin Fine Pitch BGA (PSvfBGA):

After 3 years of development in package stacking technology and infrastructure, Amkor launched the multiple award winning PSvfBGA (base PoP) platform during the 4th quarter of 2004. The next two years saw many new milestones, from publication of JEDEC mechanical and electrical standards to a range of new customers and applications adopting PoP. By the end of 2006 PSvfBGA became the fastest growing new product in Amkor's history, reflecting the broad industry benefits of PoP and Amkor's leadership position. The next few years promise to provide many new challenges and applications for PoP, as handheld multimedia applications continue to demand higher processing power and memory storage capacities. Amkor is committed to maintain strong development and production capabilities to ensure we are forefront in meeting next generation PoP requirements.

Amkor has expanded our comprehensive PoP family and aligned the roadmap across the supply chain to ensure that PoP will continue to scale with the industry's miniaturization, higher density and performance enhancement requirements.

In 2006 Amkor's PoP family ramped products with 2 die stacked in the PSvfBGA platform. Stacking multiple die in the bottom package allows customers to increase performance and provide further system miniaturization by combining analog + digital or logic + memory devices.

Applications:

PoP packages are designed for products requiring efficient memory architectures including multiple buses and increased memory density & performance, while reducing mounted area. Portable electronic products such as mobile phones (baseband or applications processor + combo memory), digital cameras (image processor + memory), PDAs, portable players (audio / graphics processor + memory), gaming and other mobile applications can benefit from the combination of stacked package and small footprint offered by Amkor's industry leading PoP family.

Broad Benefits as an Enabling Technology:

PoP offers OEMs and EMS providers a platform to cost effectively expand options for logic + memory 3D integration with the following benefits:

- Greatly expands device options by simplifying the business logistics of stacking
- Integration controlled at the system level to best match stacked combinations with system requirements
- JEDEC standards ensure broad component availability
- Improving time to market and sourcing flexibility
- Eliminates margin stacking and expands technology reuse
- Helps manage the huge cost impacts associated with increasing demand for multi-media processing and memory
- Logic device transitions to flip chip in the bottom package enables further PoP size and height reductions

Features:

- 10-15 mm body sizes tooled per product table. Additional sizes based on demand
- Top package I/O interface 0.65 mm pitch accommodating 104 to 160 pin counts
- High I/O 0.50 mm pitch interface is qualified
- Fine pitch 0.50 mm bottom package footprints with 0.40 mm pitch in qualification
- Established package on package infrastructure (over 5 years of development with leading OEM, EMS and equipment providers)
- Wafer thinning / handling $< 100\,\mu m$
- Consistent product performance and reliability
- Package configurations compliant with JEDEC standards
- Package pre-stacking support and services available based on demand
- Bottom PSvfBGA and top FBGA / Stacked CSP packages are well established in high volume production
- Stacked package heights of 1.2 mm to 1.6 mm available in a variety of configurations. (See Stack Up table below)

Reliability:

Amkor assures reliable performance by continuously monitoring key indices:

Package Level:

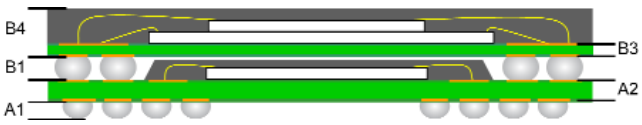
- Moisture Resistance Testing JEDEC Level 3 @260 °C x 4 reflows
- Additional Test Data at [(30 °C/85%RH/96hrs)+260]x3 or x4
- Package dimensions 14 x 14 mm, 352 I/O
- Temp Cycle -55/+125 °C, 1000 cycles
- Temp/Humidity 85 °C/85%RH/1000 hours
- High Temp Storage 150 °C, 1000 hours
- HAST 130 °C, 85% RH, 96 hours

Board Level:

- Thermal Cycle -40/+125 °C, 1000 cycles

PoP Overall Stack Up Table

		FBGA + PSvfBGA		
Symbol	Unit	Min	Max	Nom
A1 (mounted, 0.5 pitch)	mm	0.160	0.260	0.210
A2 (4L laminate)	mm	0.260	0.340	0.300
B1 (stacked, 0.65 pitch), single die	mm	0.270	0.330	0.300
B2 (stacked, 0.65 pitch), 2 + 0 die	mm	0.320	0.380	0.350
B3 (2L laminate)	mm	0.100	0.160	0.130
B4 (mold cap)	mm	0.370	0.430	0.400
Overall Pkg height	mm	1.310	1.470	1.400





VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

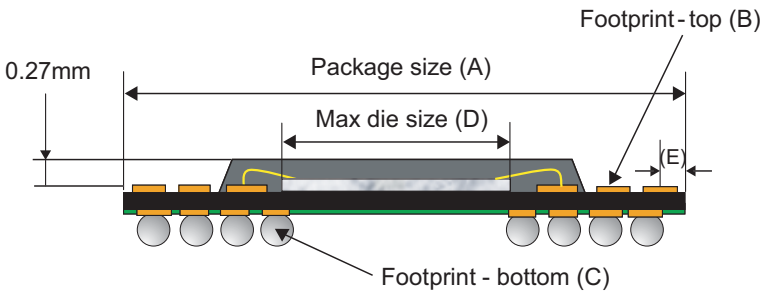
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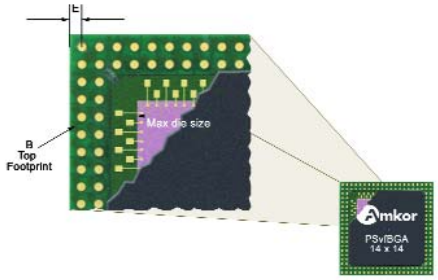
Package on Package (POP) Family

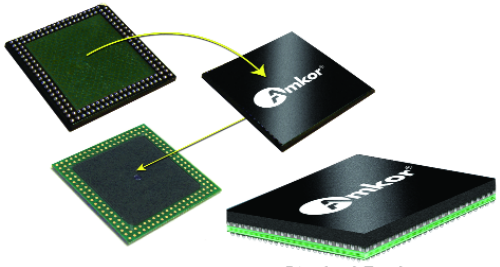
PSvfBGA

PSvfBGA Cross Section



PSvfBGA Top View





Stacked Package

Process Highlights

Die thickness (max)	75 μm ti 125 μm
Bond pad pitch (min)	40 μm (In-line)
Marking	Laser
Wafer thinning	200 & 300 mm wafers

Standard Materials

Package substrate	
-Conductor	Copper
-Dielectric	Thin core FR5 or equivalent
Die attach adhesive	Conductive or non conductive
Encapsulant	Epoxy mold compound
Solder ball	Eutectic SnPb / Pb free

Test Services

Program Generation / Conversion
Product Engineering
Wafer sort
256 Pin x 20 MHz test system available

Shipping

JEDEC trays
Tape and Reel services

Contact Amkor for Daisy chain sample availability, the latest PSvfBGA capabilities, and for full review of PSvfBGA, PoP technology and roadmaps.

A	B		C	D	E	
Body Size (mm)	Package Interconnect Matrix	Package Interconnect Ball Count	Bottom Package Ball Count	Die Size (mm)	Package Interconnect ball center to package edge (mm)	Typical Wirecount for given package size
10	15	104	300	<5.50	0.450	320
11	16	112	350	<6.00	0.625	360
12	18	128	400	<7.50	0.475	420
13	19	136	450	<8.00	0.650	460
14	21	152	550	<9.00	0.500	520
15	22	160	700	<10.00	0.675	600

- Dimensions are in line with JEDEC JC-11 standards for PoP packages in development
- Assuming 2 perimeter rows of interconnects at 0.65 mm pitch
- Assuming 4 perimeter rows of BGA balls to motherboard at 0.50 mm pitch

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