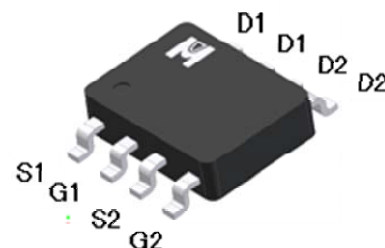
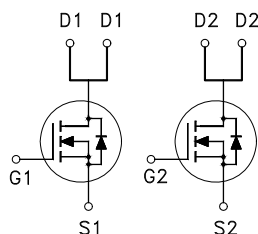


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH
BV_{DSS}	100V
$R_{DS(on)} (MAX.)$	150m Ω
I_D	3A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	3	A
	$T_A = 100\text{ }^{\circ}\text{C}$		2.1	
Pulsed Drain Current ¹		I_{DM}	12	
Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	2	W
	$T_A = 100\text{ }^{\circ}\text{C}$		0.8	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$			1	μA
		$V_{DS} = 70V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	3			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 2A$		125	150	m Ω
		$V_{GS} = 5V, I_D = 1.5A$		168	225	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 2A$		8		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 20V, f = 1MHz$		1030		pF
Output Capacitance	C_{oss}			50		
Reverse Transfer Capacitance	C_{rss}			42		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 80V, V_{GS} = 10V, I_D = 2A$		23		nC
Gate-Source Charge ^{1,2}	Q_{gs}			2.3		
Gate-Drain Charge ^{1,2}	Q_{gd}			6.1		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 50V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		12		nS
Rise Time ^{1,2}	t_r			20		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			25		
Fall Time ^{1,2}	t_f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _s				3	A
Pulsed Current ³	I _{SM}				12	
Forward Voltage ¹	V _{SD}	I _F = I _s , V _{GS} = 0V			1.3	V

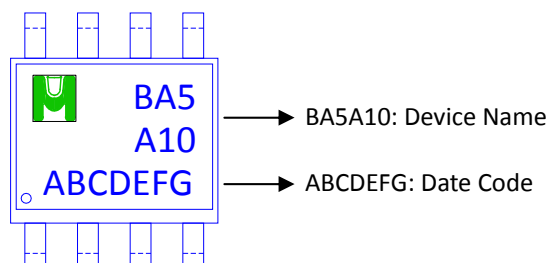
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

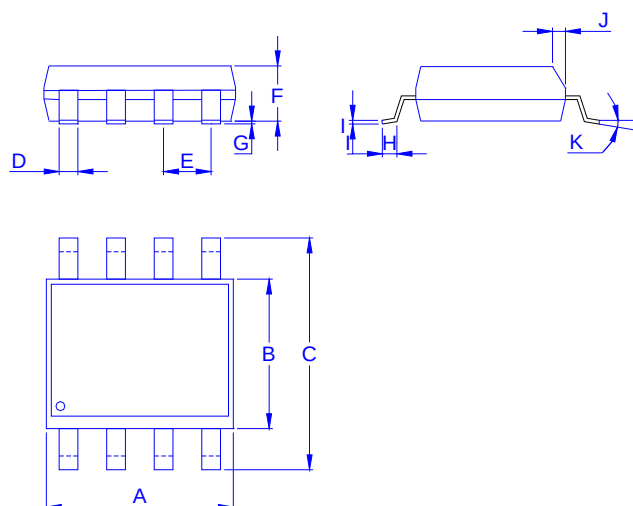
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMBA5A10G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

