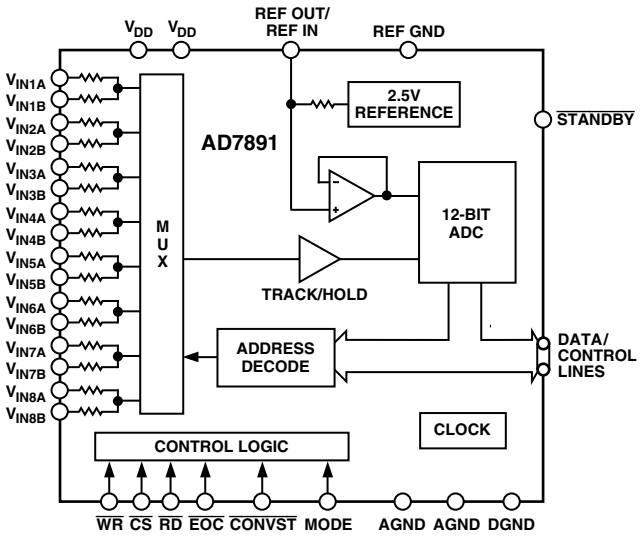
LC²MOS 8-Channel, 12-Bit High Speed Data Acquisition System

AD7891

FEATURES
- Fast 12-Bit ADC with 1.6 μs Conversion Time
- 8 Single-Ended Analog Input Channels
- Overvoltage Protection on Each Channel
- Selection of Input Ranges:
  - ±5 V, ±10 V for AD7891-1
  - 0 to +2.5 V, 0 to +5 V, ±2.5 V for AD7891-2
- Parallel and Serial Interface
- On-Chip Track/Hold Amplifier
- On-Chip Reference
- Single-Supply, Low Power Operation (100 mW Max)
- Power-Down Mode (75 μW Typ)

APPLICATIONS
- Data Acquisition Systems
- Motor Control
- Mobile Communication Base Stations
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7891 is an 8-channel, 12-bit data acquisition system with a choice of either parallel or serial interface structure. The part contains an input multiplexer, an on-chip track/hold amplifier, a high speed 12-bit ADC, a 2.5 V reference, and a high speed interface. The part operates from a single 5 V supply and accepts a variety of analog input ranges across two models, the AD7891-1 (±5 V and ±10 V) and the AD7891-2 (0 V to +2.5 V, 0 V to +5 V, and ±2.5 V).

The AD7891 provides the option of either a parallel or serial interface structure determined by the MODE pin. The part has standard control inputs and fast data access times for both the serial and parallel interfaces, ensuring easy interfacing to modern microprocessors, microcontrollers, and digital signal processors.

In addition to the traditional dc accuracy specifications, such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters, including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is 82 mW typical; in the standby mode, this is reduced to 75 μW typ. The part is available in a 44-terminal MQFP and a 44-lead PLCC.

PRODUCT HIGHLIGHTS

1. The AD7891 is a complete monolithic 12-bit data acquisition system that combines an 8-channel multiplexer, 12-bit ADC, 2.5 V reference, and track/hold amplifier on a single chip.
2. The AD7891-2 features a conversion time of 1.6 μs and an acquisition time of 0.4 μs. This allows a sample rate of 500 kSPS when sampling one channel and 62.5 kSPS when channel hopping. These sample rates can be achieved using either a software or hardware convert start. The AD7891-1 has an acquisition time of 0.6 μs when using a hardware convert start and an acquisition time of 0.7 μs when using a software convert start. These acquisition times allow sample rates of 454.5 kSPS and 435 kSPS, respectively, for hardware and software convert start.
3. Each channel on the AD7891 has overvoltage protection. This means an overvoltage on an unselected channel does not affect the conversion on a selected channel. The AD7891-1 can withstand overvoltages of ±17 V.

REV. D

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703 © 2004 Analog Devices, Inc. All rights reserved.

AD7891–SPECIFICATIONS (V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, REF IN = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version	Y Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					Sample Rate = 454.5 kSPS[3] (AD7891-1), 500 kSPS[3] (AD7891-2). Any channel.
Signal-to-(Noise + Distortion) Ratio[4]					
@ 25°C	70	70	70	dB min	
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion[4]	–78	–78	–78	dB max	
Peak Harmonic or Spurious Noise[4]	–80	–80	–80	dB max	
Intermodulation Distortion[4]					fa = 9 kHz, fb = 9.5 kHz.
Second-Order Terms	–80	–80	–80	dB typ	
Third-Order Terms	–80	–80	–80	dB typ	
Channel-to-Channel Isolation[4]	–80	–80	–80	dB max	
DC ACCURACY					Any channel.
Resolution	12	12	12	Bits	
Minimum Resolution for which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy[4]	±1	±0.75	±1	LSB max	
Differential Nonlinearity[4]	±1	±1	±1	LSB max	
Positive Full-Scale Error[4]	±3	±3	±3	LSB max	
Positive Full-Scale Error Match[4, 5]	0.6	0.6	0.6	LSB typ	1.5 LSB max.
Unipolar Offset Error	±4	±4	±4	LSB max	Input ranges of 0 V to 2.5 V, 0 V to 5 V.
Unipolar Offset Error Match[5]	0.1	0.1	0.1	LSB typ	1 LSB max.
Negative Full-Scale Error[4]	±3	±3	±3	LSB max	Input ranges of ±2.5 V, ±5 V, ±10 V.
Negative Full-Scale Error Match[4, 5]	0.6	0.6	0.6	LSB typ	1.5 LSB max.
Bipolar Zero Error	±4	±4	±4	LSB max	Input ranges of ±2.5 V, ±5 V, ±10 V.
Bipolar Zero Error Match[5]	0.2	0.2	0.2	LSB typ	1.5 LSB max.
ANALOG INPUTS					
AD7891-1 Input Voltage Range					
	±5	±5	±5	V	Input applied to both V_{INXA} and V_{INXB}.
	±10	±10	±10	V	Input applied to V_{INXA}, V_{INXB} = AGND.
AD7891-1 V_{INXA} Input Resistance	7.5	7.5	7.5	kΩ min	Input range of ±5 V.
AD7891-1 V_{INXA} Input Resistance	15	15	15	kΩ min	Input range of ±10 V.
AD7891-2 Input Voltage Range	0 to 2.5	0 to 2.5	0 to 2.5	V	Input applied to both V_{INXA} and V_{INXB}.
	0 to 5	0 to 5	0 to 5	V	Input applied to V_{INXA}, V_{INXB} = AGND.
	±2.5	±2.5	±2.5	V	Input applied to V_{INXA}, V_{INXB} = REF IN[6].
AD7891-2 V_{INXA} Input Resistance	1.5	1.5	1.5	kΩ min	Input ranges of ±2.5 V and 0 V to 5 V.
AD7891-2 V_{INXA} Input Current	±50	±50	±50	nA max	Input range of 0 V to 2.5 V.
REFERENCE INPUT/OUTPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%.
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor connected to internal reference node.
Input Capacitance[5]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ 25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±20	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	5	5	5	kΩ nom	See REF IN input impedance.
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%.
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%.
Input Current, I_{INH}	±10	±10	±10	μA max	
Input Capacitance[5] C_{IN}	10	10	10	pF max	

Parameter	A Version[1]	B Version	Y Version	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 μA.
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA.
DB11to DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Capacitance[5]	15	15	15	pF max	
Output Coding					
	Straight (Natural) Binary				Data format bit of control register = 0.
	Twos Complement				Data format bit of control register = 1.
CONVERSION RATE					
Conversion Time	1.6	1.6	1.6	μs max	
Track/Hold Acquisition Time	0.6	0.6	0.6	μs max	AD7891-1 hardware conversion.
	0.7	0.7	0.7	μs max	AD7891-1 software conversion.
	0.4	0.4	0.4	μs max	AD7891-2.
POWER REQUIREMENTS					
V_{DD}	5	5	5	V nom	±5% for specified performance.
I_{DD}					
Normal Mode	20	20	21	mA max	
Standby Mode	80	80	80	μA max	Logic inputs = 0 V or V_{DD}.
Power Dissipation					V_{DD} = 5 V.
Normal Mode	100	100	105	mW max	Typically 82 mW.
Standby Mode	400	400	400	μW max	Typically 75 μW.

NOTES
[1]Temperature ranges for the A and B Versions: –40°C to +85°C. Temperature range for the Y Version: –55°C to +105°C.
[2]The AD7891-1's dynamic performance (THD and SNR) and the AD7891-2's THD are measured with an input frequency of 10 kHz. The AD7891-2's SNR is evaluated with an input frequency of 100 kHz.
[3]This throughput rate can only be achieved when the part is operated in the parallel interface mode. Maximum achievable throughput rate in the serial interface mode is 357 kSPS.
[4]See the Terminology section.
[5]Sample tested during initial release and after any redesign or process change that may affect this parameter.
[6]REF IN must be buffered before being applied to V_{INXB}.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C, unless otherwise noted)

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
Analog Input Voltage to AGND
  AD7891-1 . . . . . ±17 V
  AD7891-2 . . . . . –5 V, +10 V
Reference Input Voltage to AGND . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A, B Versions) . . . . . –40°C to +85°C
  Automotive (Y Version) . . . . . –55°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
MQFP Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 95°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . 215°C
    Infrared (15 sec) . . . . . 220°C
PLCC Package, Power Dissipation . . . . . 500 mW
  θ_{JA} Thermal Impedance . . . . . 55°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . 215°C
    Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7891 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TIMING CHARACTERISTICS[1, 2]

Parameter	A, B, Y Versions	Unit	Test Conditions/Comments
t_{CONV}	1.6	μs max	Conversion Time
Parallel Interface			
t_1	0	ns min	$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time
t_2	35	ns min	Write Pulse Width
t_3	25	ns min	Data Valid to Write Setup Time
t_4	5	ns min	Data Valid to Write Hold Time
t_5	0	ns min	$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time
t_6	35	ns min	$\overline{CONVST}$ Pulse Width
t_7	55	ns min	$\overline{EOC}$ Pulse Width
t_8	35	ns min	Read Pulse Width
t_9[3]	25	ns min	Data Access Time after Falling Edge of $\overline{RD}$
t_{10}[4]	5	ns min	Bus Relinquish Time after Rising Edge of $\overline{RD}$
	30	ns max	
Serial Interface			
t_{11}	30	ns min	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
t_{12}[3]	20	ns max	$\overline{RFS}$ Low to Data Valid Delay
t_{13}	25	ns min	SCLK High Pulse Width
t_{14}	25	ns min	SCLK Low Pulse Width
t_{15}[3]	5	ns min	SCLK Rising Edge to Data Valid Hold Time
t_{16}[3]	15	ns max	SCLK Rising Edge to Data Valid Delay
t_{17}	20	ns min	$\overline{RFS}$ to SCLK Falling Edge Hold Time
t_{18}[4]	0	ns min	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
	30	ns max	
t_{18A}[4]	0	ns min	Bus Relinquish Time after Rising Edge of SCLK
	30	ns max	
t_{19}	20	ns min	$\overline{TFS}$ Low to SCLK Falling Edge Setup Time
t_{20}	15	ns min	Data Valid to SCLK Falling Edge Setup Time
t_{21}	10	ns min	Data Valid to SCLK Falling Edge Hold Time
t_{22}	30	ns min	$\overline{TFS}$ Low to SCLK Falling Edge Hold Time

NOTES

[1]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with tr = tf = 1 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 2, 3, and 4.

[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Specifications subject to change without notice.

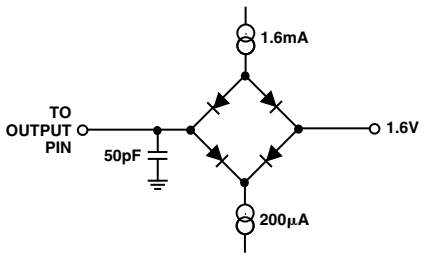


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

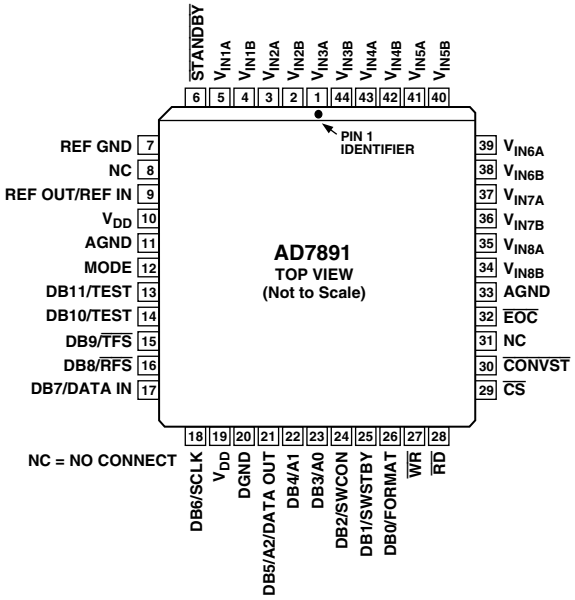
ORDERING GUIDE

Model	Input Range	Sample Rate	Relative Accuracy	Temperature Range	Package Option[1]
AD7891ACHIPS-1					DIE
AD7891ACHIPS-2					DIE
AD7891AS-1	±5 V or ±10 V	454 kSPS	±1 LSB	–40°C to +85°C	S-44
AD7891ASZ-1[2]	±5 V or ±10 V	454 kSPS	±1 LSB	–40°C to +85°C	S-44
AD7891AP-1	±5 V or ±10 V	454 kSPS	±1 LSB	–40°C to +85°C	P-44A
AD7891AP-1REEL	±5 V or ±10 V	454 kSPS	±1 LSB	–40°C to +85°C	P-44A
AD7891BS-1	±5 V or ±10 V	454 kSPS	±0.75 LSB	–40°C to +85°C	S-44
AD7891BP-1	±5 V or ±10 V	454 kSPS	±0.75 LSB	–40°C to +85°C	P-44A
AD7891BP-1REEL	±5 V or ±10 V	454 kSPS	±0.75 LSB	–40°C to +85°C	P-44A
AD7891YS-1	±5 V or ±10 V	454 kSPS	±1 LSB	–55°C to +105°C	S-44
AD7891YS-1REEL	±5 V or ±10 V	454 kSPS	±1 LSB	–55°C to +105°C	S-44
AD7891YP-1	±5 V or ±10 V	454 kSPS	±1 LSB	–55°C to +105°C	P-44A
AD7891YP-1REEL	±5 V or ±10 V	454 kSPS	±1 LSB	–55°C to +105°C	P-44A
AD7891AS-2	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	S-44
AD7891ASZ-2[2]	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	S-44
AD7891AP-2	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	P-44A
AD7891AP-2REEL	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	P-44A
AD7891BS-2	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±0.75 LSB	–40°C to +85°C	S-44
AD7891BP-2	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±0.75 LSB	–40°C to +85°C	P-44A
AD7891BP-2REEL	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±0.75 LSB	–40°C to +85°C	P-44A
AD7891YS-2	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±1 LSB	–55°C to +105°C	S-44
AD7891YS-2REEL	0 V to +5 V, 0 V to +2.5 V, ±2.5 V	500 kSPS	±1 LSB	–55°C to +105°C	S-44
EVAL-AD7891-1CB					Evaluation Board
EVAL-AD7891-2CB					Evaluation Board

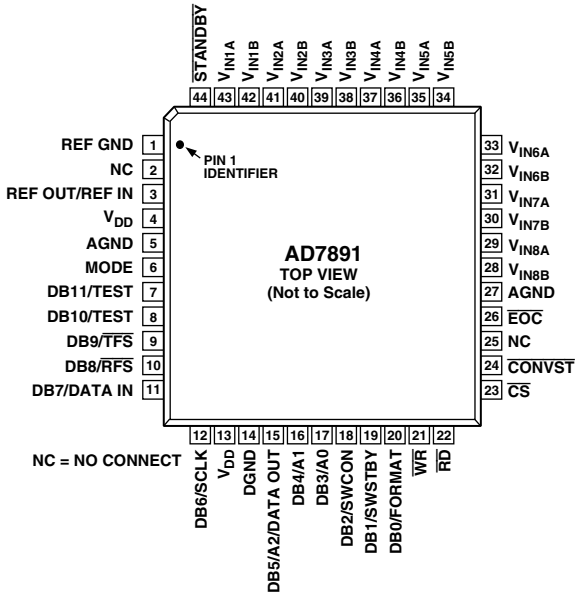
NOTES
[1]S = Plastic Quad Flatpack (MQFP); P = Plastic Leaded Chip Carrier (PLCC).
[2]Z = Pb-free part.

PIN CONFIGURATIONS

PLCC



MQFP



PIN FUNCTION DESCRIPTIONS

PLCC Pin No.	MQFP Pin No.	Mnemonic	Description
1–5 34–44	28–43	V_{INXA}, V_{INXB}	Analog Input Channels. The AD7891 contains eight pairs of analog input channels. Each channel contains two input pins to allow a number of different input ranges to be used with the AD7891. There are two possible input voltage ranges on the AD7891-1. The ±5 V input range is selected by connecting the input voltage to both V_{INXA} and V_{INXB}, while the ±10 V input range is selected by applying the input voltage to V_{INXA} and connecting V_{INXB} to AGND. The AD7891-2 has three possible input ranges. The 0 V to 2.5 V input range is selected by connecting the analog input voltage to both V_{INXA} and V_{INXB}; the 0 V to 5 V input range is selected by applying the input voltage to V_{INXA} and connecting V_{INXB} to AGND while the ±2.5 V input range is selected by connecting the analog input voltage to V_{INXA} and connecting V_{INXB} to REF IN (provided this REF IN voltage comes from a low impedance source). The channel to be converted is selected by the A2, A1, and A0 bits of the control register. In the parallel interface mode, these bits are available as three data input lines (DB3 to DB5) in a parallel write operation. While in the serial interface mode, these three bits are accessed via the DATA IN line in a serial write operation. The multiplexer has guaranteed break-before-make operation.
10, 19	4, 13	V_{DD}	Positive Supply Voltage, 5 V ± 5%.
11, 33	5, 27	AGND	Analog Ground. Ground reference for track/hold, comparator, and DAC.
20	14	DGND	Digital Ground. Ground reference for digital circuitry.
6	44	$\overline{\text{STANDBY}}$	Standby Mode Input. TTL compatible input used to put the device into the power save or standby mode. The $\overline{\text{STANDBY}}$ input is high for normal operation and low for standby operation.
9	3	REF OUT/REF IN	Voltage Reference Output/Input. The part can either be used with its own internal reference or with an external reference source. The on-chip 2.5 V reference voltage is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should be decoupled to REF GND with a 0.1 μF disc ceramic capacitor. The output impedance of the reference source is typically 2 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The reference pin is buffered on-chip but must be able to sink or source current through this 2 kΩ resistor to the output of the on-chip reference. The nominal reference voltage for correct operation of the AD7891 is 2.5 V.
7	1	REF GND	Reference Ground. Ground reference for the part's on-chip reference buffer. The REF OUT pin of the part should be decoupled with a 0.1 μF capacitor to this REF GND pin. If the AD7891 is used with an external reference, the external reference should also be decoupled to this pin. The REF GND pin should be connected to the AGND pin or the system's AGND plane.
30	24	$\overline{\text{CONVST}}$	Convert Start. Edge-triggered logic input. A low-to-high transition on this input puts the track/hold into hold and initiates conversion. When changing channels on the part, sufficient time should be given for multiplexer settling and track/hold acquisition between the channel change and the rising edge of $\overline{\text{CONVST}}$.
32	26	$\overline{\text{EOC}}$	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low-going pulse on this line. The duration of this $\overline{\text{EOC}}$ pulse is nominally 80 ns.
12	6	MODE	Interface Mode. Control input that determines the interface mode for the part. With this pin at a logic low, the AD7891 is in its serial interface mode; with this pin at a logic high, the device is in its parallel interface mode.

PARALLEL INTERFACE MODE FUNCTIONS

PLCC Pin No.	MQFP Pin No.	Mnemonic	Description
8, 31	2, 25	NC	No Connect. The two NC pins on the device can be left unconnected. If they are to be connected to a voltage, it should be to ground potential. To ensure correct operation of the AD7891, neither of the NC pins should be connected to a logic high potential.
29	23	$\overline{CS}$	Chip Select Input. Active low logic input that is used in conjunction with to enable the data outputs and with $\overline{WR}$ to allow input data to be written to the part.
28	22	$\overline{RD}$	Read Input. Active low logic input that is used in conjunction with $\overline{CS}$ low to enable the data outputs.
27	21	$\overline{WR}$	Write Input. Active low logic input used in conjunction with $\overline{CS}$ to latch the multiplexer address and software control information. The rising edge of this input also initiates an internal pulse. When using the software start facility, this pulse delays the point at which the track/hold goes into hold and conversion is initiated. This allows the multiplexer to settle and the acquisition time of the track/hold to elapse when a channel address is changed. If the SWCON bit of the control register is set to 1, when this pulse times out, the track/hold then goes into hold and conversion is initiated. If the SWCON bit of the control register is set to 0, the track/hold and conversion sequence are unaffected by $\overline{WR}$ operation.

Data I/O Lines

There are 12 data input/output lines on the AD7891. When the part is configured for parallel mode (MODE = 1), the output data from the part is provided at these 12 pins during a read operation. For a write operation in parallel mode, these lines provide access to the part's control register.

Parallel Read Operation

During a parallel read operation, the 12 lines become the 12 data bits containing the conversion result from the AD7891. These data bits are labelled Data Bit 0 (LSB) to Data Bit 11 (MSB). They are three-state, TTL compatible outputs. Output data coding is twos complement when the data FORMAT bit of the control register is 1, and straight binary when the data FORMAT bit of the control register is 0.

PLCC Pin No.	MQFP Pin No.	Mnemonic	Description
13 to 18, 21 to 26	7 to 12, 15 to 20	DB0 to DB11	Data Bit 0 (LSB) to Data Bit 11 (MSB). Three-state TTL compatible outputs that are controlled by the $\overline{CS}$ and $\overline{RD}$ inputs.

Parallel Write Operation

During a parallel write operation, the following functions can be written to the control register via the 12 data input/output pins.

PLCC Pin No.	MQFP Pin No.	Mnemonic	Description
23	17	A0	Address Input. The status of this input during a parallel write operation is latched to the A0 bit of the control register (see Control Register section).
22	16	A1	Address Input. The status of this input during a parallel write operation is latched to the A1 bit of the control register (see Control Register section).
21	15	A2	Address Input. The status of this input during a parallel write operation is latched to the A2 bit of the control register (see Control Register section).
24	18	SWCON	Software Conversion Start. The status of this input during a parallel write operation is latched to the SWCONV bit of the control register (see Control Register section).
25	19	SWSTBY	Software Standby Control. The status of this input during a parallel write operation is latched to the SWSTBY bit of the control register (see Control Register section).
26	20	FORMAT	Data Format Selection. The status of this input during a parallel write operation is latched to the FORMAT bit of the control register (see Control Register section).

SERIAL INTERFACE MODE FUNCTIONS

When the part is configured for serial mode (MODE = 0), five of the 12 data input/output lines provide serial interface functions. These functions are outlined below.

PLCC Pin No.	MQFP Pin No.	Mnemonic	Description
18	12	SCLK	Serial Clock Input. This is an externally applied serial clock that is used to load serial data to the control register and to access data from the output register.
15	9	$\overline{\text{TFS}}$	Transmit Frame Synchronization Pulse. Active low logic input with serial data expected after the falling edge of this signal.
16	10	$\overline{\text{RFS}}$	Receive Frame Synchronization Pulse. This is an active low logic input with $\overline{\text{RFS}}$ provided externally as a strobe or framing pulse to access serial data from the output register. For applications that require that data be transmitted and received at the same time, $\overline{\text{RFS}}$ and $\overline{\text{TFS}}$ should be connected together.
21	15	DATA OUT	Serial Data Output. Sixteen bits of serial data are provided with the data FORMAT bit and the three address bits of the control register preceding the 12 bits of conversion data. Serial data is valid on the falling edge of SCLK for 16 edges after $\overline{\text{RFS}}$ goes low. Output conversion data coding is twos complement when the FORMAT bit of the control register is 1 and straight binary when the FORMAT bit of the control register is 0.
17	11	DATA IN	Serial Data Input. Serial data to be loaded to the control register is provided at this input. The first six bits of serial data are loaded to the control register on the first six falling edges of SCLK after $\overline{\text{TFS}}$ goes low. Serial data on subsequent SCLK edges is ignored while $\overline{\text{TFS}}$ remains low.
13, 14	7, 8	TEST	Test Pin. When the device is configured for serial mode of operation, two of the pins which had been data inputs become test inputs. To ensure correct operation of the device, both TEST inputs should be tied to a logic low potential.

CONTROL REGISTER

The control register for the AD7891 contains six bits of information as described below. These six bits can be written to the control register either in a parallel mode write operation or via a serial mode write operation. The default (power-on) condition of all bits in the control register is 0. Six serial clock pulses must be provided to the part in order to write data to the control register. If $\overline{\text{TFS}}$ returns high before six serial clock cycles, no data transfer takes place to the control register and the write cycle has to be restarted to write data to the control register. However, if the SWCONV bit of the register was previously set to a Logic 1 and $\overline{\text{TFS}}$ is brought high before six serial clock cycles, another conversion is initiated.

LSB (DB0)

A2	**A1**	**A0**	**SWCONV**	**SWSTBY**	**FORMAT**

A2 — Address Input. This input is the most significant address input for multiplexer channel selection.

A1 — Address Input. This is the second most significant address input for multiplexer channel selection.

A0 — Address Input. Least significant address input for multiplexer channel selection. When the address is written to the control register, an internal pulse is initiated to allow for the multiplexer settling time and track/hold acquisition time before the track/hold goes into hold and conversion is initiated. When the internal pulse times out, the track/hold goes into hold and conversion is initiated. The selected channel is given by the formula

$$A2 \times 4 + A1 \times 2 + A0 + 1$$

SWCONV — Conversion Start. Writing a 1 to this bit initiates a conversion in a similar manner to the $\overline{\text{CONVST}}$ input. Continuous conversion starts do not take place when there is a 1 in this location. The internal pulse and the conversion process are initiated when a 1 is written to this bit. With a 1 in this bit, the hardware conversion start, i.e., the $\overline{\text{CONVST}}$ input, is disabled. Writing a 0 to this bit enables the hardware $\overline{\text{CONVST}}$ input.

SWSTBY — Standby Mode Input. Writing a 1 to this bit places the device in its standby or power-down mode. Writing a 0 to this bit places the device in its normal operating mode.

FORMAT — Data Format. Writing a 0 to this bit sets the conversion data output format to straight (natural) binary. This data format is generally used for unipolar input ranges. Writing a 1 to this bit sets the conversion data output format to twos complement. This output data format is generally used for bipolar input ranges.

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise +distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(Noise + Distortion) = (6.02N + 1.76) dB

Therefore, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7891, it is defined as

$$THD\left(\text{dB}\right) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa – fb), while the third-order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb).

The AD7891 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second- and third-order terms are of different significance. The second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and-third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 20 kHz (AD7891-1) or 100 kHz (AD7891-2) sine wave signal to one input channel and determining how much that signal is attenuated in each of the other channels. The figure given is the worst case across all eight channels.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error (AD7891-1, ±10 V and ±5 V; AD7891-2, ±2.5 V)
This is the deviation of the last code transition (01. . .110 to 01. . .111) from the ideal 4 × REF IN – 3/2 LSB (AD7891-1 ±10 V range), 2 × REF IN – 3/2 LSB (AD7891-1 ± 5 V range), or REF IN – 3/2 LSB (AD7891-2, ±2.5 V range), after the bipolar zero error has been adjusted out.

Positive Full-Scale Error (AD7891-2, 0 V to 5 V and 0 V to 2.5 V)
This is the deviation of the last code transition (11. . .110 to 11. . .111) from the ideal 2 × REF IN – 3/2 LSB (0 V to 5 V range), or REF IN – 3/2 LSB (0 V to 2.5 V range), after the unipolar offset error has been adjusted out.

Bipolar Zero Error (AD7891-1, ±10 V and ±5 V; AD7891-2, ±2.5 V)
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal AGND – 1/2 LSB.

Unipolar Offset Error (AD7891-2, 0 V to 5 V and 0 V to 2.5 V)
This is the deviation of the first code transition (00. . .000 to 00. . .001) from the ideal AGND + 1/2 LSB.

Negative Full-Scale Error (AD7891-1, ±10 V and ±5 V; AD7891-2, ±2.5 V)
This is the deviation of the first code transition (10. . .000 to 10. . .001) from the ideal –4 × REF IN + 1/2 LSB (AD7891-1 ±10 V range), –2 × REF IN + 1/2 LSB (AD7891-1 ± 5 V range), or –REF IN + 1/2 LSB (AD7891-2, ±2.5 V range), after bipolar zero error has been adjusted out.

Track/Hold Acquisition Time
Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7891. It means the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a channel change/step input change to V_{IN} before starting another conversion, to ensure the part operates to specification.

CONVERTER DETAILS

The AD7891 is an 8-channel, high speed, 12-bit data acquisition system. It provides the user with signal scaling, multiplexer, track/hold, reference, ADC, and high speed parallel and serial interface logic functions on a single chip. The signal conditioning on the AD7891-1 allows the part to accept analog input ranges of ±5 V or ±10 V when operating from a single supply. The input circuitry on the AD7891-2 allows the part to handle input signal ranges of 0 V to +2.5 V, 0 V to +5 V, and ±2.5 V again while operating from a single 5 V supply. The part requires a 2.5 V reference that can be provided from the part's own internal reference or from an external reference source.

Conversion is initiated on the AD7891 either by pulsing the $\overline{\text{CONVST}}$ input or by writing a Logic 1 to the SWCONV bit of the control register. When using the hardware $\overline{\text{CONVST}}$ input, the on-chip track/hold goes from track to hold mode and the conversion sequence is started on the rising edge of the $\overline{\text{CONVST}}$ signal. When a software conversion start is initiated, an internal pulse is generated, delaying the track/hold acquisition point and the conversion start sequence until the pulse is timed out. This internal pulse is initiated (goes from low to high) whenever a write to the AD7891 control register takes place with a 1 in the SWCONV bit. It then starts to discharge and the track/hold cannot go into hold and conversion cannot be initiated until the pulse signal goes low. The internal pulse duration is equal to the track/hold acquisition time. This allows the user to obtain a valid result after changing channels and initiating a conversion in the same write operation.

The conversion clock for the part is internally generated and conversion time for the AD7891 is 1.6 µs from the rising edge of the hardware $\overline{\text{CONVST}}$ signal. The track/hold acquisition time for the AD7891-1 is 600 ns, while the track/hold acquisition time for the AD7891-2 is 400 ns. To obtain optimum performance from the part, the data read operation should not occur during the conversion or during the 100 ns prior to the next conversion. This allows the AD7891-1 to operate at throughput rates up to 454.5 kSPS and the AD7891-2 to operate at throughput rates up to 500 kSPS in the parallel mode and achieve data sheet specifications. In the serial mode, the maximum achievable throughput rate for both the AD7891-1 and the AD7891-2 is 357 kSPS (assuming a 20 MHz serial clock).

All unused analog inputs should be tied to a voltage within the nominal analog input range to avoid noise pickup. For minimum power consumption, the unused analog inputs should be tied to AGND.

INTERFACE INFORMATION

The AD7891 provides two interface options, a 12-bit parallel interface and a high speed serial interface. The required interface mode is selected via the MODE pin. The two interface modes are discussed in the following sections.

Parallel Interface Mode

The parallel interface mode is selected by tying the MODE input to a logic high. Figure 2 shows a timing diagram illustrating the operational sequence of the AD7891 in parallel mode for a hardware conversion start. The multiplexer address is written to the AD7891 on the rising edge of the $\overline{\text{WR}}$ input. The on-chip track/hold goes into hold mode on the rising edge of $\overline{\text{CONVST}}$; conversion is also initiated at this point. When the conversion is complete, the end of conversion line ($\overline{\text{EOC}}$) pulses low to indicate that new data is available in the AD7891's output register. This $\overline{\text{EOC}}$ line can be used to drive an edge-triggered interrupt of a microprocessor. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ going low accesses the 12-bit conversion result. In systems where the part is interfaced to a gate array or ASIC, this $\overline{\text{EOC}}$ pulse can be applied to the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs to latch data out of the AD7891 and into the gate array or ASIC. This means the gate array or ASIC does not need any conversion status recognition logic, and it also eliminates the logic required in the gate array or ASIC to generate the read signal for the AD7891.

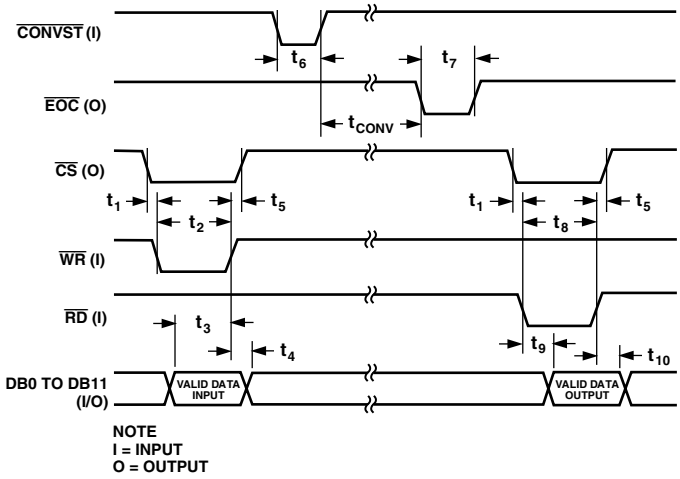


Figure 2. Parallel Mode Timing Diagram

Serial Interface Mode

The serial interface mode is selected by tying the MODE input to a logic low. In this case, five of the data/control inputs of the parallel mode assume serial interface functions.

The serial interface on the AD7891 is a 5-wire interface with read and write capabilities, with data being read from the output register via the DATA OUT line and data being written to the control register via the DATA IN line. The part operates in a slave or external clocking mode and requires an externally applied serial clock to the SCLK input to access data from the data register or write data to the control register. There are separate framing signals for the read ($\overline{RFS}$) and write ($\overline{TFS}$) operations. The serial interface on the AD7891 is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data, such as the 80C51, 87C51, 68HC11, and 68HC05, and most digital signal processors.

When using the AD7891 in serial mode, the data lines DB11 to DB10 should be tied to logic low, and the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ inputs should be tied to logic high. Pins DB4 to DB0 can be tied to either logic high or logic low but must not be left floating because this condition could cause the AD7891 to draw large amounts of current.

Read Operation

Figure 3 shows the timing diagram for reading from the AD7891 in serial mode. $\overline{RFS}$ goes low to access data from the AD7891. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Sixteen bits of data are transmitted in serial mode with the data FORMAT bit first, followed by the three address bits in the control register, followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. At the end of the read operation, the DATA OUT line is three-stated by a rising edge on either the SCLK or $\overline{RFS}$ inputs, whichever occurs first.

Write Operation

Figure 4 shows a write operation to the control register of the AD7891. The $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. The AD7891 control register requires only six bits of data. These are loaded on the first six clock cycles of the serial clock with data on all subsequent clock cycles being ignored. Serial data to be written to the AD7891 must be valid on the falling edge of SCLK.

Simplifying the Serial Interface

To minimize the number of interconnect lines to the AD7891 in serial mode, the user can connect the $\overline{RFS}$ and $\overline{TFS}$ lines of the AD7891 together and read and write from the part simultaneously. In this case, a new control register data line selecting the input channel and providing a conversion start command should be provided on the DATA IN line, while the part provides the result from the conversion just completed on the DATA OUT line.

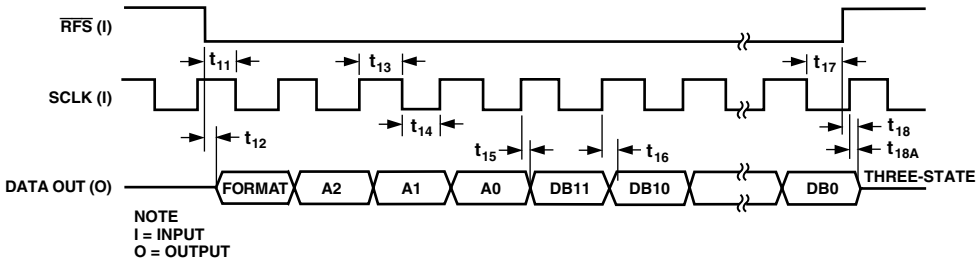


Figure 3. Serial Mode Read Operation

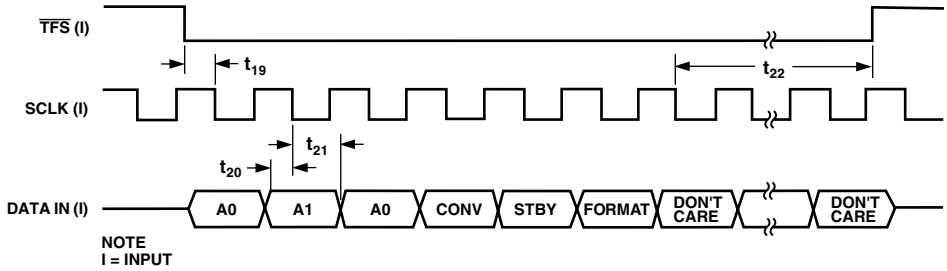


Figure 4. Serial Mode Write Operation

CIRCUIT DESCRIPTION

Reference

The AD7891 contains a single reference pin labeled REF OUT/REF IN that either provides access to the part's own 2.5 V internal reference or to which an external 2.5 V reference can be connected to provide the reference source for the part. The part is specified with a 2.5 V reference voltage. Errors in the reference source result in gain errors in the transfer function of the AD7891 and add to the specified full-scale errors on the part. They also result in an offset error injected into the attenuator stage.

The AD7891 contains an on-chip 2.5 V reference. To use this reference as a reference source for the AD7891, simply connect a 0.1 μF disc ceramic capacitor from the REF OUT/REF IN pin to REFGND. REFGND should be connected to AGND or the analog ground plane. The voltage that appears at the REF OUT/REF IN pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7891, it should be buffered since the part has a FET switch in series with the reference, resulting in a source impedance for this output of 2 kΩ nominal. The tolerance of the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±20 mV.

If the application requires a reference with a tighter tolerance or if the AD7891 needs to be used with a system reference, an external reference can be connected to the REF OUT/REF IN pin. The external reference overdrives the internal reference and thus provides the reference source for the ADC. The reference input is buffered before being applied to the ADC and the maximum input current is ±100 μA. Suitable reference for the AD7891 include the AD580, the AD680, the AD780, and the REF43 precision 2.5 V references.

Analog Input Section

The AD7891 is offered as two part types: the AD7891-1 where each input can be configured to have a ±10 V or a ±5 V input range, and the AD7891-2 where each input can be configured to have a 0 V to +2.5 V, 0 V to +5 V, and ±2.5 V input range.

AD7891-1

Figure 5 shows the analog input section of the AD7891-1. Each input can be configured for ±5 V or ±10 V operation. For 5 V operation, the V_{INXA} and V_{INXB} inputs are tied together and the input voltage is applied to both. For ±10 V operation, the V_{INXB} input is tied to AGND and the input voltage is applied to the V_{INXA} input. The V_{INXA} and V_{INXB} inputs are symmetrical and fully interchangeable. Therefore, for ease of PCB layout on the ±10 V range, the input voltage may be applied to the V_{INXB} input while the V_{INXA} input is tied to AGND.

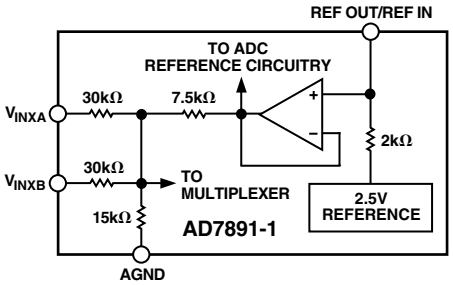


Figure 5. AD7891-1 Analog Input Structure

The input resistance for the ±5 V range is typically 20 kΩ. For the ±10 V input range, the input resistance is typically 34.3 kΩ. The resistor input stage is followed by the multiplexer, which is followed by the high input impedance stage of the track/hold amplifier.

The designed code transitions take place midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). LSB size is given by the formula 1 LSB = F_S/4096. Therefore, for the ±5 V range, 1 LSB = 10 V/4096 = 2.44 mV. For the ±10 V range, 1 LSB = 20 V/4096 = 4.88 mV. Output coding is determined by the FORMAT bit of the control register. The ideal input/output code transitions are shown in Table I.

AD7891-2

Figure 6 shows the analog input section of the AD7891-2. Each input can be configured for input ranges of 0 V to +5 V, 0 V to +2.5 V, or ±2.5 V. For the 0 V to 5 V input range, the V_{INXB} input is tied to AGND and the input voltage is applied to the V_{INXA} input. For the 0 V to 2.5 V input range, the V_{INXA} and V_{INXB} inputs are tied together and the input voltage is applied to both. For the ±2.5 V input range, the V_{INXB} input is tied to 2.5 V and the input voltage is applied to the V_{INXA} input. The 2.5 V source must have a low output impedance. If the internal reference on the AD7891 is used, it must be buffered before being applied to V_{INXB}. The V_{INXA} and V_{INXB} inputs are symmetrical and fully interchangeable. Therefore, for ease of PCB layout on the 0 V to +5 V or ±2.5 V range, the input voltage may be applied to the V_{INXB} input, while the V_{INXA} input is tied to AGND or 2.5 V.

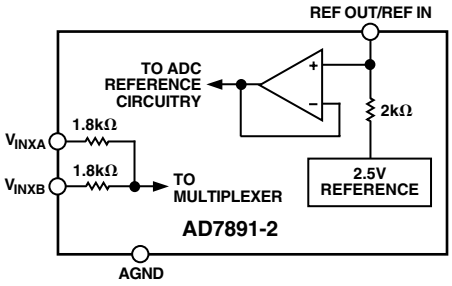


Figure 6. AD7891-2 Analog Input Structure

The input resistance for both the 0 V to +5 V and ±2.5 V ranges is typically 3.6 kΩ. When an input is configured for 0 V to 2.5 V operation, the input is fed into the high impedance stage of the track/hold amplifier via the multiplexer and the two 1.8 kΩ resistors in parallel.

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). LSB size is given by the formula 1 LSB = F_S/4096. Therefore, for the 0 V to 5 V range, 1 LSB = 5 V/4096 = 1.22 mV, for the 0 V to 2.5 V range, 1 LSB = 2.5 V/4096 = 0.61 mV, and for the ±2.5 V range, 1 LSB = 5 V/4096 = 1.22 mV. Output coding is determined by the FORMAT bit in the control register. The ideal input/output code transitions for the ±2.5 V range are shown in Table I. The ideal input/output code transitions for the 0 V to 5 V range and the 0 V to 2.5 V range are shown in Table II.

Table I. Ideal Code Transition Table for the AD7891-1, ±10 V and ±5 V Ranges and the AD7891-2, ±2.5 V Range

Analog Input	Input Voltage	Digital Output Code Transition[1]	
		Twos Complement	Straight Binary
+FSR[2]/2 – 3/2 LSB[3]	(9.99268 V, 4.99634 V or 2.49817 V)[4]	011...110 to 011...111	111...110 to 111...111
+FSR/2 – 5/2 LSB	(9.98779 V, 4.99390 V or 2.49695 V)	011...101 to 011...110	111...101 to 111...110
+FSR/2 – 7/2 LSB	(9.99145 V, 4.99146 V or 2.49573 V)	011...100 to 011...101	111...100 to 111...101
AGND + 3/2 LSB	(7.3242 mV, 3.6621 mV or 1.8310 mV)	000...001 to 000...010	100...001 to 100...010
AGND + 1/2 LSB	(2.4414 mV, 1.2207 mV or 0.6103 mV)	000...000 to 000...001	100...000 to 100...001
AGND – 1/2 LSB	(–2.4414 mV, –1.2207 mV or –0.6103 mV)	111...111 to 000...000	011...111 to 100...000
AGND – 3/2 LSB	(–7.3242 mV, –3.6621 mV or –1.8310 mV)	111...110 to 111...111	011...110 to 011...111
–FSR/2 + 5/2 LSB	(–9.98779 V, –4.99390 V or –2.49695 V)	100...010 to 100...011	000...010 to 000...011
–FSR/2 + 3/2 LSB	(–9.99268 V, –4.99634 V or –2.49817 V)	100...001 to 100...010	000...001 to 000...010
–FSR/2 + 1/2 LSB	(–9.99756 V, –4.99878 V or –2.49939 V)	100...000 to 100...001	000...000 to 000...001

NOTES
[1]Output code format is determined by the FORMAT bit in the control register.
[2]FSR is full-scale range and is +20 V for the ±10 V range, +10 V for the ±5 V range, and +5 V for the ±2.5 V range, with REF IN = +2.5 V.
[3]1 LSB = FSR/4096 = +4.88 mV (±10 V range), +2.44 mV (±5 V range), and +1.22 mV (±2.5 V range), with REF IN = +2.5 V.
[4]±10 V range, ±5 V range, or ±2.5 V range.

Table II. Ideal Code Transition Table for the AD7891-2, 0 V to 5 V and 0 V to 2.5 V Ranges

Analog Input	Input Voltage	Digital Output Code Transition[1]	
		Twos Complement	Straight Binary
+FSR[2] – 3/2 LSB[3]	(4.99817 V or 2.49908 V)[4]	011...110 to 011...111	111...110 to 111...111
+FSR – 5/2 LSB	(4.99695 V or 2.49847 V)	011...101 to 011...110	111...101 to 111...110
+FSR – 7/2 LSB	(4.99573 V or 2.49786 V)	011...100 to 011...101	111...100 to 111...101
AGND + 5/2 LSB	(3.0518 mV or 1.52588 mV)	100...010 to 000...011	000...010 to 000...011
AGND + 3/2 LSB	(1.83105 mV or 0.9155 mV)	100...001 to 000...010	000...001 to 000...010
AGND + 1/2 LSB	(0.6103 mV or 0.3052 mV)	100...000 to 000...001	000...000 to 000...001

NOTES
[1]Output code format is determined by the FORMAT bit in the control register.
[2]FSR is the full-scale range and is 5 V for the 0 to 5 V range and 2.5 V for the 0 to 2.5 V range, with REF IN = 2.5 V.
[3]1 LSB = F_S/4096 = 1.22 mV (0 to 5 V range) or 610 µV (0 to 2.5 V range), with REF IN = 2.5 V.
[4]0 V to 5 V range or 0 V to 2.5 V range.

Transfer Function of the AD7891-1 and AD7891-2

The transfer function of the AD7891-1 and AD7891-2 can be expressed as

$$Input\ Voltage = \left(M \times REF\ IN \times D/4096\right) + \left(N \times REF\ IN\right)$$

D is the output data from the AD7891 and is in the range 0 to 4095 for straight binary encoding and from –2048 to +2047 for twos complement encoding. Values for *M* depend upon the input voltage range. Values for *N* depend upon the input voltage range and the output data format. These values are given in Table III. *REF IN* is the reference voltage applied to the AD7891.

Table III. Transfer Function M and N Values

Range	Output Data Format	M	N
AD7891-1			
±10 V	Straight Binary	8	–4
±10 V	Twos Complement	8	0
±5 V	Straight Binary	4	–2
±5 V	Twos Complement	4	0
AD7891-2			
0 V to +5 V	Straight Binary	2	0
0 V to +5 V	Twos Complement	2	1
0 V to +2.5 V	Straight Binary	1	0
0 V to +2.5 V	Twos Complement	1	0.5
±2.5 V	Straight Binary	2	–1
±2.5 V	Twos Complement	2	0

Track/Hold Amplifier

The track/hold amplifier on the AD7891 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 454 kHz (AD7891-1) or 500 kHz (AD7891-2). In other words, the track/hold amplifier can handle input frequencies in excess of 227 kHz (AD7891-1) or 250 kHz (AD7891-2).

The track/hold amplifier acquires an input signal in 600 ns (AD7891-1) or 400 ns (AD7891-2). The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode on the rising edge of $\overline{\text{CONVST}}$. The aperture time for the track/hold (i.e., the delay between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns. At the end of conversion, the part returns to its tracking mode. The track/hold starts acquiring the next signal at this point.

$\overline{\text{STANDBY}}$ Operation

The AD7891 can be put into power save or standby mode by using the $\overline{\text{STANDBY}}$ pin or the SWSTBY bit of the control register. Normal operation of the AD7891 takes place when the $\overline{\text{STANDBY}}$ input is at a Logic 1 and the SWSTBY bit is at a Logic 0. When the $\overline{\text{STANDBY}}$ pin is brought low or a 1 is written to the SWSTBY bit, the part goes into its standby mode of operation, reducing its power consumption to typically 75 μW.

The AD7891 is returned to normal operation when the $\overline{\text{STANDBY}}$ input is at a Logic 1 and the SWSTBY bit is a Logic 0. The wake-up time of the AD7891 is normally determined by the amount of time required to charge the 0.1 μF capacitor between the REF OUT/REF IN pin and REF GND. If the internal reference is being used as the reference source, this capacitor is charged via a nominal 2 kΩ resistor. Assuming 10 time constants to charge the capacitor to 12-bit accuracy, this implies a wake-up time of 2 ms.

If an external reference is used, this must be taken into account when working out how long it will take to charge the capacitor. If the external reference has remained at 2.5 V during the time the AD7891 was in standby mode, the capacitor will already be charged when the part is taken out of standby mode. Therefore, the wake-up time is now the time required for the internal circuitry of the AD7891 to settle to 12-bit accuracy. This typically takes 5 μs. If the external reference was also put into standby then the wake-up time of the reference, combined with the amount of time taken to recharge the reference capacitor from the external reference, determines how much time must elapse before conversions can begin again.

MICROPROCESSOR INTERFACING

AD7891 to 8X51 Serial Interface

A serial interface between the AD7891 and the 8X51 microcontroller is shown in Figure 7. TXD of the 8X51 drives SCLK of the AD7891, while RXD transmits data to and receives data from the part. The serial clock speed of the 8X51 is slow compared to the maximum serial clock speed of the AD7891, so maximum throughput of the AD7891 is not achieved with this interface.

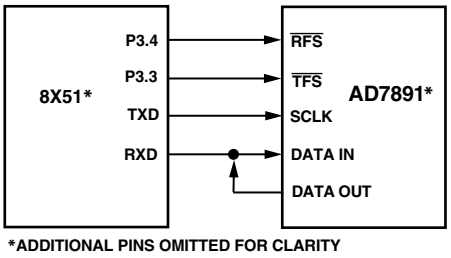


Figure 7. AD7891 to 8X51 Interface

The 8X51 provides the LSB of its SBUF register as the first bit in the serial data stream. The AD7891 expects the MSB of the 6-bit write first. Therefore, the data in the SBUF register must be arranged correctly so that this is taken into account. When data is to be transmitted to the part, P3.3 is taken low. The 8X51 transmits its data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. One 8-bit transfer is needed to write data to the control register of the AD7891. After the data has been transferred, the P3.3 line is taken high to complete the transmission.

When reading data from the AD7891, P3.4 of the 8X51 is taken low. Two 8-bit serial reads are performed by the 8X51, and P3.4 is taken high to complete the transfer. Again, the 8X51 expects the LSB first, while the AD7891 transmits MSB first, so this must be taken into account in the 8X51 software.

No provision has been made in the given interface to determine when a conversion has ended. If the conversions are initiated by software, the 8X51 can wait a predetermined amount of time before reading back valid data. Alternately, the falling edge of the $\overline{\text{EOC}}$ signal can be used to initiate an interrupt service routine that reads the conversion result from part to part.

AD7891 to 68HC11 Serial Interface

Figure 8 shows a serial interface between the AD7891 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7891, the MOSI output drives DATA IN of the AD7891, and the MISO input receives data from DATA OUT of the AD7891. Ports PC6 and PC7 of the 68HC11 drive the $\overline{\text{TFS}}$ and $\overline{\text{RFS}}$ lines of the AD7891, respectively.

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 1 and its CPHA bit is a 0. When data is to be transferred to the AD7891, PC7 is taken low. When data is to be received from the AD7891, PC6 is taken low. The 68HC11 transmits and receives its serial data in 8-bit bytes, MSB first. The AD7891 also transmits and receives data MSB first. Eight falling clock edges occur in a read or write cycle from the 68HC11. A single 8-bit write with PC7 low is required to write to the control register. When data has been written, PC7 is taken high. When reading from the AD7891, PC6 is left low after the first eight bits have been read. A second byte of data is then transmitted serially from the AD7891. When this transfer is complete, the PC6 line is taken high.

As in the 8X51 circuit in Figure 7, the way the 68HC11 is informed that a conversion is completed is not shown in the diagram. The $\overline{EOC}$ line can be used to inform the 68HC11 that a conversion is complete by using it as an interrupt signal. The interrupt service routine reads in the result of the conversion. If a software conversion start is used, the 68HC11 can wait for 2.0 µs (AD7891-2) or 2.2 µs (AD7891-1) before reading from the AD7891.

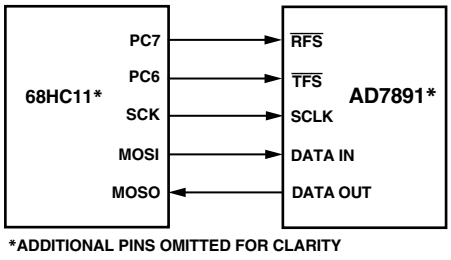


Figure 8. AD7891 to 68HC11 Interface

AD7891 to ADSP-21xx Serial Interface

An interface between the AD7891 and the ADSP-21xx is shown in Figure 9. In the interface shown, either SPORT0 or SPORT1 can be used to transfer data to the AD7891. When reading from the part, the SPORT must be set up with a serial word length of 16 bits. When writing to the AD7891, a serial word length of 6 bits or more can be used. Other setups for the serial interface on the ADSP-21xx internal SCLK use alternate framing mode and active low framing signal. Normally, the $\overline{EOC}$ line from the AD7891 would be connected to the $\overline{IRQ2}$ line of the ADSP-21xx to interrupt the DSP at the end of a conversion (not shown in diagram).

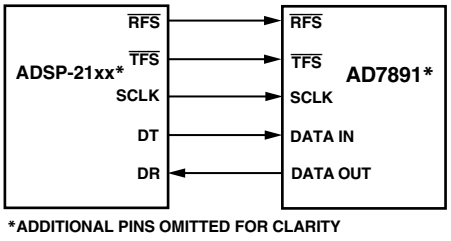


Figure 9. AD7891 to ADSP-21xx Serial Interface

AD7891 to DSP5600x Serial Interface

Figure 10 shows a serial interface between the AD7891 and the DSP5600x series of DSPs. When reading from the AD7891, the DSP5600x should be set up for 16-bit data transfers, MSB first, normal mode synchronous operation, internally generated word frame sync, and gated clock. When writing to the AD7891, 8-bit or 16-bit data transfers can be used. The frame sync signal from the DSP5600x must be inverted before being applied to the $\overline{RFS}$ and $\overline{TFS}$ inputs of the AD7891, as shown in Figure 10.

To monitor the conversion time of the AD7891, a scheme such as those outlined in previous interfaces with $\overline{EOC}$ can be used. This can be implemented by connecting the $\overline{EOC}$ line directly to the $\overline{IRQA}$ input of the DSP5600x.

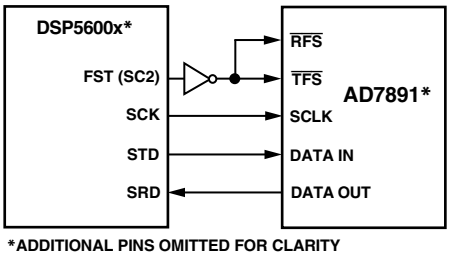


Figure 10. AD7891 to DSP5600x Serial Interface

AD7891 to TMS320xxx Serial Interface

The AD7891 can be interfaced to the serial port of TMS320xxx DSPs, as shown in Figure 11. External timing generation circuitry is necessary to generate the serial clock and syncs necessary for the interface.

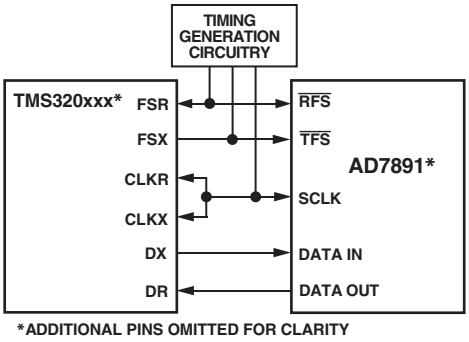


Figure 11. AD7891 to TMS320xxx Serial Interface

PARALLEL INTERFACING

The parallel port on the AD7891 allows the device to be interfaced to microprocessors or DSP processors as a memory mapped or I/O mapped device. The $\overline{CS}$ and $\overline{RD}$ inputs are common to all memory peripheral interfacing. Typical interfaces to different processors are shown in Figures 12 to 15. In all the interfaces shown, an external timer controls the $\overline{CONVST}$ input of the AD7891 and the $\overline{EOC}$ output interrupts the host DSP.

AD7891 to ADSP-21xx

Figure 12 shows the AD7891 interfaced to the ADSP-21xx series of DSPs as a memory mapped device. A single wait state may be necessary to interface the AD7891 to the ADSP-21xx depending on the clock speed of the DSP. This wait state can be programmed via the data memory wait state control register of the ADSP-21xx (please see the ADSP-2100 family Users Manual for details). The following instruction reads data from the AD7891.

MR = DM (ADC)

where *ADC* is the address of the AD7891.

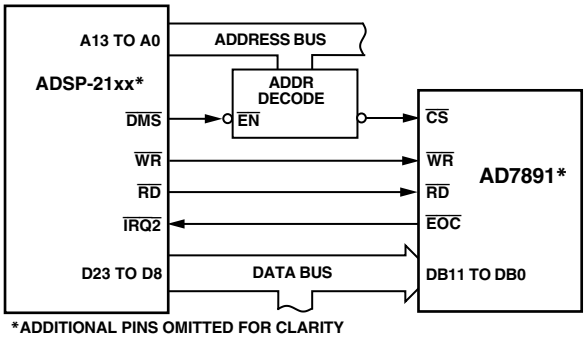


Figure 12. AD7891 to ADSP-21xx Parallel Interface

AD7891 to TMS32020, TMS320C25, and TMS320C5x

Parallel interfaces between the AD7891 and the TMS32020, TMS320C25, and TMS320C5x family of DSPs are shown in Figure 13. The memory mapped address chosen for the AD7891 should be chosen to fall in the I/O memory space of the DSPs.

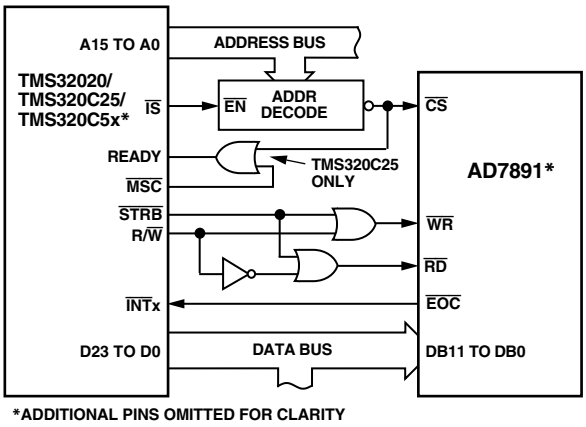


Figure 13. AD7891 to TMS32020/TMS320C25/TMS320C5x Parallel Interface

The parallel interface on the AD7891 is fast enough to interface to the TMS32020 with no extra wait states. If high speed glue logic, such as 74AS devices, are used to drive the $\overline{WR}$ and $\overline{RD}$ lines when interfacing to the TMS320C25, then again no wait states are necessary. However, if slower logic is used, data accesses may be slowed sufficiently when reading from and writing to the part to require the insertion of one wait state. In such a case, this wait state can be generated using the single OR gate to combine the $\overline{CS}$ and $\overline{MSC}$ signals to drive the READY line of the TMS320C25, as shown in Figure 13. Extra wait states are necessary when using the TMS320C5x at their fastest clock speeds. Wait states can be programmed via the IOWSR and CWSR registers (see the TMS320C5x User Guide for details).

Data is read from the ADC using the following instruction:

IN D, ADC

where *D* is the memory location where the data is to be stored, and *ADC* is the I/O address of the AD7891.

AD7891 to TMS320C3x

Figure 14 shows a parallel interface between the AD7891 and the TMS320C3x family of DSPs. The AD7891 is interfaced to the expansion bus of the TMS320C3x. A single wait state is required in this interface. This can be programmed using the WTCNT bits of the expansion bus control register (see the TMS320C3x Users Guide for details). Data from the AD7891 can be read using the following instruction:

LDI × ARn, Rx

where *ARn* is an auxiliary register containing the lower 16 bits of the address of the AD7891 in the TMS320C3x memory space, and *Rx* is the register into which the ADC data is loaded.

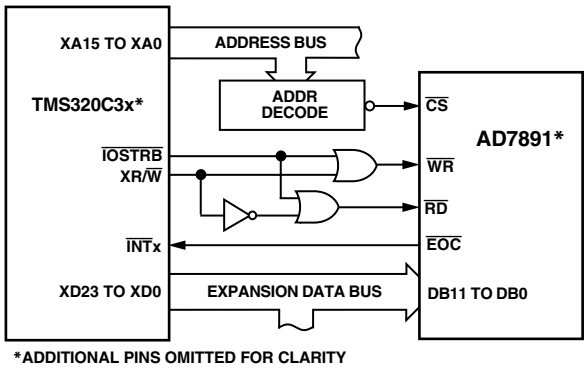


Figure 14. AD7891 to TMS320C3x Parallel Interface

AD7891 to DSP5600x

Figure 15 shows a parallel interface between the AD7891 and the DSP5600x series of DSPs. The AD7891 should be mapped into the top 64 locations of Y data memory. If extra wait states are needed in this interface, they can be programmed using the Port A Bus control register (see the DSP5600x Users Manual for details). Data can be read from the AD7891 using the following instruction:

MOVEO Y: ADC, X0

where *ADC* is the address in the DSP5600x address space to which the AD7891 has been mapped.

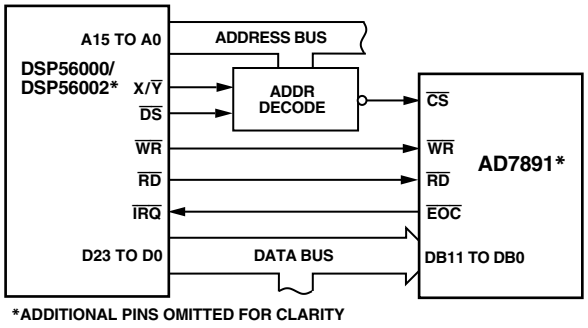


Figure 15. AD7891 to DSP5600x Parallel Interface

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the specified performance. The PCB on which the AD7891 is mounted should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined at only one place. If the AD7891 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7891. If the AD7891 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point established as close as possible to the AD7891.

Digital lines running under the device should be avoided because these couple noise onto the die. The analog ground plane should be allowed to run under the AD7891 to avoid noise coupling. The power supply lines of the AD7891 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best technique but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

The AD7891 should have ample supply bypassing located as close to the package as possible, ideally right up against the device. One of the V_{DD} pins (Pin 10 of the PLCC package and Pin 4 on the MQFP package) mainly drives the analog circuitry on the chip. This pin should be decoupled to the analog ground plane with a 10 μF tantalum bead capacitor in parallel with a 0.1 μF capacitor. The other V_{DD} pin (Pin 19 on the PLCC package and Pin 13 on the MQFP package) mainly drives digital circuitry on the chip. This pin should be decoupled to the digital ground plane with a 0.1 μF capacitor. The 0.1 μF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface mount types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching. Figure 16 shows the recommended decoupling scheme.

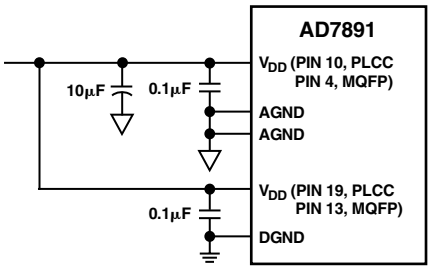


Figure 16. Recommended Decoupling Scheme for the AD7891

AD7891 PERFORMANCE

Linearity

The linearity of the AD7891 is primarily determined by the on-chip 12-bit DAC. This is a segmented DAC that is laser trimmed for 12-bit integral linearity and differential linearity. Typical INL for the AD7891 is ±0.25 LSB while typical DNL is ±0.5 LSB.

Noise

In an ADC, noise exhibits itself as code uncertainty in dc applications and as the noise floor (in an FFT for example) in ac applications. In a sampling ADC, such as the AD7891, all information about the analog input appears in the baseband from dc to half the sampling frequency. The input bandwidth of the track/hold amplifier exceeds the Nyquist bandwidth and, therefore, an antialiasing filter should be used to remove unwanted signals above $f_S/2$ in the input signal in applications where such signals exist.

Figure 17 shows a histogram plot for 16384 conversions of a dc input signal using the AD7891-1. The analog input was set at the center of a code transition in the following way. An initial dc input level was selected and a number of conversions were made. The resulting histogram was noted and the applied level was adjusted so that only two codes were generated with an equal number of occurrences. This indicated that the transition point between the two codes had been found. The voltage level at which this occurred was recorded. The other edge of one of these two codes was then found in a similar manner. The dc level for the center of code could then be calculated as the average of the two transition levels. The AD7891-1 inputs were configured for the ±5 V input range and the data was read from the part in parallel mode after conversion. Similar results have been found with the AD7891-1 on the ±10 V range and on all input ranges of the AD7891-2. The same performance is achieved in serial mode, again with the data read from the AD7891-1 after conversion. All the codes, except for 3, appear in one output bin, indicating excellent noise performance from the ADC.

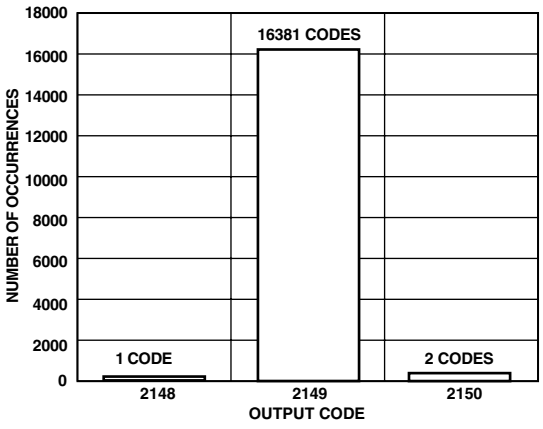


Figure 17. Typical Histogram Plot (AD7891-1)

Dynamic Performance

The AD7891 contains an on-chip track/hold amplifier, allowing the part to sample input signals of up to 250 kHz on any of its input channels. Many of the AD7891's applications require it to sequence through low frequency input signals across its eight channels. There may be some applications, however, for which the dynamic performance of the converter on signals of up to 250 kHz input frequency is of interest. It is recommended for these wider bandwidth signals that the hardware conversion start method of sampling is used.

These applications require information on the spectral content of the input signal. Signal-to-(noise + distortion), total harmonic distortion, peak harmonic or spurious tone, and intermodulation distortion are all specified. Figure 18 shows a typical FFT plot of a 10 kHz, ±10 V input after being digitized by the AD7891-1 operating at 500 kHz, with the input connected for ±10 V operation. The signal-to-(noise + distortion) ratio is 72.2 dB and the total harmonic distortion is –87 dB. Figure 19 shows a typical FFT plot of a 100 kHz, 0 V to 5 V input after being digitized by the AD7891-2 operating at 500 kHz, with the input connected for 0 V to 5 V operation. The signal-to-(noise + distortion) ratio is 71.17 dB and the total harmonic distortion is –82.3 dB. It should be noted that reading from the part during conversion does have a significant impact on dynamic performance. Therefore, for sampling applications, it is recommended not to read during conversion.

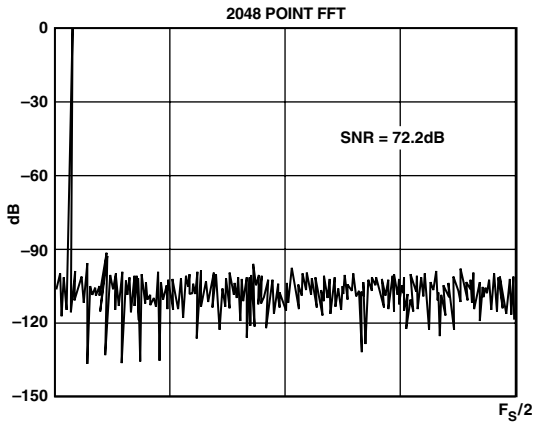


Figure 18. Typical AD7891-1 FFT Plot

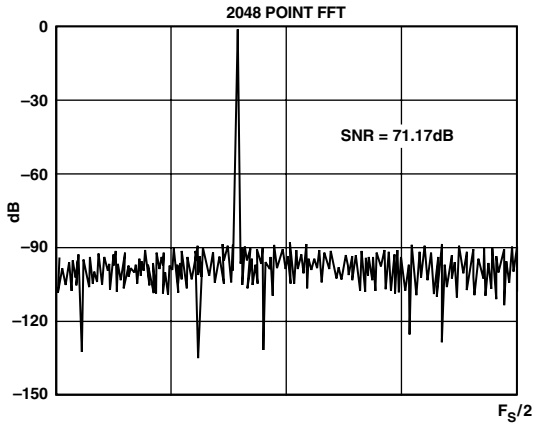


Figure 19. Typical AD7891-2 FFT Plot

Effective Number of Bits

The formula for signal-to-(noise + distortion) ratio (see Terminology section) is related to the resolution or number of bits of the converter. Rewriting the formula gives a measure of performance expressed in effective number of bits (ENOB).

$$ENOB = \left(SNR - 1.76\right) / 6.02$$

where *SNR* is the signal-to-(noise + distortion) ratio.

The effective number of bits for a device can be calculated from its measured SNR. Figure 20 shows a typical plot of effective number of bits versus frequency for the AD7891-1 and the AD7891-2 from dc to 200 kHz. The sampling frequency is 500 kHz. The AD7891-1 inputs were configured for ±10 V operation. The AD7891-2 inputs were configured for 0 to 5 V operation. The AD7891-1 plot only goes to 100 kHz as a ±10 V sine wave of sufficient quality was unavailable at higher frequencies.

Figure 20 shows that the AD7891-1 converts an input sine wave of 100 kHz to an effective number of bits of 11 which equates to a signal-to-(noise + distortion) level of 68.02 dBs. The AD7891-2 converts an input sine wave of 200 kHz to an effective number of bits of 11.07, which equates to a signal-to-(noise + distortion) level of 68.4 dBs.

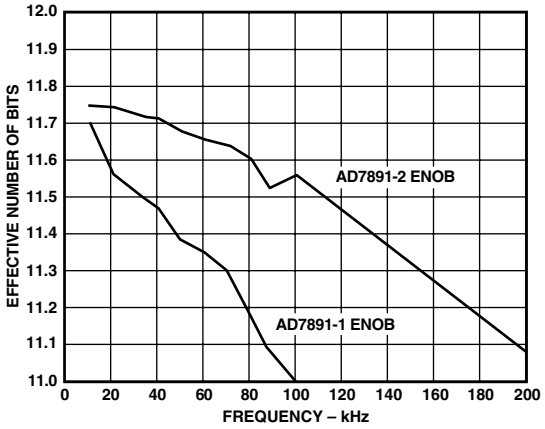
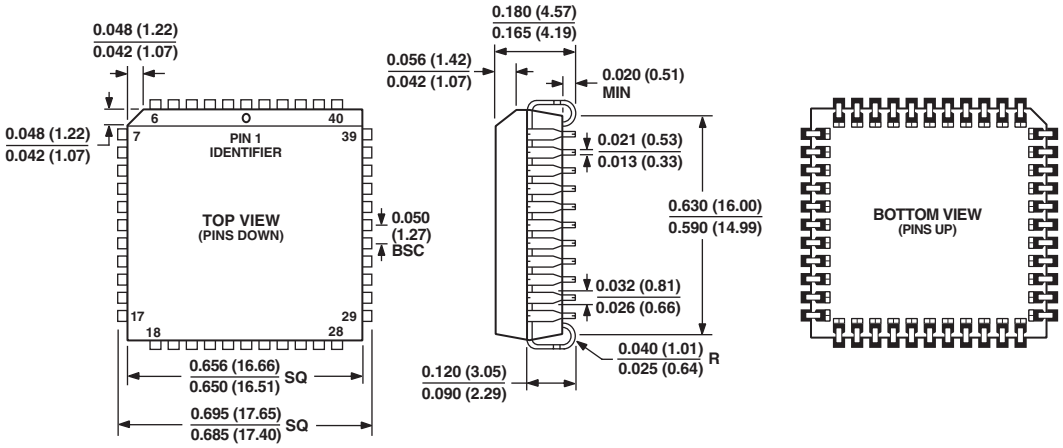


Figure 20. Effective Number of Bits vs. Frequency

OUTLINE DIMENSIONS

44-Lead Plastic Leaded Chip Carrier [PLCC]
(P-44A)

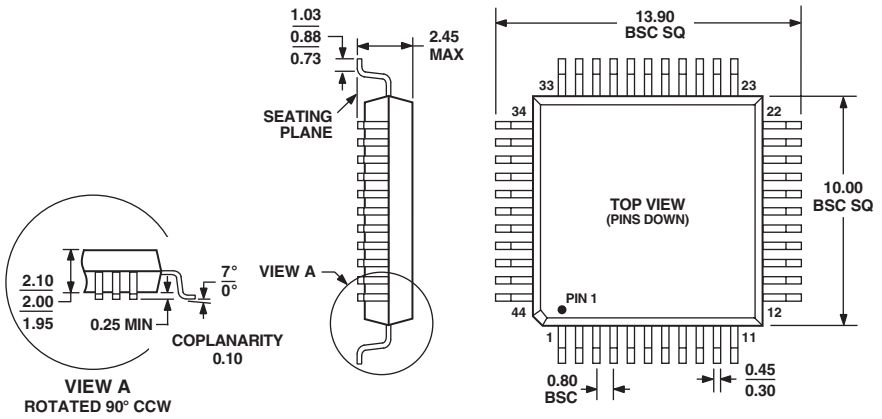
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

OUTLINE DIMENSIONS

44-Lead Metric Quad Flat Package [MQFP]
(S-44-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-112-AA-1

C01358–0–4/04(D)

Revision History

Location	Page

4/04—Data Sheet changed from REV. C to REV. D.

Changes to SPECIFICATIONS . . . 2
Changes to ORDERING GUIDE . . . 5
Changes to PIN FUNCTION DESCRIPTIONS . . . 6
Changes to PARALLEL INTERFACE MODE FUNCTIONS . . . 7
Changes to SERIAL INTERFACE MODE FUNCTIONS . . . 8
Changes to CONTROL REGISTER . . . 8
Changes to AD7891 to 8X51 Serial Interface section . . . 14
Changes to Figure 10 . . . 15
Changes to Figure 11 . . . 15
Changes to Power Supply Bypassing and Grounding . . . 17
Changes to Figure 16 . . . 17
Updated OUTLINE DIMENSIONS . . . 20

01/02—Data Sheet changed from REV. B to REV. C.

Changed page 7 to page 6 and moved page 6 to page 9 to keep Pin Configurations together with Pin Function descriptions.

Edits to CONTROL REGISTER . . . 9
Text added to CONVERTER DETAILS . . . 10
Edits to Figure 2 . . . 10

02/01—Data Sheet changed from REV. A to REV. B.

PQFP designation changed to MQFP throughout.

Edit to FEATURES, Single Supply Low Power Operation . . . 1
Edits to mW (90 to 82) in last paragraph of left hand column . . . 1
Edits to POWER REQUIREMENTS section of Specifications table . . . 3