MAX11154

18-Bit, 500ksps, 0 to 5V SAR ADC with Internal Reference in TDFN

General Description

The MAX11154 18-bit, 500ksps, SAR ADC offers excellent AC and DC performance with unipolar input range, small size, and internal reference. The MAX11154 integrates an optional internal reference and buffer, saving additional cost and space.

This ADC typically achieves 93.8dB SNR and -105.8dB THD. The device guarantees 18-bit no-missing codes and ±2 LSB INL (typ).

The MAX11154 communicates using an SPI-compatible serial interface at 2.3V, 3V, 3.3V, or 5V logic. The serial interface can be used to daisy-chain multiple ADCs for multichannel applications and provides a busy indicator option for simplified system synchronization and timing.

The MAX11154 is offered in a 12-pin, 3mm x 3mm, TDFN package and is specified over the -40°C to +85°C temperature range.

Applications

- Data Acquisition Systems
- Industrial Control Systems/Process Control
- Medical Instrumentation
- Automatic Test Equipment

***Selector Guide* and *Ordering Information* appear at end of data sheet.**

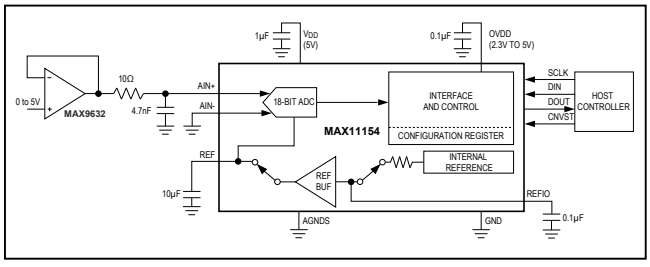
Benefits and Features

- High DC/AC Accuracy Improves Measurement Quality
  - 18-Bit Resolution with No Missing Codes
  - 500ksps Throughput Rates without Pipeline Delay/Latency
  - 93.8dB SNR and -105.8dB THD at 10kHz
  - 1.7 LSB_{RMS} Transition Noise
  - ±0.6 LSB DNL (typ) and ±2 LSB INL (typ)
- Highly Integrated ADC Saves Cost and Space
  - ±7ppm/°C Internal Reference
  - Internal Reference Buffer
- Wide Supply Range and Low Power Simplify Power-Supply Design
  - 5V Analog Supply
  - 2.3V to 5V Digital Supply
  - 23.6mW Power Consumption with External Reference at 500ksps
  - 10µA in Shutdown Mode
- Multi-Industry Standard Serial Interface and Small Package Reduce Size
  - SPI/QSPI™/MICROWIRE®/DSP-Compatible Serial Interface
  - 3mm x 3mm Tiny 12-Pin TDFN Package

QSPI is a trademark of Motorola, Inc.

MICROWIRE is a registered trademark of National Semiconductor Corporation.

Typical Operating Circuit



14-Bit to 18-Bit SAR ADC Family

	14-BIT 500ksps	16-BIT 250ksps	16-BIT 500ksps	18-BIT 500ksps
±5V Input Internal Reference	—	MAX11167 MAX11169	MAX11166 MAX11168	MAX11156 MAX11158
0 to 5V Input Internal Reference	—	MAX11161 MAX11165	MAX11160 MAX11164	MAX11150 MAX11154
0 to 5V Input External Reference	MAX11262	MAX11163	MAX11162	MAX11152

maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
OVDD to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
AIN+ to GND .....-0.3V to +6V
AIN-, REF, REFIO, AGNDS
to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
SCLK, DIN, DOUT, CNVST
to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 18.2mW/°C above +70°C).....1349mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....59.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....22.5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT (Note 3)						
Input Voltage Range		AIN+ to AIN-, K = 5.0/4.096	0		+K x V_{REF}	V
Absolute Input Voltage Range		AIN+ to GND	-0.1		+(V_{DD} + 0.1)	V
		AIN- to GND	-0.1		+0.1	
Input Leakage Current		Acquisition phase	-10	+0.001	+10	µA
Input Capacitance				32		pF
Input-Clamp Protection Current		Both inputs	-20		+20	mA
STATIC PERFORMANCE (Note 4)						
Resolution	N		18			Bits
No Missing Codes			18			Bits
Offset Error			-15.5	±1.45	+15.5	LSB
Offset Error Temperature Coefficient				±0.01		LSB/°C
Gain Error			-15	±4.3	+15	LSB
Gain Error Temperature Coefficient				±0.016		LSB/°C
Integral Nonlinearity	INL		-6	±2	+6	LSB
Differential Nonlinearity	DNL	Guaranteed by design	-1	±0.6	+1	LSB
Positive Full-Scale Error			-22		+22	LSB
Analog Input CMRR	CMRR			-7.86		LSB/V

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection (Note 5)	PSR			-23.5		LSB/V
Transition Noise				1.7		LSB_{RMS}
REFERENCE (Note 7)						
REF Output Initial Accuracy	V_{REF}	Reference mode 0	4.092	4.096	4.100	V
REF Output Temperature Coefficient	T_{CREF}	Reference mode 0	-17	±9	+17	ppm/°C
REFIO Output Initial Accuracy	V_{REFIO}	Reference modes 0 and 2	4.092	4.096	4.100	V
REFIO Output Temperature Coefficient	TC_{REFIO}	Reference modes 0 and 2	-15	±7	+15	ppm/°C
REFIO Output Impedance		Reference modes 0 and 2		10		kΩ
REFIO Input Voltage Range		Reference mode 1	3	4.096	4.25	V
Reference Buffer Initial Offset		Reference mode 0 and 1	-500		+500	µV
Reference Buffer Offset Drift		Reference mode 0 and 1	-12	±6	+12	µV/°C
External Compensation Capacitor	C_{EXT}	Required for reference modes 0 and 1, recommended for reference modes 2 and 3	10			µF
REF Voltage Input Range	V_{REF}	Reference modes 2 and 3	2.5		4.25	V
REF Input Capacitance		Reference modes 2 and 3		20		pF
REF Load Current	I_{REF}	V_{REF} = 4.096V, reference modes 2 and 3		137		µA
DYNAMIC PERFORMANCE (Note 6)						
Signal-to-Noise Ratio	SNR	V_{REF} = 4.096V, reference mode 3	91.7	93.8		dB
		V_{REF} = 4.096V, reference mode 1		93.5		
		V_{REF} = 2.5V, reference mode 3		89.9		
		Internal reference, reference mode 0		93.4		
Signal-to-Noise Plus Distortion	SINAD	V_{REF} = 4.096V, reference mode 3	91.0	93.13		dB
		V_{REF} = 4.096V, reference mode 1		93.3		
		V_{REF} = 2.5V, reference mode 3		89.6		
		Internal reference, reference mode 0		93.0		
Spurious-Free Dynamic Range	SFDR		97.7	108		dB
Total Harmonic Distortion	THD			-105.8	-96	dB
Intermodulation Distortion (Note 8)	IMD			-119.4		dBFS
SAMPLING DYNAMICS						
Throughput Sample Rate					500	ksps
Transient Response		Full-scale step			400	ns
Full-Power Bandwidth		-3dB point		6		MHz
		-0.1dB point		> 0.2		
Aperture Delay				2.5		ns
Aperture Jitter				50		ps_{RMS}

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	V_{DD}		4.75		5.25	V
Interface Supply Voltage	V_{OVDD}		2.3		5.25	V
Analog Supply Current	I_{VDD}	Reference modes 0 and 1	4.5	5.7	6.75	mA
		Reference modes 2 and 3	2.9	3.2	3.5	
V_{DD} Shutdown Current				0.01	10	µA
Interface Supply Current (Note 9)	I_{OVDD}	V_{OVDD} = 2.3V		1.6	2.2	mA
		V_{OVDD} = 5.25V			5.5	
OVDD Shutdown Current				0.2	10	µA
Power Dissipation		V_{DD} = 5V, V_{OVDD} = 3.3V, reference mode = 2, 3		23.6		mW
		V_{DD} = 5V, V_{OVDD} = 3.3V, reference mode = 0, 1		35.7		
DIGITAL INPUTS (DIN, SCLK, CNVST)						
Input Voltage High	V_{IH}		0.7 x V_{OVDD}			V
Input Voltage Low	V_{IL}				0.3 x V_{OVDD}	V
Input Hysteresis	V_{HYS}			±0.05 x V_{OVDD}		V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	V_{IN} = 0V or V_{OVDD}	-10		+10	µA
DIGITAL OUTPUT (D_{OUT})						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Three-State Leakage Current			-10		+10	µA
Three-State Output Capacitance				15		pF
TIMING (Note 9)						
Time Between Conversions	t_{CYC}		2			µs
Conversion Time	t_{CONV}	CNVST rising to data available	1.35		1.5	µs
Acquisition Time	t_{ACQ}	t_{ACQ} = t_{CYC} - t_{CONV}	0.5			µs
CNVST Pulse Width	t_{CNVPW}	$\overline{CS}$ mode	5			ns

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

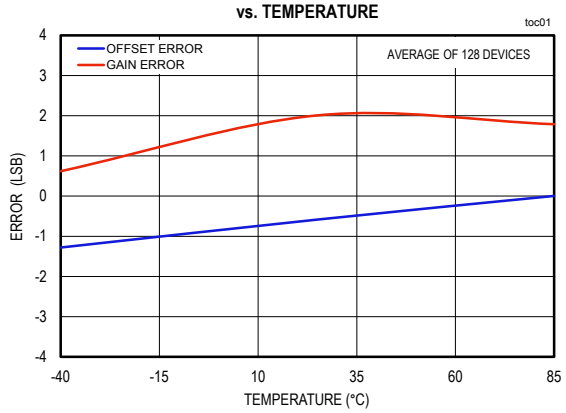
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Period ($\overline{CS}$ Mode)	t_{SCLK}	V_{OVDD} > 4.5V	14			ns
		V_{OVDD} > 2.7V	20			
		V_{OVDD} > 2.3V	26			
SCLK Period (Daisy-Chain Mode)	t_{SCLK}	V_{OVDD} > 4.5V	16			ns
		V_{OVDD} > 2.7V	24			
		V_{OVDD} > 2.3V	30			
SCLK Low Time	t_{SCLKL}		5			ns
SCLK High Time	t_{SCLKH}		5			ns
SCLK Falling-Edge to Data Valid Delay	t_{DDO}	V_{OVDD} > 4.5V			12	ns
		V_{OVDD} > 2.7V			18	
		V_{OVDD} > 2.3V			23	
CNVST Low to D_{OUT} D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}	V_{OVDD} > 2.7V			14	ns
		V_{OVDD} < 2.7V			17	
CNVST High or Last SCLK Falling Edge to D_{OUT} High Impedance	t_{DIS}	$\overline{CS}$ Mode			20	ns
DIN Valid Setup Time from SCLK Falling Edge	$t_{SDINSCK}$	V_{OVDD} > 4.5V	3			ns
		V_{OVDD} > 2.7V	5			
		V_{OVDD} > 2.3V	6			
DIN Valid Hold Time from SCLK Falling Edge	$t_{HDINSCK}$		0			ns
SCLK Valid Setup Time to CNVST Falling Edge	$t_{SSCKCNF}$		3			ns
SCLK Valid Hold Time to CNVST Falling Edge	$t_{HSCKCNF}$		6			ns

Note 2: Maximum and minimum limits are fully production tested over specified supply voltage range and at a temperature of +25°C. Limits over the operating temperature range are guaranteed by design and device characterization.
Note 3: See the *Analog Inputs* and *Overvoltage Input Clamps* sections.
Note 4: Static Performance limits are guaranteed by design and device characterization. For definitions, see the *Definitions* section.
Note 5: Defined as the change in positive full-scale code transition caused by a ±5% variation in the V_{DD} supply voltage.
Note 6: 10kHz sine wave input, -0.1dB below full scale.
Note 7: See Table 4 for definition of the reference modes.
Note 8: f_{IN1} ~ 9.4kHz, f_{IN2} ~ 10.7kHz, Each tone at -6.1dB below full scale.
Note 9: C_{LOAD} = 65pF on DOUT.

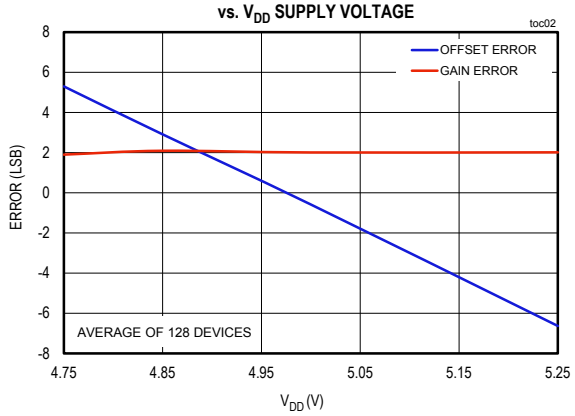
Typical Operating Characteristics

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = +25°C, unless otherwise noted.)

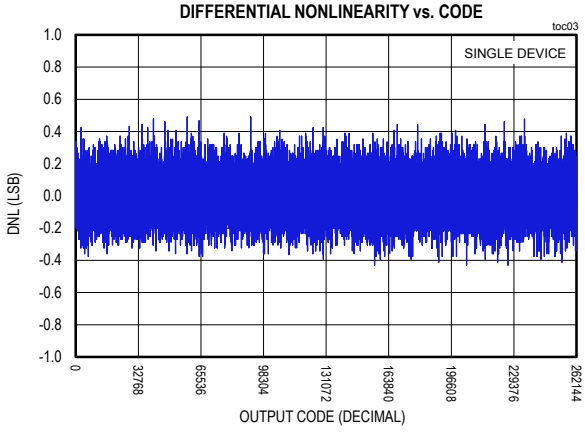
OFFSET AND GAIN ERROR vs. TEMPERATURE



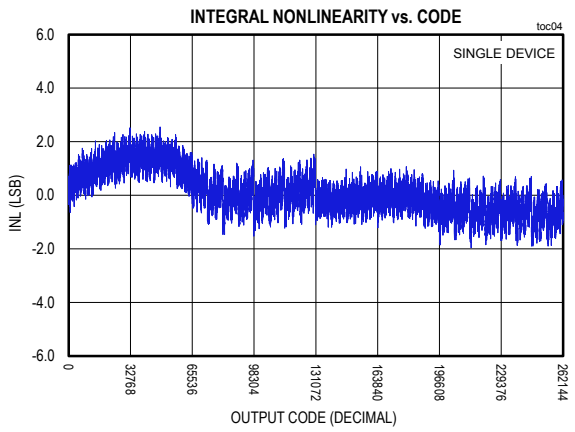
OFFSET AND GAIN ERROR vs. V_{DD} SUPPLY VOLTAGE



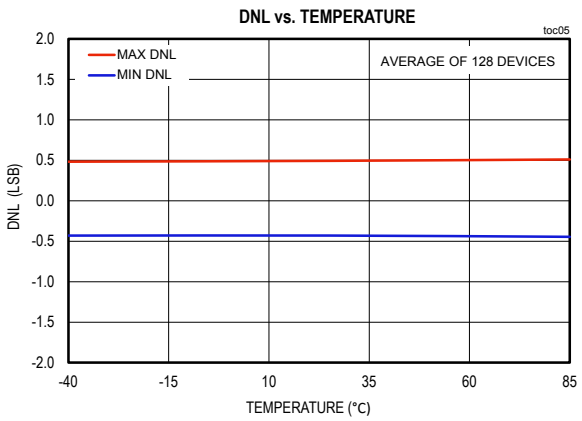
DIFFERENTIAL NONLINEARITY vs. CODE



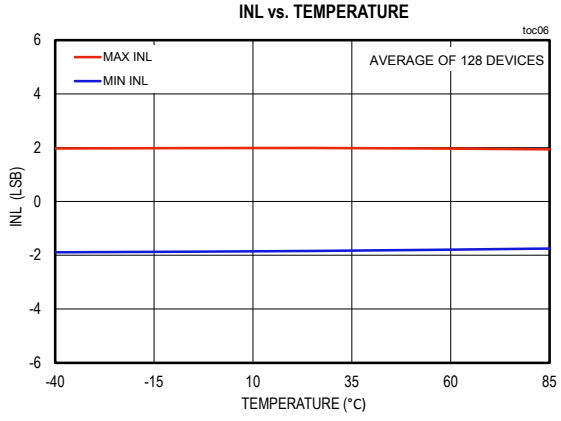
INTEGRAL NONLINEARITY vs. CODE



DNL vs. TEMPERATURE



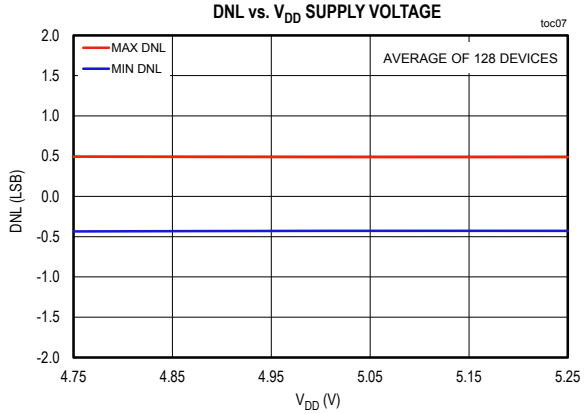
INL vs. TEMPERATURE



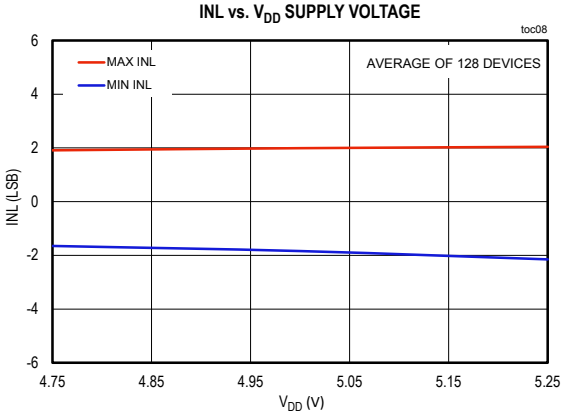
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = +25°C, unless otherwise noted.)

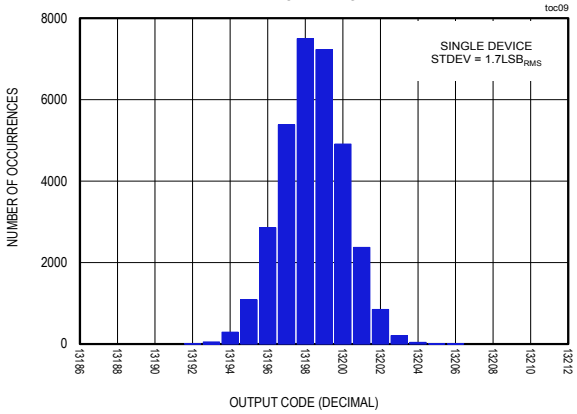
DNL vs. V_{DD} SUPPLY VOLTAGE



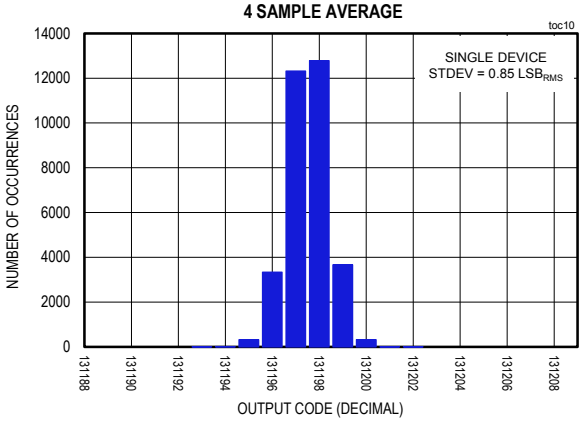
INL vs. V_{DD} SUPPLY VOLTAGE



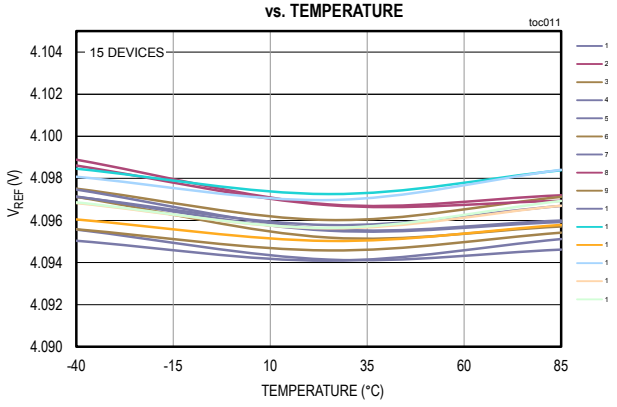
OUTPUT NOISE HISTOGRAM NO AVERAGE



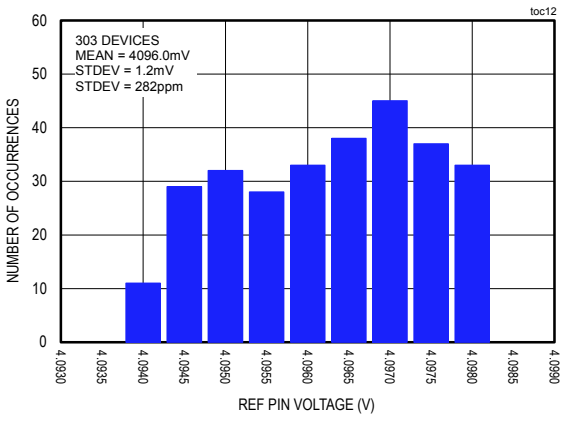
OUTPUT NOISE HISTOGRAM WITH 4 SAMPLE AVERAGE



INTERNAL REFERENCE VOLTAGE (REF PIN) vs. TEMPERATURE



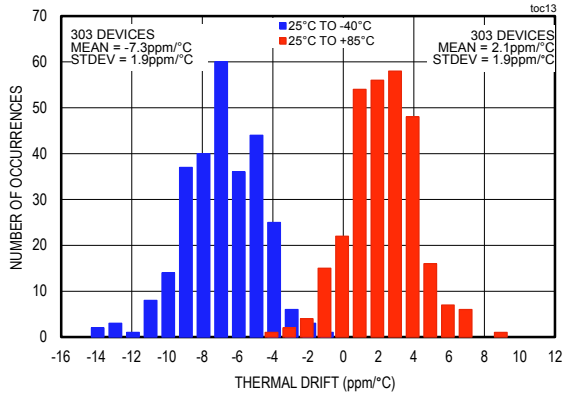
INITIAL ERROR VOLTAGE ON REF PIN



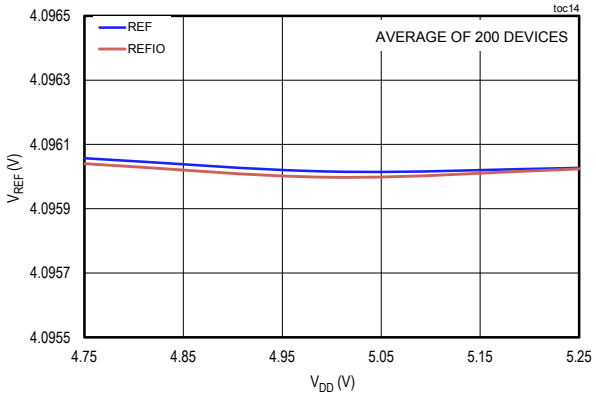
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = +25°C, unless otherwise noted.)

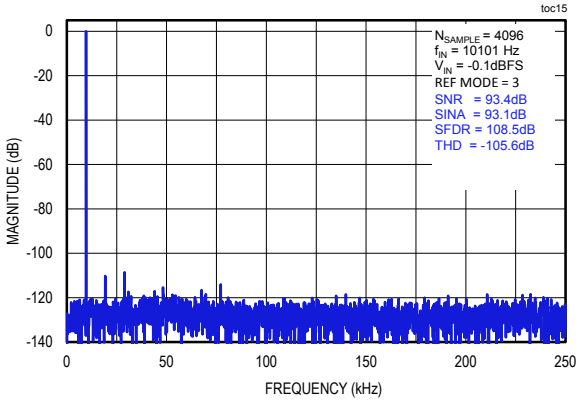
REF PIN THERMAL DRIFT SLOPE



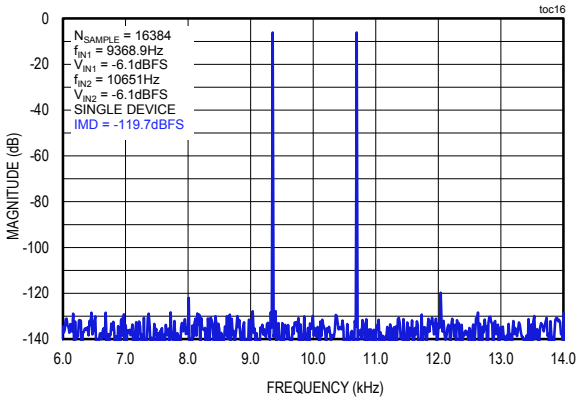
INTERNAL REFERENCE VOLTAGES vs. V_{DD} VOLTAGE



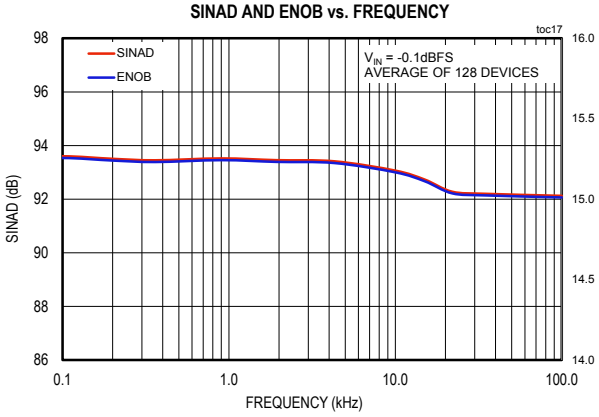
FFT PLOT



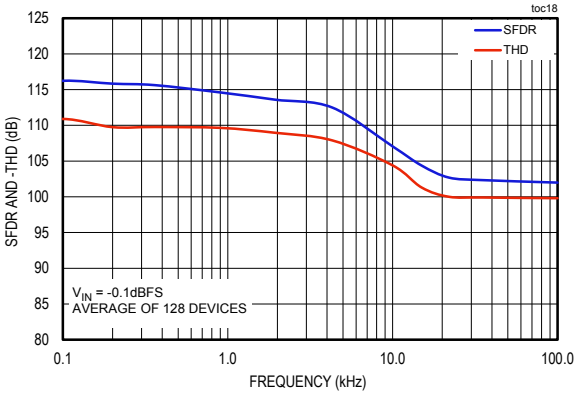
TWO TONES IMD



SINAD AND ENOB vs. FREQUENCY



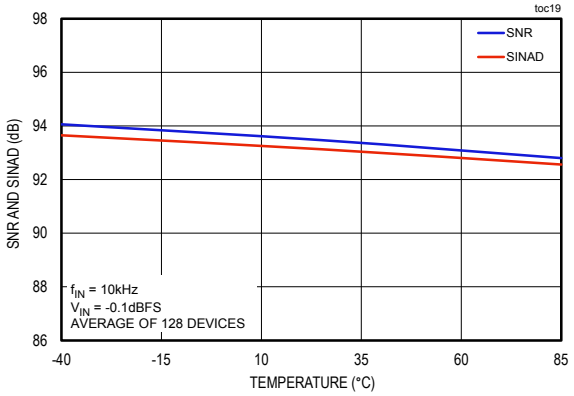
SFDR and -THD vs. FREQUENCY



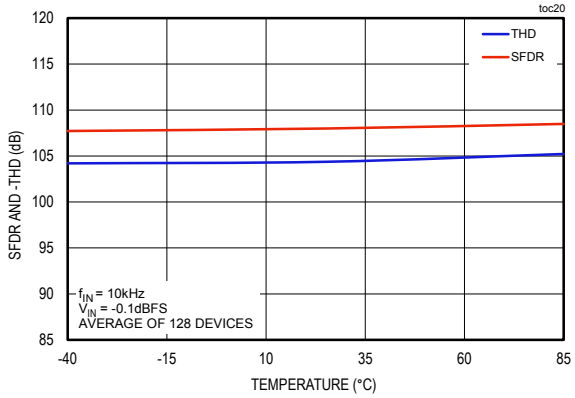
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = +25°C, unless otherwise noted.)

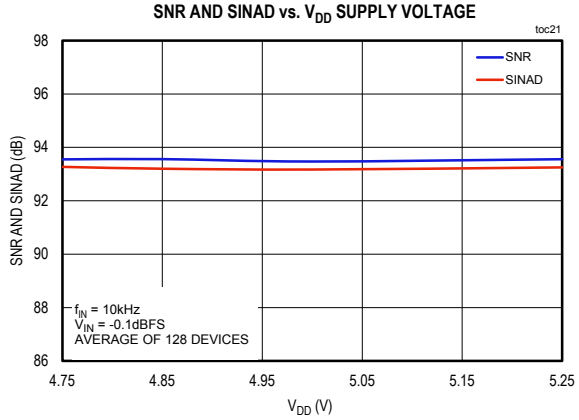
SNR AND SINAD vs. TEMPERATURE



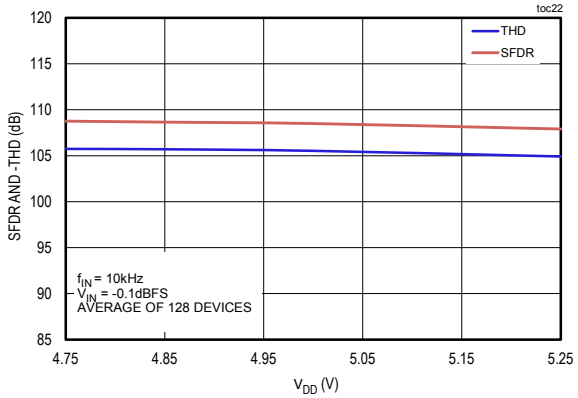
SFDR AND THD vs. TEMPERATURE



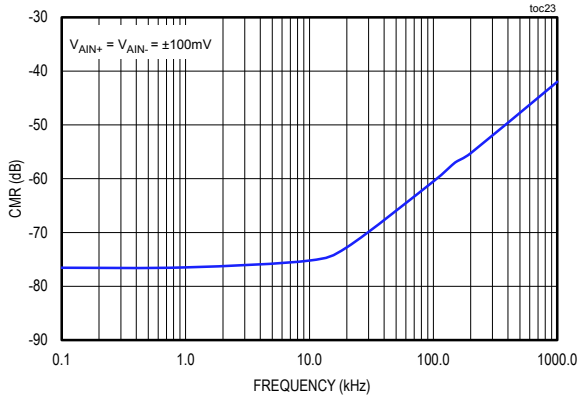
SNR AND SINAD vs. V_{DD} SUPPLY VOLTAGE



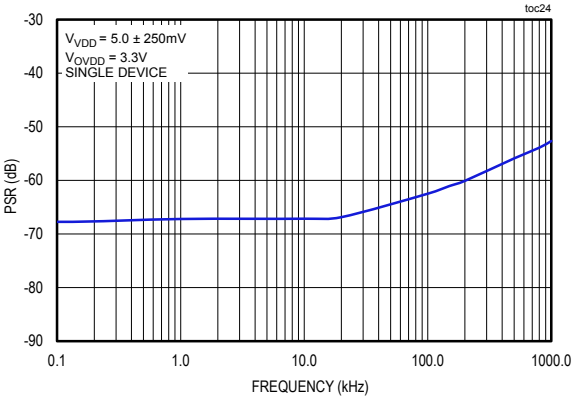
THD AND SFDR vs. V_{DD} SUPPLY VOLTAGE



CMR vs. INPUT FREQUENCY



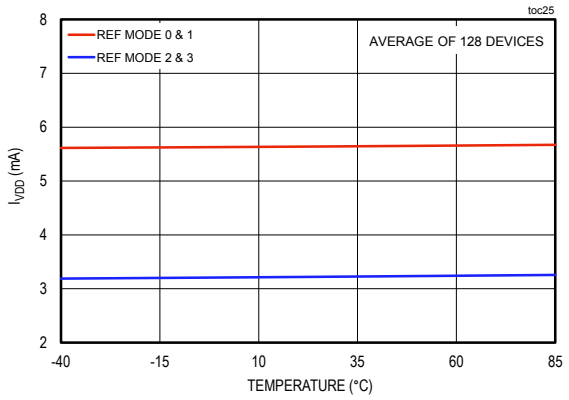
PSR vs. V_{DD} SUPPLY FREQUENCY



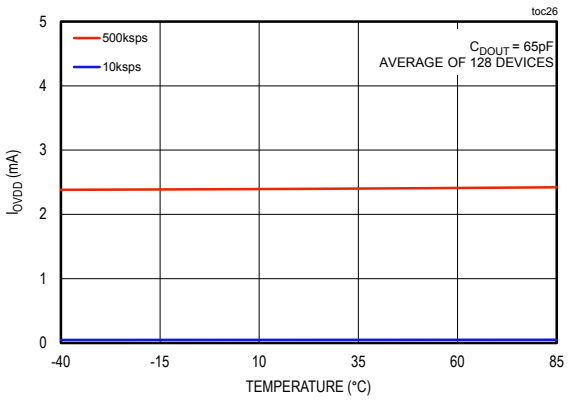
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500ksps, Reference Mode 3, V_{REF} = 4.096V; T_A = +25°C, unless otherwise noted.)

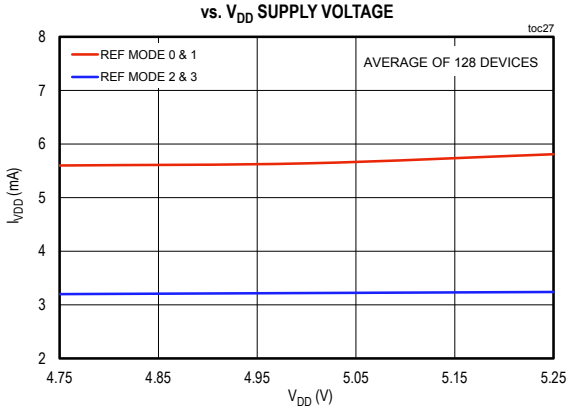
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



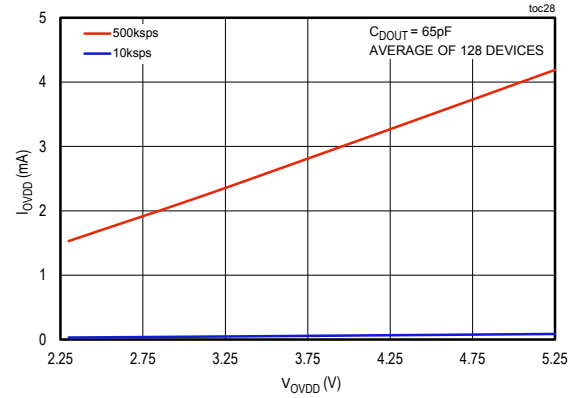
OVDD SUPPLY CURRENT vs. TEMPERATURE



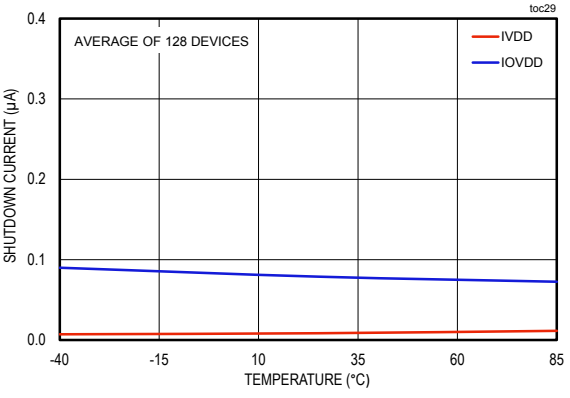
V_{DD} SUPPLY CURRENT vs. V_{DD} SUPPLY VOLTAGE



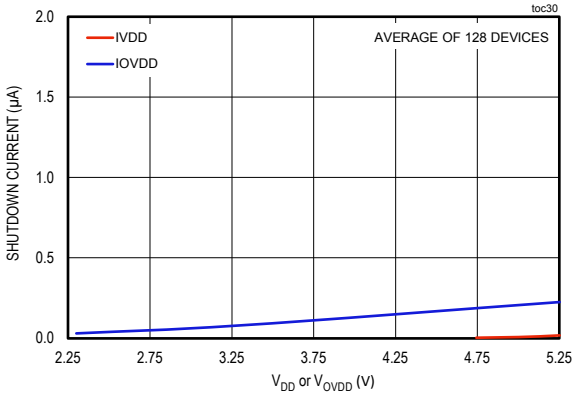
OVDD SUPPLY CURRENT vs. OVDD SUPPLY VOLTAGE



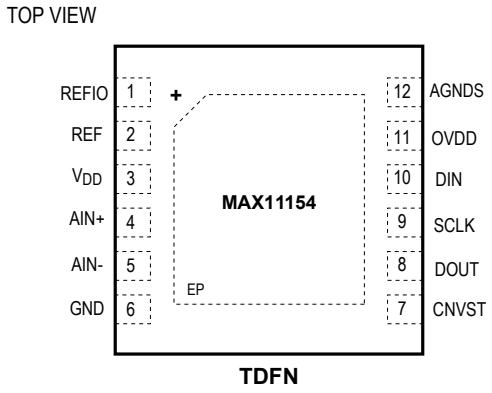
V_{DD} AND OVDD SHUTDOWN CURRENT vs. TEMPERATURE



V_{DD} AND OVDD SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



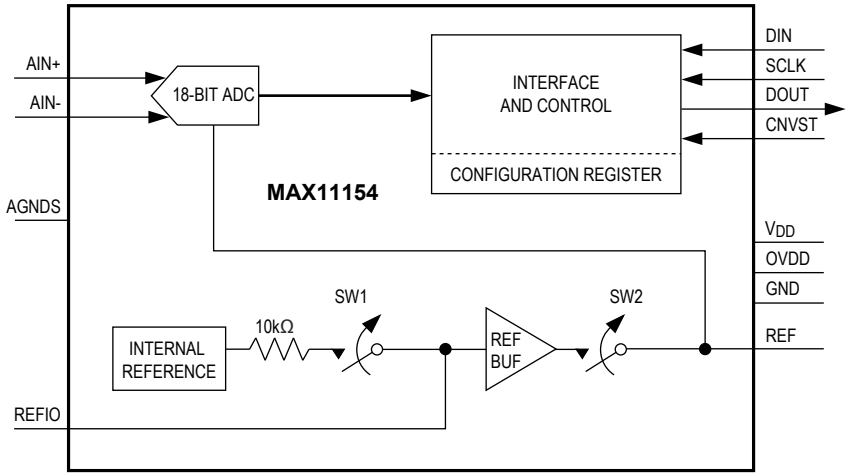
Pin Configuration



Pin Description

PIN	NAME	I/O	FUNCTION
1	REFIO	I/O	External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGNDS.
2	REF	I/O	External Reference Input/Reference Buffer Decoupling. Bypass to AGNDS in close proximity with a X5R or X7R 10µF 16V capacitor. See the *Layout*, *Grounding*, and *Bypassing* section.
3	V_{DD}	I	Analog Power Supply. Bypass to GND with a 0.1µF capacitor for each device and one 10µF capacitor per PCB.
4	AIN+	I	Positive Analog Input
5	AIN-	I	Negative Analog Input. Connect AIN- to the analog ground plane or to a remote-sense ground.
6	GND	I	Power-Supply Ground
7	CNVST	I	Convert Start Input. The rising edge of CNVST initiates conversions. The falling edge of CNVST with SCLK high enables the serial interface.
8	DOUT	O	Serial Data Output. DOUT will change state on the falling edge of SCLK.
9	SCLK	I	Serial Clock Input. Clocks data out of the serial interface when the device is selected.
10	DIN	I	Serial Data Input. DIN data is latched into the serial interface on the rising edge of SCLK.
11	OVDD	I	Digital Power Supply. Bypass to GND with a 0.1µF capacitor for each device and one 10µF capacitor per PCB.
12	AGNDS	I	Analog Ground Sense. Zero current reference for the on-board DAC and reference source. Reference for REFIO and REF.
—	EP	—	Exposed Pad. Connect to PCB GND.

Functional Diagram



CONFIGURATION REGISTER		REFERENCE MODE	REFERENCE SWITCH STATE	
B5	B4		SW2	SW1
0	0	0	CLOSED	CLOSED
0	1	1	CLOSED	OPEN
1	0	2	OPEN	CLOSED
1	1	3	OPEN	OPEN

Detailed Description

The MAX11154 is a 18-bit single-channel, pseudo-differential ADC with maximum throughput rates of 500ksps. This ADC includes a precision internal reference that allows for measuring an input voltage interval from 0 to 5V. Input ranges of 0 to 3.05V and 0 to 5.19V can be obtained by applying external reference. Both inputs (AIN+ and AIN-) are sampled with a pseudo-differential on-chip track-and-hold.

The MAX11154 inputs are protected for up to ±20mA of overrange current. This ADC is powered from a 4.75V to 5.25V analog supply (V_{DD}) and a separate 2.3V to 5.25V digital supply (OVDD). The MAX11154 requires 500ns to acquire the input sample on an internal track-and-hold and then convert the sampled signal to 18 bits of accuracy using an internally clocked converter.

Analog Inputs

The MAX11154 ADC consists of a true sampling pseudo-differential input stage with high-impedance, capacitive inputs. The internal T/H circuitry feature a small-signal bandwidth of about 6MHz to provide 18-bit accurate sampling in 500ns. This allows for accurate sampling of a number of scanned channels through an external multiplexer.

The MAX11154 can thus convert input signals on AIN+ in the range of 0V to +(K x V_{REF} + AIN-) where K = 5.000/4.096. AIN+ should also be limited to -0.1V to (V_{DD} + 0.1V) for accurate conversions. AIN- has an input range of -0.1V to +0.1V and should be connected to the ground reference of the input signal source. The MAX11154 performs a true differential sampling on inputs between AIN+ and AIN- with good common-mode rejection (see the *Typical Operating Circuit*). This allows for improved sampling of remote transducer inputs.

Overvoltage Input Clamps

The MAX11154 includes an input clamping circuit that activates when the input voltage at AIN+ is above (V_{DD} + 300mV) or below -300mV. The clamp circuit remains high impedance while the input signal is within the range of -100mV to (V_{DD} + 100mV) and draws little to no current. However, when the input signal exceeds this range the clamps begin to turn on. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed the range of -100mV to (V_{DD} + 100mV).

To make use of the input clamps, connect a resistor (R_S) between the AIN+ input and the voltage source to limit the voltage at the analog input and to ensure the fault current into the devices does not exceed ±20mA. Note that the voltage at the AIN+ input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of R_S:

$$R_S = \frac{V_{FAULT\,MAX} - 7V}{20mA}$$

where $V_{FAULTMAX}$ is the maximum voltage that the source produces during a fault condition.

Figure 1 and Figure 2 illustrate the clamp circuit voltage current characteristics for a source impedance R_S = 1170Ω. While the input voltage is within the -300mV to (V_{DD} + 300mV) range, no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

Internal/External Reference (REFIO) Configuration

The MAX11154 includes a standard SPI interface that selects internal or external reference modes of operation through an input configuration register (see the *Input Configuration Interface* section). The MAX11154 features an internal bandgap reference circuit (V_{REFIO} = 4.096V) that is buffered with an internal reference buffer that drives the REF pin. The MAX11154 configurations register allows four combinations of reference configuration. These reference mode are:

Reference Mode 00: ADC reference is provided by the internal bandgap feed out the REFIO pin, noise filtered with an external capacitor on the REFIO pin, then buffered by the internal reference buffer and decoupled with an external capacitor on the REF pin. In this mode, the ADC requires no external reference source.

Reference Mode 01: ADC reference is provided externally and feeds into the REFIO pin, buffered with the internal reference buffer and decoupled with an external capacitor on the REF pin. This mode is typically used when a common reference source is needed for more than one MAX11154.

Reference Mode 10: The internal bandgap is used as a reference source output and feed out the REFIO pin. However, the internal reference buffer is in a shutdown state and the REF pin is high impedance. This state would typically be used to provide a common reference source to a set of external reference buffers for several MAX11154.

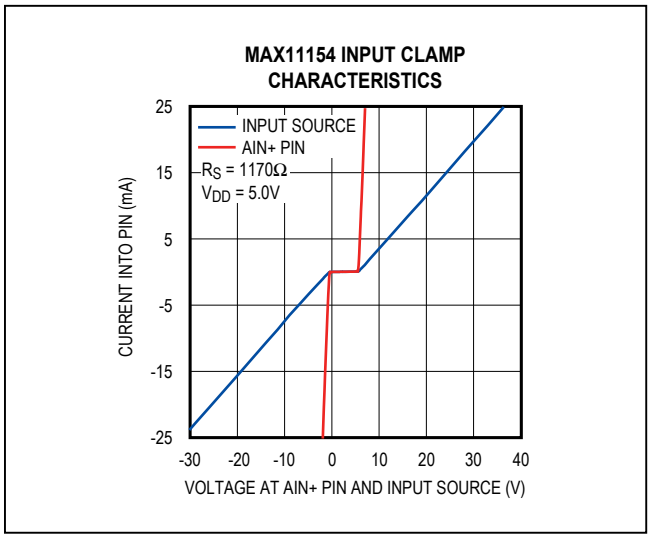


Figure 1. Input Clamp Characteristics

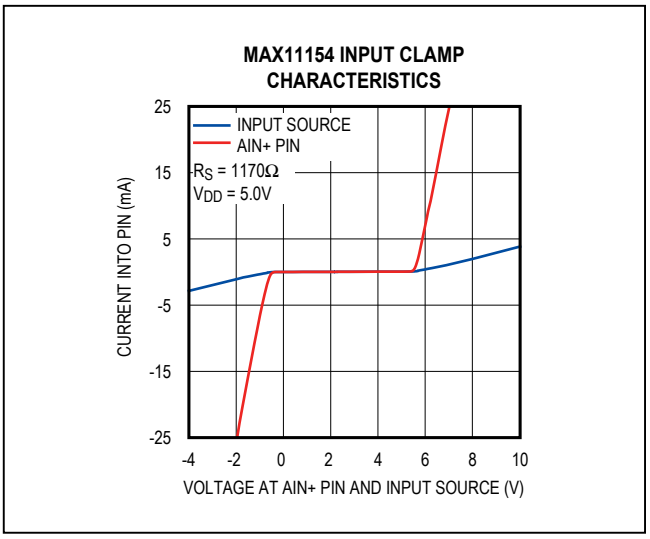


Figure 2. Input Clamp Characteristics (Zoom In)

Reference Mode 11: The internal bandgap reference source as well as the internal reference buffer are both in a shutdown state. The REF pin is in a high-impedance state. This mode would typically be used when an external reference source and external reference buffer is used to drive all MAX11154 parts in a system.

Regardless of the reference mode used, the MAX11154 requires a low-impedance reference source on the REF pin to support 18-bit accuracy. When using the internal reference buffer, externally bypass the reference buffer output using at least a 10µF, low-inductance, low-ESR capacitor placed as close as possible to the REF pin, thus minimizing additional PCB inductance. When using the internal bandgap reference source, bypass the REFIO pin with a 0.1µF capacitor to ground. If providing an external reference and using the internal reference buffer, drive the REFIO pin directly with an external reference source in the range of 3.0V to 4.25V. Finally, if disabling the MAX11154 internal bandgap reference source and internal reference buffer, drive the REF pin with a reference voltage in the range of 2.5V to 4.25V and place at least a 10µF capacitor as close as possible to the REF pin.

When using the MAX11154 in external reference mode, it is recommended that an external reference buffer be used. For bypass capacitors on the REF pin, X7R or X5R ceramic capacitors in a 1210 case size or smaller have been found to provide adequate bypass performance. Y5U or Z5U ceramics capacitors are not recommended due to their high voltage and temperature coefficients.

Maxim offers a wide range of precision references ideal for 18-bit accuracy. Table 1 lists some of the options recommended.

Input Amplifier

The conversion results are accurate when the ADC acquires the input signal for an interval longer than the input signal's worst-case settling time. The ADC input sampling capacitor charges during the acquisition period. During this acquisition period, the settling of the sampled voltage is affected by the source resistance and the input sampling capacitance. Sampling error can be estimated by modeling the time constant of the total input capacitance and the driving source impedance.

Although the device is easy to drive, an amplifier buffer is recommended if the source impedance is such that when driving a switch capacitor of ~32pF a significant settling error in the desired sampling period will occur. If this is the case, it is recommended that a configuration shown in the *Typical Operating Circuit* is used where at least a 4.7nF capacitor is attached to the AIN+ pin. This capacitance reduces the size of the transient at the start of the acquisition period, which in some buffers will cause an input signal dependent offsets.

Regardless of whether an external buffer amp is used or not, the time constant, $R_{SOURCE} \times C_{LOAD}$, of the input should not exceed $t_{ACQ}/14$, where R_{SOURCE} is the total signal source impedance, C_{LOAD} is the total capacitance at the ADC input (external and internal) and t_{ACQ} is the acquisition period. Thus to obtain accurate sampling in a 500ns acquisition time a source impedance of less than 1.3kΩ should be used if driving the ADC directly. When driving the ADC from a buffer, it is recommended a series resistance (5Ω to 15Ω typical) between the amplifier and the external input capacitance as shown in the *Typical Operating Circuit*.

These amplifier features help select the ADC driver.

1) Fast settling time: For multichannel multiplexed applications the driving operational amplifier must be able to settle to 18-bit resolution when a full-scale step is applied during the minimum acquisition time.
2) Low noise: It is important to ensure that the driver amplifier has a low average noise density appropriate for the desired bandwidth of the application. When the MAX11154 is used with its full bandwidth of 6MHz, it is preferable to use an amplifier that will produce an output noise spectral density of less than 3nV/√Hz, to ensure that the overall SNR is not degraded significantly. It is recommended to insert an external RC filter at the MAX11154 AIN+ input to attenuate out-of-band

Table 1. MAX11154 External Reference Recommendations

PART	V_{OUT} (V)	TEMPERATURE COEFFICIENT (MAX)	INITIAL ACCURACY (%)	NOISE (0.1Hz TO 10Hz) (μV_{P-P})	PACKAGE
MAX6126	2.5, 3, 4.096, 5.0	3 (A), 5 (B)	0.06	1.35	µMAX-8 SO-8
MAX6325 MAX6341 MAX6350	2.5, 4.096, 5.0	1	0.04, 0.02	1.5, 2.4, 3.0	SO-8

input noise and preserve the ADC's SNR. The effective RMS noise at the MAX11154 AIN+ input is 32µV, thus additional noise from a buffer circuit should be significantly lower in order to achieve the maximum SNR performance.

3) THD performance: The input buffer amplifier used should have a comparable THD performance with that of the MAX11154 to ensure the THD of the digitized signal is not degraded.

Table 2 summarizes the operational amplifiers that are compatible with the MAX11154. The MAX9632 has sufficient bandwidth, low enough noise and distortion to support the full performance of the MAX11154. The MAX9633 is a dual amp and can support buffering for true pseudo-differential sampling.

Transfer Function

The ideal transfer characteristic for the MAX11154 is shown in Figure 3. The precise location of various points on the transfer function are given in Table 3.

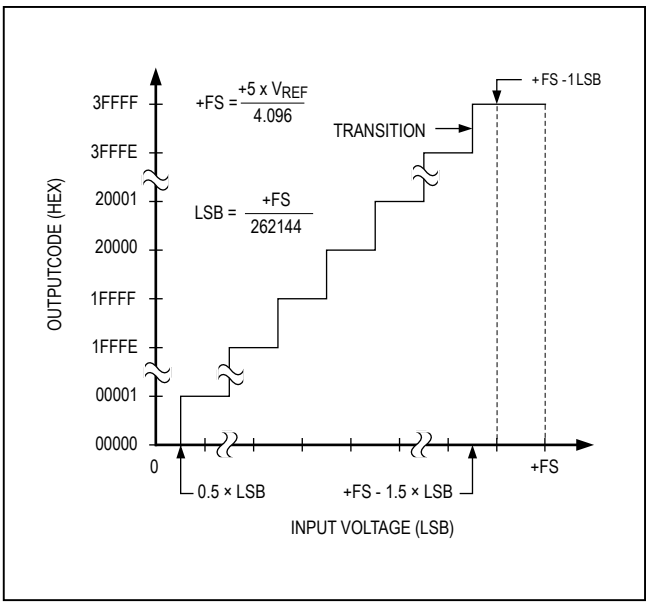


Figure 3. Unipolar Transfer Function

Table 2. List of Recommended ADC Driver Op Amps for MAX11154

AMPLIFIER	INPUT-NOISE DENSITY (nV/√Hz)	SMALL-SIGNAL BANDWIDTH (MHz)	SLEW RATE (V/µs)	THD (dB)	I_{CC} (mA)	COMMENTS
MAX9632	0.9	55	30	-128	3.9	Low noise, THD at 10kHz
MAX9633	3	27	18	-130	3.5/amp	Low noise, dual amp, THD at 10kHz

Table 3. Transfer Function Example

CODE TRANSITION	BIPOLAR INPUT (V)	DIGITAL OUTPUT CODE (HEX)
+FS - 1.5 LSB	4.9999714	3FFFE - 3FFFF
Midscale + 0.5 LSB	2.5000095	20000 - 20001
Midscale	2.500000	20000
Midscale - 0.5 LSB	2.4999905	1FFFF - 20000
-FS + 0.5 LSB	0.0000095	00000 - 00001

Input Configuration Interface

An SPI interface clocked at up to 50MHz controls the MAX11154. Input configuration data is clocked into the configuration register on the falling edge of SCLK through the DIN pin. The data on DIN is used to program the ADC configuration register. The construct of this register is illustrated in Table 4. The configuration register defines the output interface mode, the reference mode, and the power-down state of the MAX11154.

Configuring in $\overline{CS}$ Mode

Figure 4 details the timing for loading the input configuration register when the MAX11154 is connected in $\overline{CS}$ mode (see Figure 6 and Figure 8 for hardware connections). The load process is enabled on the falling edge of CNVST when SCLK is held high. The configuration data is clocked into the configuration register through DIN on the next 8 SCLK falling edges. Pull CNVST high to complete the input configuration register load process. DIN should idle high outside an input configuration register read.

Table 4. ADC Configuration Register

BIT NAME	BIT	DEFAULT STATE	LOGIC STATE	FUNCTION
MODE	7:6	00	00	$\overline{CS}$ Mode, No-Busy Indicator
			01	$\overline{CS}$ Mode, with Busy Indicator
			10	Daisy-Chain Mode, No-Busy Indicator
			11	Daisy-Chain Mode, with Busy Indicator
REF	5:4	00	00	Reference Mode 0. Internal reference and reference buffer are both powered on.
			01	Reference Mode 1. Internal reference is turned off, but internal reference buffer powered on. Apply the external reference voltage at REFIO.
			10	Reference Mode 2. Internal reference is powered on, but the internal reference buffer is powered off. This mode allows for internal reference to be used with an external reference buffer.
			11	Reference Mode 3. Internal reference and reference buffer are both powered off. Apply an external reference voltage at REF.
SHDN	3	0	0	Normal Mode. All circuitry is fully powered up at all times.
			1	Static Shutdown. All circuitry is powered down.
Reserved	2:0	0	0	Reserved, Set to 0

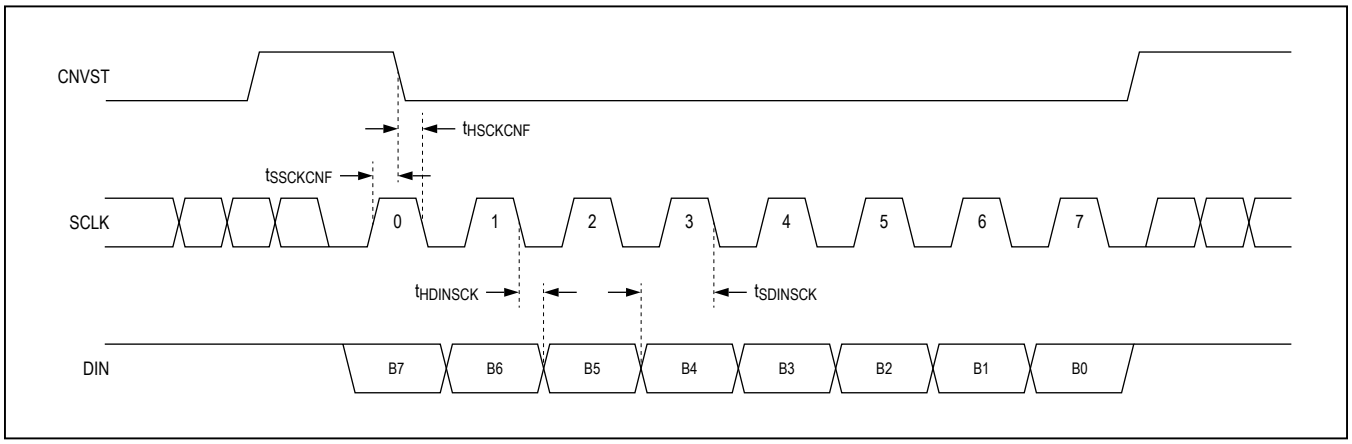


Figure 4. Input Configuration Timing in $\overline{CS}$ Mode

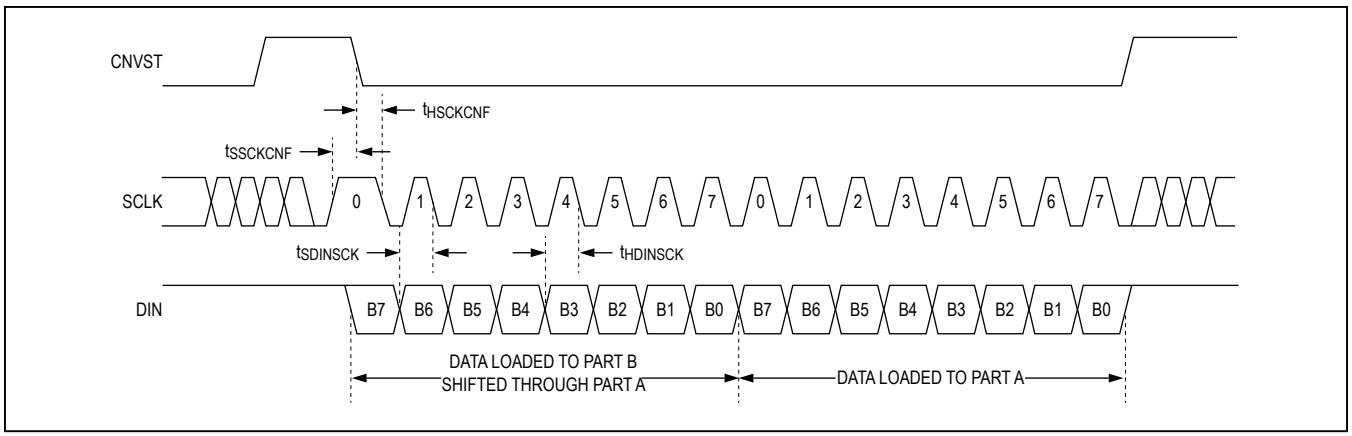


Figure 5. Input Configuration Timing in Daisy-Chain Mode

Configuring in Daisy-Chain Mode

Figure 5 details the configuration register load process when the MAX11154 is connected in a daisy-chain configuration (see Figure 12 and Figure 14 for hardware connections). The load process is enabled on the falling edge of CNVST when SCLK is held high. In daisy-chain mode, the input configuration registers are chained together through DOUT to DIN. Device A's DOUT will drive device B's DIN. The input configuration register is an 8-bit, first-in first-out shift register. The configuration data is clocked in N times through 8 x N falling SCLK edges. After the MAX11154 ADC in the chain is loaded with the configuration byte, pull CNVST high to complete the configuration register loading process. Figure 5 illustrates a configuration sequence for loading two devices in a chain.

Data loaded into the configuration register alters the state of the MAX11154 on the next conversion cycle after the register is loaded. However, powering up the internal reference buffer or stabilizing the REFIO pin voltage will take several milliseconds to settle to 18-bit accuracy.

Shutdown Mode

The SHDN bit in the configuration register forces the MAX11154 into and out of shutdown. Set SHDN to 0 for normal operation. Set SHDN to 1 to shut down all internal circuitry and reset all registers to their default state.

Output Interface

The MAX11154 can be programmed into one of four output modes; $\overline{CS}$ modes with and without busy indicator and daisy-chain modes with and without busy indicator. When operating without busy indication, the user must externally timeout the maximum ADC conversion time before commencing readback. When operating in one of the two busy indication modes, the user can connect the DOUT output of the MAX11154 to an interrupt input on the digital host and use this interrupt to trigger the output data read.

Regardless of the output interface mode used, digital activity should be limited to the first half of the conversion phase. Having SCLK or DIN transitions near the sampling instance can also corrupt the input sample accuracy. Therefore, keep the digital inputs quiet for approximately 25ns before and 10ns after the rising edge of CNVST. These times are denoted as t_{SQ} and t_{HQ} in all subsequent timing diagrams.

In all interface modes, the data on DOUT is valid on both SCLK edges. However, the input setup time into the receiving digital host will be maximized when data is clocked into that digital host on the falling SCLK edge. Doing so will allow for higher data transfer rates between the MAX11154 and the digital host and consequently higher converter throughput.

In all interface modes, it is recommended that the SCLK be idled low to avoid triggering an input configuration write

on the falling edge of CNVST. If at anytime the device detects a high SCLK state on a falling edge of CNVST, it will enter the input configuration write mode and will write the state of DIN on the next 8 falling SCLK edges to the input configuration register.

In all interface modes, all data bits from a previous conversion must be read before reading bits from a new conversion. When reading out conversion data, if too few SCLK falling edges are provided and all data bits are not read out, only the remaining unread data bits will be outputted during the next readout cycle. In such an event, the output data in every other readout cycle will appear to have been truncated as only the leftover bits from the previous readout cycle are outputted. This is an indication to the user that there are insufficient SCLK falling edges in a given readout cycle. Table 5 provides a guide to aid in the selection of the appropriate output interface mode for a given application.

$\overline{CS}$ No-Busy Indicator Mode

The $\overline{CS}$ no-busy indicator mode is ideally suited for maximum throughput when a single MAX11154 is connected to a SPI-compatible digital host. The connection diagram is shown in Figure 6, and the corresponding timing is provided in Figure 7.

A rising edge on CNVST completes the acquisition, initiates the conversion, and forces DOUT to high impedance. The conversion continues to completion irrespective of the state of CNVST allowing CNVST to be used as a select line for other devices on the board. If CNVST is brought low during a conversion and held low throughout the maximum conversion time, the MSB will be output at the end of the conversion.

When the conversion is complete, the device enters the acquisition phase. Drive CNVST low to output the MSB onto DOUT. The remaining data bits are then clocked by subsequent SCLK falling edges. DOUT returns to high impedance after the 18th SCLK falling edge, or when CNVST goes high.

Table 5. ADC Output Interface Mode Selector Guide

MODE	TYPICAL APPLICATION AND BENEFITS
$\overline{CS}$ Mode, No-Busy Indicator	Single or multiple ADCs connected to SPI-compatible digital host. Ideally suited for maximum throughput.
$\overline{CS}$ Mode, With Busy Indicator	Single ADC connected to SPI-compatible digital host with interrupt input. Ideally suited for maximum throughput.
Daisy-Chain Mode, No-Busy Indicator	Multiple ADCs connected to a SPI-compatible digital host. Ideally suited for multichannel simultaneous sampled isolated applications.
Daisy-Chain Mode, With Busy Indicator	Multiple ADCs connected to a SPI-compatible digital host with interrupt input. Ideally suited for multichannel simultaneous sampled isolated applications.

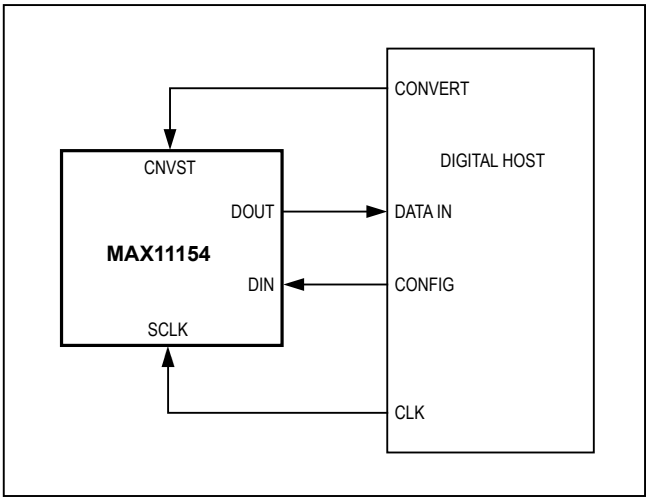


Figure 6. $\overline{CS}$ No-Busy Indicator Mode Connection Diagram

$\overline{CS}$ with Busy Indicator Mode

The $\overline{CS}$ with busy indicator mode is shown in Figure 8 where a single ADC is connected to a SPI-compatible digital host with interrupt input. The corresponding timing is given in Figure 9.

A rising edge on CNVST completes the acquisition, initiates the conversion and forces DOUT to high impedance. The conversion continues to completion irrespective of the state of CNVST allowing CNVST to be used as a select line for other devices on the board.

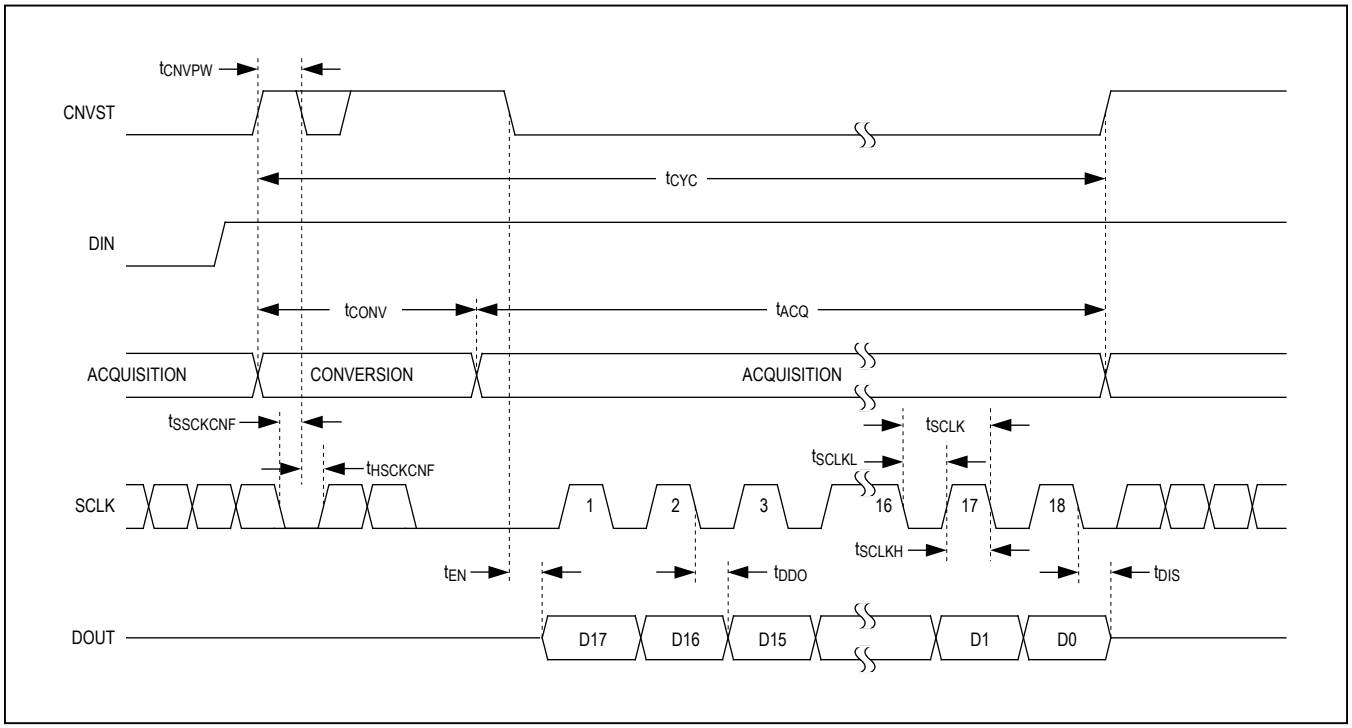


Figure 7. $\overline{CS}$ No Busy Indicator Mode Timing

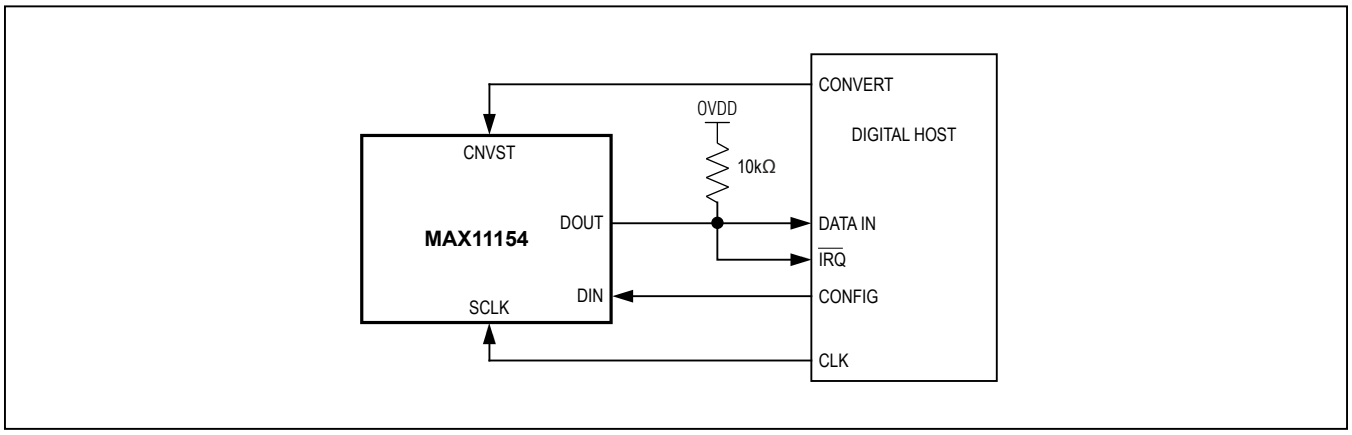


Figure 8. $\overline{CS}$ With Busy Indicator Mode Connection Diagram

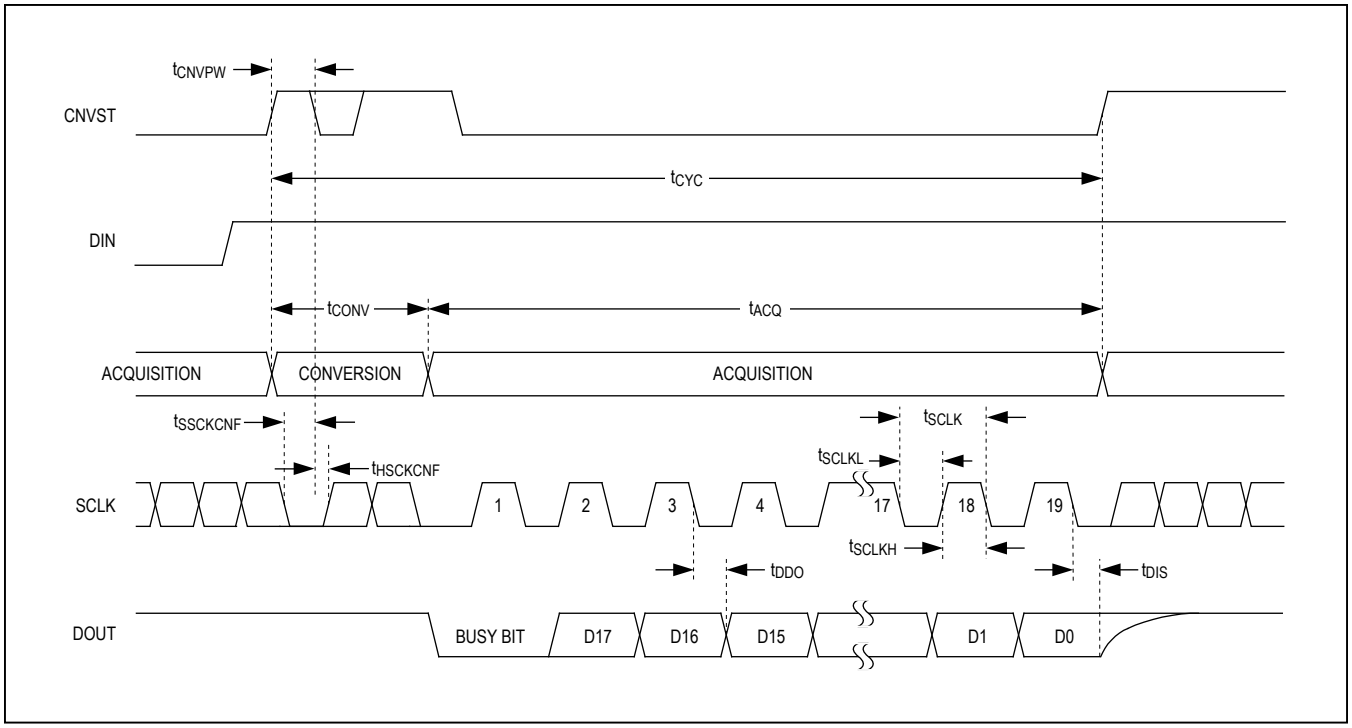


Figure 9. $\overline{CS}$ With Busy Indicator Mode Timing

When the conversion is complete, DOUT transitions from high impedance to a low logic level, signaling to the digital host through the interrupt input that data readback can commence. The MAX11154 then enters the acquisition phase. The data bits are then clocked out, MSB first, by subsequent SCLK falling edges. DOUT returns to high impedance after the 19th SCLK falling edge or when CNVST goes high, and is then pulled to OVDD through the external pullup resistor.

Multichannel $\overline{CS}$ Configuration, Asynchronous or Simultaneous Sampling

The multichannel $\overline{CS}$ configuration is generally used when multiple MAX11154 ADCs are connected to an SPI-compatible digital host. Figure 10 shows the connection diagram example using two MAX11154 devices. Figure 11 shows the corresponding timing.

Asynchronous or simultaneous sampling is possible by controlling the $\overline{CS1}$ and $\overline{CS2}$ edges. In Figure 10, the DOUT bus is shared with the digital host limiting the throughput rate. However, maximum throughput is possible if the host accommodates each ADC's DOUT pin independently.

A rising edge on CNVST completes the acquisition, initiates the conversion and forces DOUT to high impedance. The conversion continues to completion irrespective of the state of CNVST allowing CNVST to be used as a select line for other devices on the board. However, CNVST must be returned high before the minimum conversion time for proper operation so that another conversion is not initiated with insufficient acquisition time and data correctly read out of the device.

When the conversion is complete, the MAX11154 enters the acquisition phase. Each ADC result can be read by bringing its CNVST input low, which consequently outputs the MSB onto DOUT. The remaining data bits are then clocked by subsequent SCLK falling edges. For each device, its DOUT will return to a high-impedance state after the 18th SCLK falling edge or when CNVST goes high. This control allows multiple devices to share the same DOUT bus.

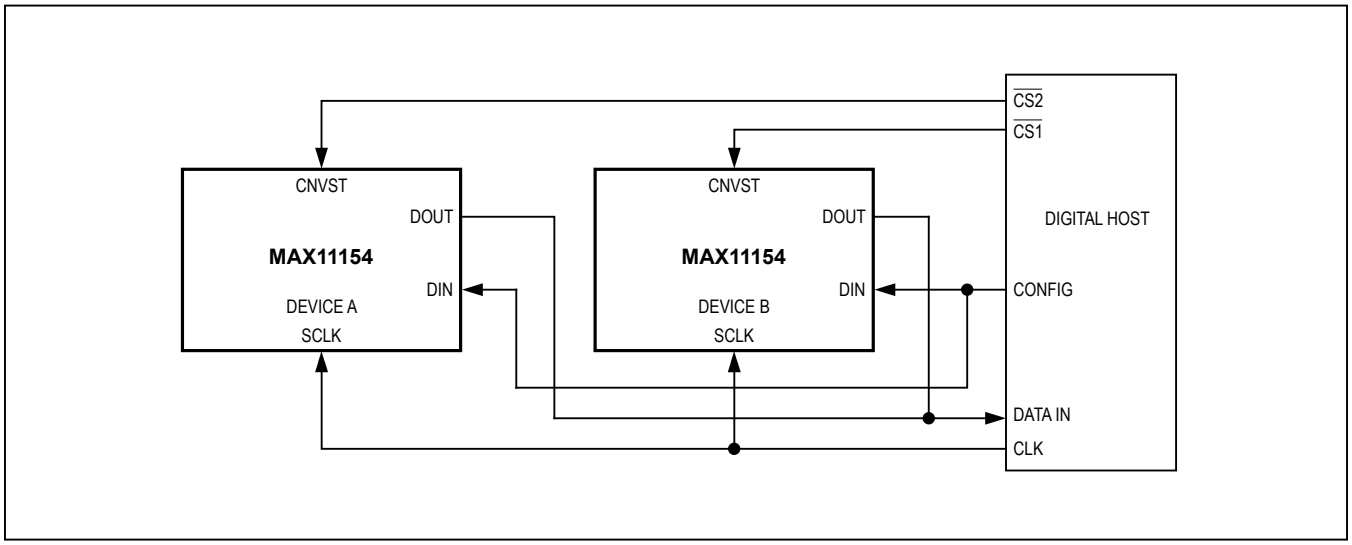


Figure 10. Multichannel $\overline{CS}$ Configuration Diagram

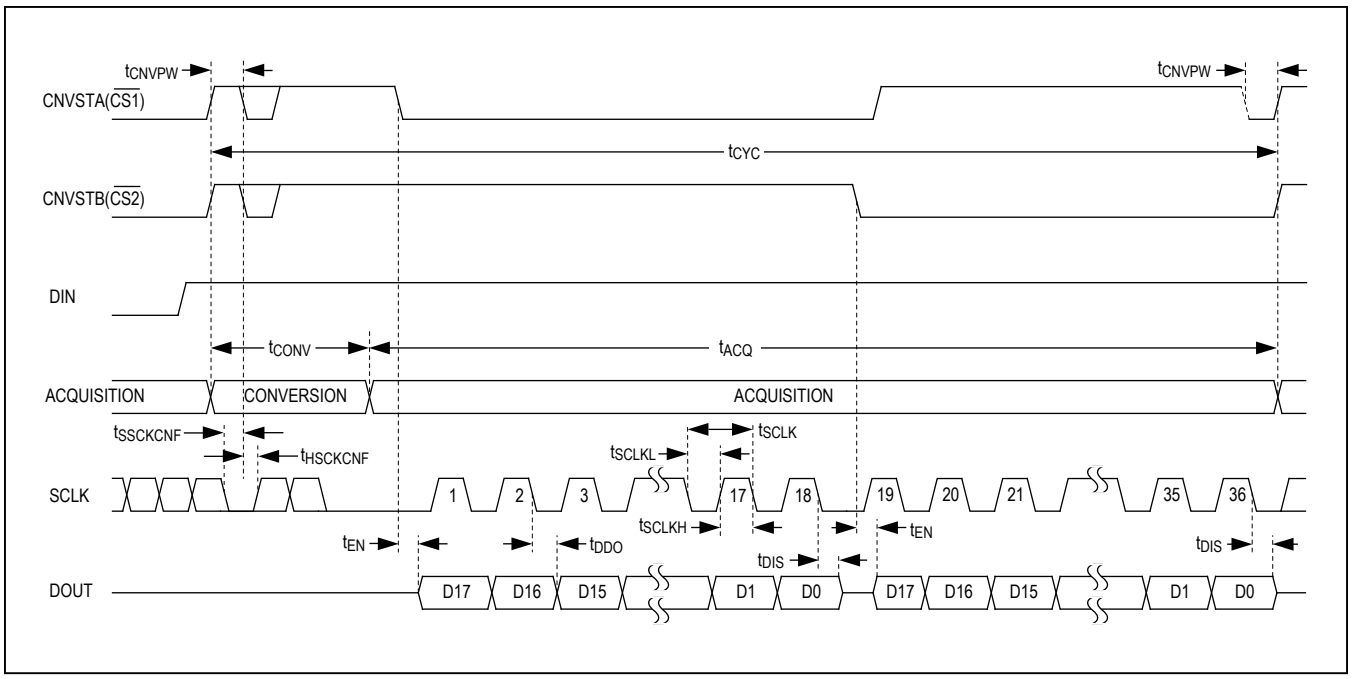


Figure 11. Multichannel $\overline{CS}$ Configuration Timing

Daisy-Chain, No-Busy Indicator Mode

The daisy-chain mode with no-busy indicator is ideally suited for multichannel isolated applications that require minimal wiring complexity. Simultaneous sampling of multiple ADC channels is realized on the serial interface where data readback is analogous to clocking a shift register. Figure 12 shows a connection diagram of two MAX11154s configured in a daisy chain. The corresponding timing is given in Figure 13.

A rising edge on CNVST completes the acquisition and initiates the conversion. Once a conversion is initiated, it continues to completion irrespective of the state of CNVST. When a conversion is complete, the MSB is presented onto DOUT and the MAX11154 returns to the acquisition phase. The remaining data bits are stored within an internal shift register. To read these bits out, CNVST is brought low and each bit is shifted out on subsequent SCLK falling edge. The DIN input of each ADC in the chain is used to transfer conversion data from the previous ADC into the internal shift register of the next ADC, thus allowing for data to be clocked through the multichip chain on each SCLK falling edge. Each ADC in the chain outputs its MSB data first requiring 18 × N clocks to read back N ADCs.

In daisy-chain mode, the maximum conversion rate is reduced due to the increased readback time. For instance, with a 6ns or less digital host setup time and 3V interface, up to four MAX11154 devices running at a conversion rate of 320ksps can be daisy-chained.

Daisy-Chain with Busy Indicator Mode

The daisy-chain mode with busy indicator is ideally suited for multichannel isolated applications that require minimal wiring complexity while providing a conversion complete indication that can be used to interrupt a host processor to read data.

Simultaneous sampling of multiple ADC channels is realized on the serial interface where data readback is analogous to clocking a shift register. The daisy-chain mode with busy indicator is shown in Figure 14 where three MAX11154s are connected to a SPI-compatible digital host with corresponding timing given in Figure 15.

A rising edge on CNVST completes the acquisition and initiates the conversion. Once a conversion is initiated, it

continues to completion irrespective of the state of CNVST. When a conversion is complete, the busy indicator is presented onto each DOUT and the MAX11154 returns to the acquisition phase. The busy indicator for the last ADC in the chain can be connected to an interrupt input on the digital host. The digital host should insert a 50ns delay from the receipt of this interrupt before reading out data from all ADCs to ensure that all devices in the chain have completed conversion.

The conversion data is stored within an internal shift register. To read these bits out, CNVST is brought low and each bit is shifted out on subsequent SCLK falling edge. The DIN input of each ADC in the chain is used to transfer conversion data from the previous ADC into the internal shift register of the next ADC, thus allowing for data to be clocked through the multichip chain on each SCLK falling edge. The total of number of falling SCLKs needed to read back all data from N ADCs is 18 × N + 1 edges, the one additional SCLK falling edge required to clock out the busy mode bit from the host side ADC.

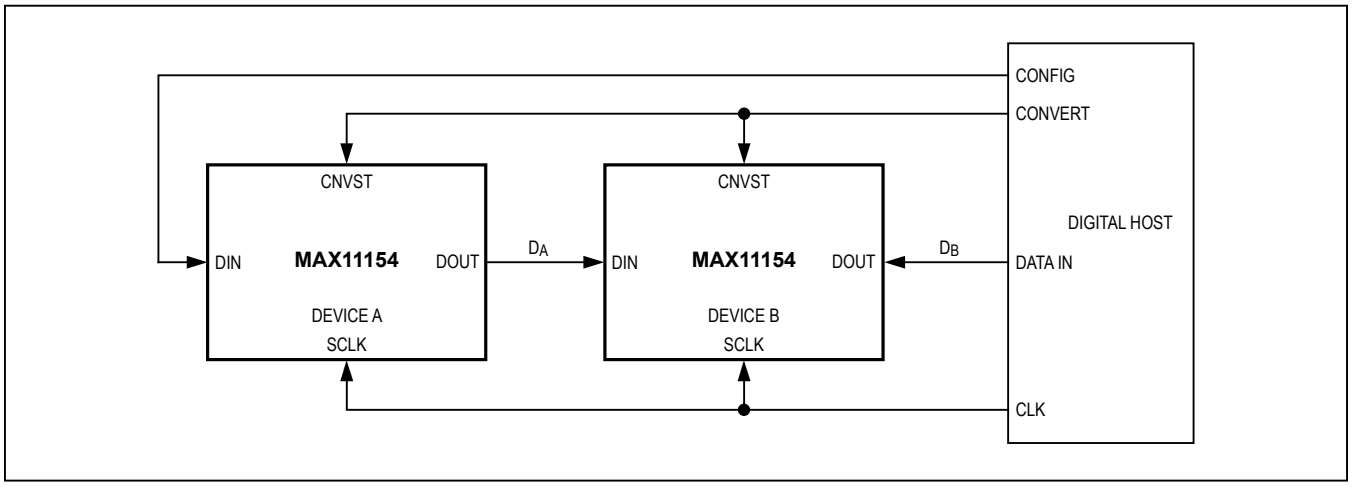


Figure 12. Daisy-Chain, No-Busy Indicator Mode Connection Diagram

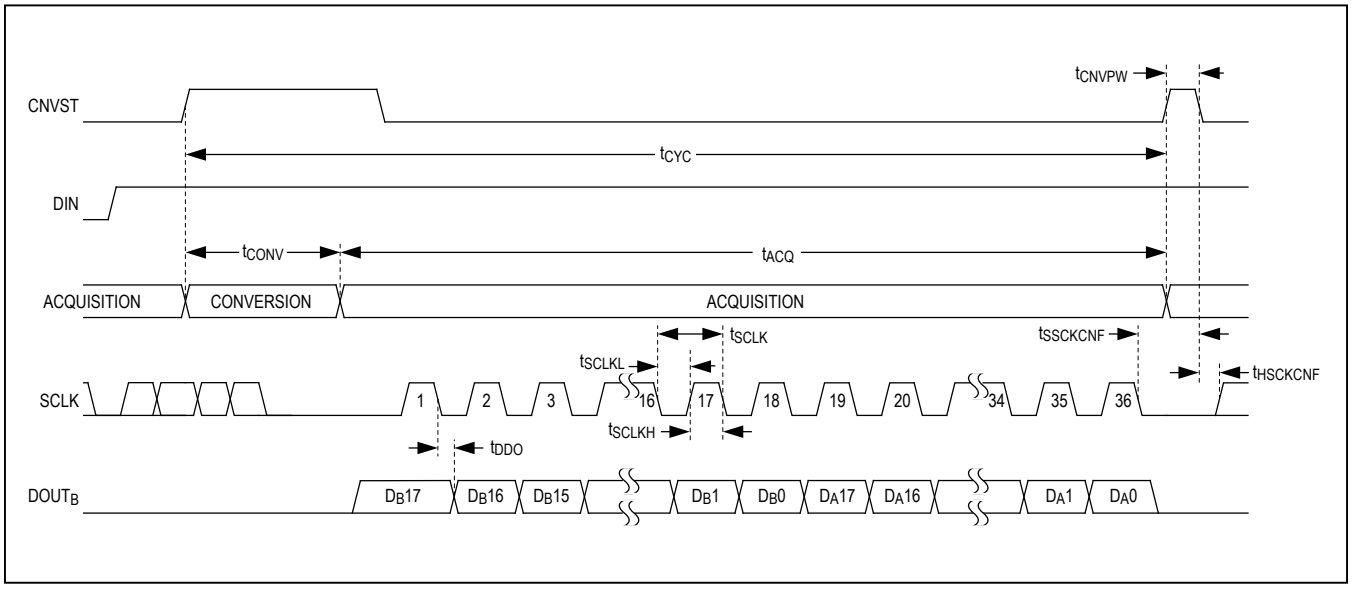


Figure 13. Daisy-Chain, No-Busy Indicator Mode Timing

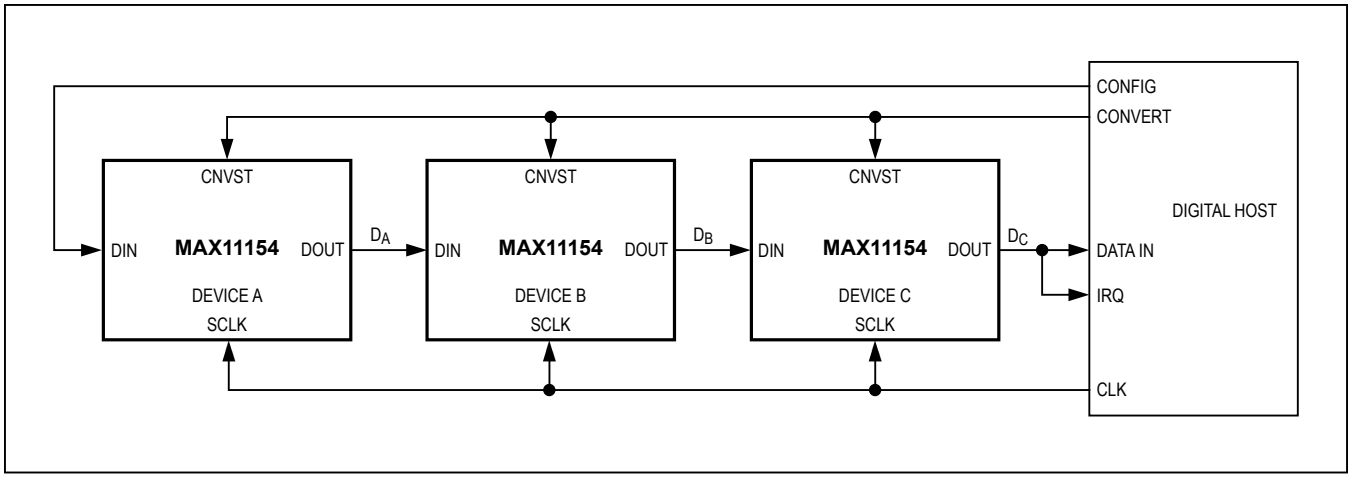


Figure 14. Daisy-Chain Mode with Busy Indicator Connection Diagram

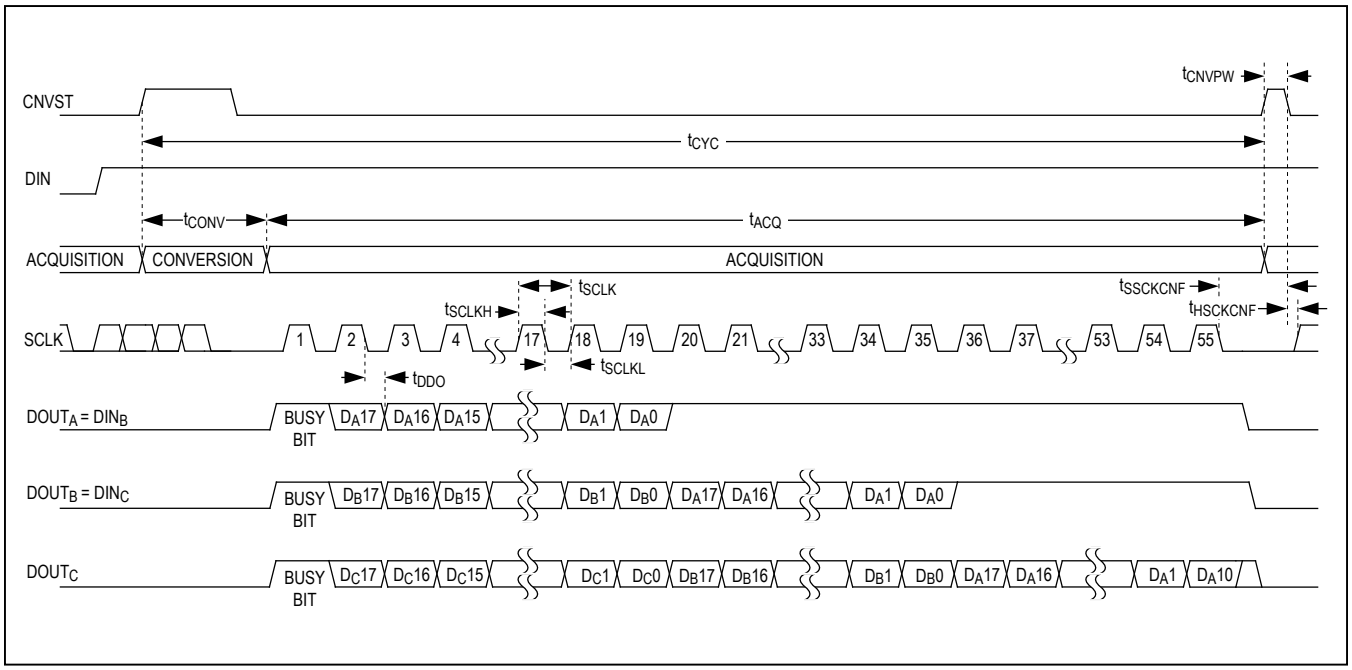


Figure 15. Daisy-Chain Mode with Busy Indicator Timing

In daisy-chain mode, the maximum conversion rate is reduced due to the increased readback time. For instance, with a 6ns or less digital host setup time and 3V interface, up to four MAX11154 devices running at a conversion rate of 317ksps can be daisy-chained on a 3-wire port.

Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect the GND and AGNDS pins on the MAX11154 to this ground plane. Keep the ground return to the power-supply low impedance and as short as possible for noise-free operation.

A 4.7nF C0G (or NPO) ceramic capacitor should be placed between AIN+ and the ground plane as close as possible to the MAX11154. This capacitor reduces the inductance seen by the sampling circuitry and reduces the voltage transient seen by the input source circuit.

For best performance, connect the REF output to the ground plane with a 16V, 10µF ceramic capacitor with a X5R or X7R dielectric in a 1210 or smaller case size. Ensure that all bypass capacitors are connected directly into the ground plane with an independent via.

Bypass V_{DD} and OVDD to the ground plane with 0.1µF ceramic capacitors on each pin as close as possible to the device to minimize parasitic inductance. Add at least one bulk 10µF decoupling capacitor to V_{DD} and OVDD per PCB. For best performance, bring a V_{DD} power plane from the analog interface side of the MAX11154 and a OVDD power plane from the digital interface side of the device.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the Electrical Characteristics table. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

For the MAX11154, the offset error is defined at the code center 0x00000. The code center should occur at 0V input between AIN+ and AIN-. The offset error is the actual voltage required to produce code center 0x00000, expressed in LSB.

Gain Error

Gain error is designed as the difference between the acutal change in analog input voltage required to produce a top code transition minus a bottom code transition, and the ideal change in analog input voltage range to produce the same code transitions. It is expressed in LSB.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input power to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the power signal to the power noise, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of RMS amplitude of the fundamental input frequency to the RMS equivalent of all other ADC output signals:

$$SINAD(dB) = 20 \times \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits

The effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the power contained in the first five harmonics of the converted data to the power of the fundamental. This is expressed as:

$$THD = 10 \times \log \left[\frac{P_2 + P_3 + P_4 + P_5}{P_1} \right]$$

where P_1 is the fundamental power and P_2 through P_5 is the power of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the power of the fundamental (maximum signal component) to the power of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

Selector Guide

PART	BITS	INPUT RANGE (V)	REFERENCE	PACKAGE	SPEED (KSPS)
MAX11262	14	0 TO 5	EXTERNAL	3MM X 5MM MMAX-10	500
MAX11160	16	0 TO 5	INTERNAL	3MM X 5MM MMAX-10	500
MAX11161	16	0 TO 5	INTERNAL	3MM X 5MM MMAX-10	250
MAX11162	16	0 TO 5	EXTERNAL	3MM X 5MM MMAX-10	500
MAX11163	16	0 TO 5	EXTERNAL	3MM X 5MM MMAX-10	250
MAX11164	16	0 TO 5	INTERNAL/ EXTERNAL	3MM X 3MM TDFN-12	500
MAX11165	16	0 TO 5	INTERNAL/ EXTERNAL	3MM X 3MM TDFN-12	250
MAX11166	16	±5	INTERNAL/ EXTERNAL	3MM X 3MM TDFN-12	500
MAX11167	16	±5	INTERNAL/ EXTERNAL	3MM X 3MM TDFN-12	250
MAX11168	16	±5	INTERNAL	3MM X 5MM MMAX-10	500
MAX11169	16	±5	INTERNAL	3MM X 5MM MMAX-10	250
MAX11150	18	0 TO 5	INTERNAL	3MM X 5MM MMAX-10	500
MAX11152	18	0 TO 5	EXTERNAL	3MM X 5MM MMAX-10	500
MAX11154	18	0 TO 5	INTERNAL/ EXTERNAL	3MM X 3MM TDFN-12	500
MAX11156	18	±5	INTERNAL/ EXTERNAL	3MM X 3MM TDFN-12	500
MAX11158	18	±5	INTERNAL	3MM X 5MM MMAX-10	500

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11154ETC+T	-40°C TO +85°C	12 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 TDFN-EP	TD1233+1	21-0664	90-0397

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—
1	1/15	Revised the *Benefits and Features* section	1
2	11/15	Updated *Electrical Characteristics* table, *Typical Operating Characteristics*, and text updates.	1–12, 14, 15, 18, 20–23, 25–27

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