

SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs to Reduce dc Loading Effects
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

description

These 10-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

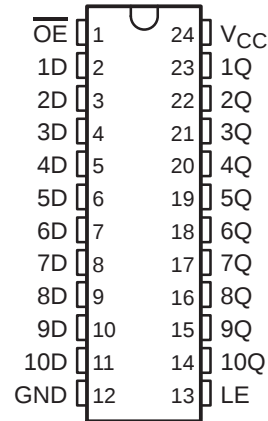
The ten latches are transparent D-type latches. The SN74ALS841 and SN74AS841A have noninverting data (D) inputs. The SN74ALS842 has inverting $\bar{D}$ inputs.

A buffered output-enable ($\overline{OE}$) input places the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

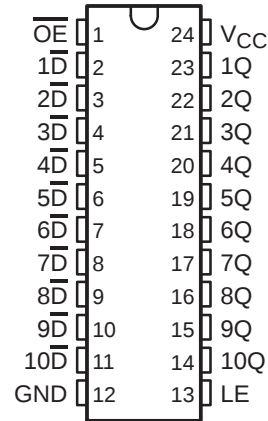
$\overline{OE}$ does not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are off.

The SN74ALS841, SN74AS841A, and SN74ALS842 are characterized for operation from 0°C to 70°C.

SN74ALS841, SN74AS841A . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS842 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS841, SN74AS841A, SN74ALS842

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

Function Tables

SN74ALS841, SN74AS841A

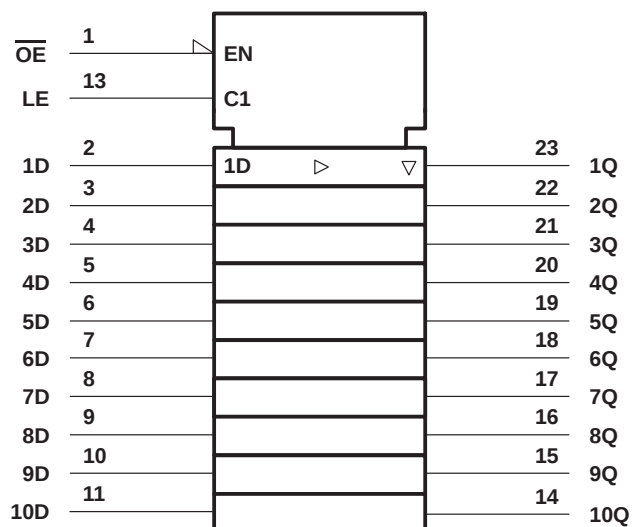
INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN74ALS842

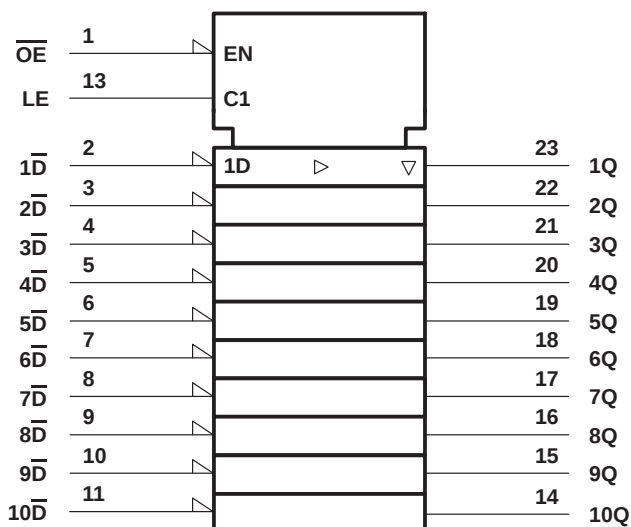
INPUTS			OUTPUT Q
$\overline{OE}$	LE	$\overline{D}$	
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic symbols[†]

SN74ALS841, SN74AS841A



SN74ALS842

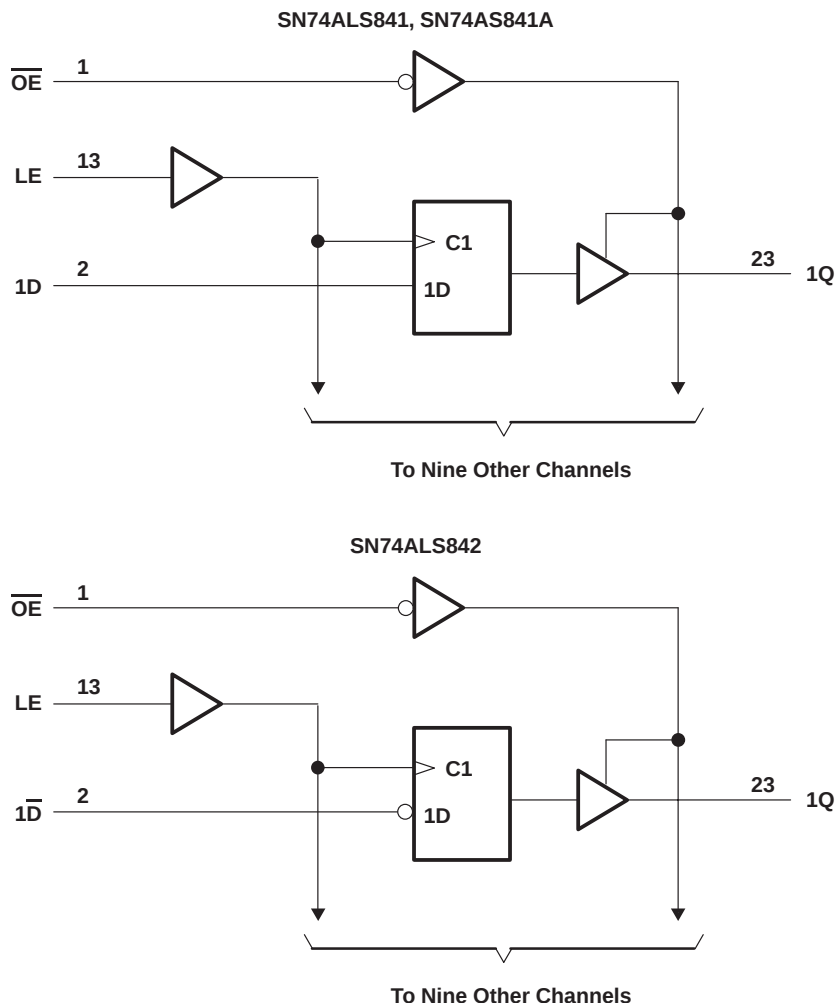


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN74ALS841, SN74ALS842	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS841, SN74AS841A, SN74ALS842

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

recommended operating conditions

		SN74ALS841 SN74ALS842			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration, LE high	20			ns
t_{su}	Setup time, data before LE↓	10			ns
t_h	Hold time, data after LE↓	5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS841 SN74ALS842			UNIT
				MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V,	I _I = −18 mA	−1.2			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V,	I _{OH} = −0.4 mA	V _{CC} − 2			V
		V _{CC} = 4.5 V,	I _{OH} = −2.6 mA	2.4	3.2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	V	
			I _{OL} = 24 mA	0.35	0.5		
I _{OZH}		V _{CC} = 5.5 V,	V _O = 2.7 V	20			μA
I _{OZL}		V _{CC} = 5.5 V,	V _O = 0.4 V	−20			μA
I _I		V _{CC} = 5.5 V,	V _I = 7 V	0.1			mA
I _{IH}		V _{CC} = 5.5 V,	V _I = 2.7 V	20			μA
I _{IL}		V _{CC} = 5.5 V,	V _I = 0.4 V	−0.1			mA
I _O [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	−30	−112		mA
I _{CC}	SN74ALS841	V _{CC} = 5.5 V	Outputs high	19	30		mA
			Outputs low	38	62		
			Outputs disabled	23	40		
	SN74ALS842	V _{CC} = 5.5 V	Outputs high	20	35		
			Outputs low	48	74		
			Outputs disabled	27	44		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN74ALS841, SN74AS841A, SN74ALS842

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS841		
			MIN	MAX	
t _{PLH}	D	Q	2	13	ns
t _{PHL}			2	13	
t _{PLH}	LE	Q	7	21	ns
t _{PHL}			8	26	
t _{PZH}	$\overline{\text{OE}}$	Q	2	12	ns
t _{PZL}			2	12	
t _{PHZ}	$\overline{\text{OE}}$	Q	2	10	ns
t _{PLZ}			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS842		
			MIN	MAX	
t _{PLH}	$\overline{\text{D}}$	Q	4	18	ns
t _{PHL}			3	13	
t _{PLH}	LE	Q	8	27	ns
t _{PHL}			6	20	
t _{PZH}	$\overline{\text{OE}}$	Q	2	12	ns
t _{PZL}			2	12	
t _{PHZ}	$\overline{\text{OE}}$	Q	1	10	ns
t _{PLZ}			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T _A : SN74AS841A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS841, SN74AS841A, SN74ALS842

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

recommended operating conditions

		SN74AS841A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, LE high	4			ns
t_{su}	Setup time, data before LE↓	2.5			ns
t_h	Hold time, data after LE↓	2.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS841A		UNIT
			MIN	TYP†	
V _{IK}	V _{CC} = 4.5 V,	I _I = −18 mA	−1.2		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA		V _{CC} − 2		V
	V _{CC} = 4.5 V	I _{OH} = −15 mA	2.4	3.2	
		I _{OH} = −24 mA	2		
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 48 mA	0.35	0.5	V
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V	50		μA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.4 V	−50		μA
I _I	V _{CC} = 5.5 V,	V _I = 7 V	0.1		mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V	20		μA
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V	−0.5		mA
I _O [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	−30	−112	mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	36	60	mA
		Outputs low	58	94	
		Outputs disabled	56	93	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS841, SN74AS841A, SN74ALS842

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

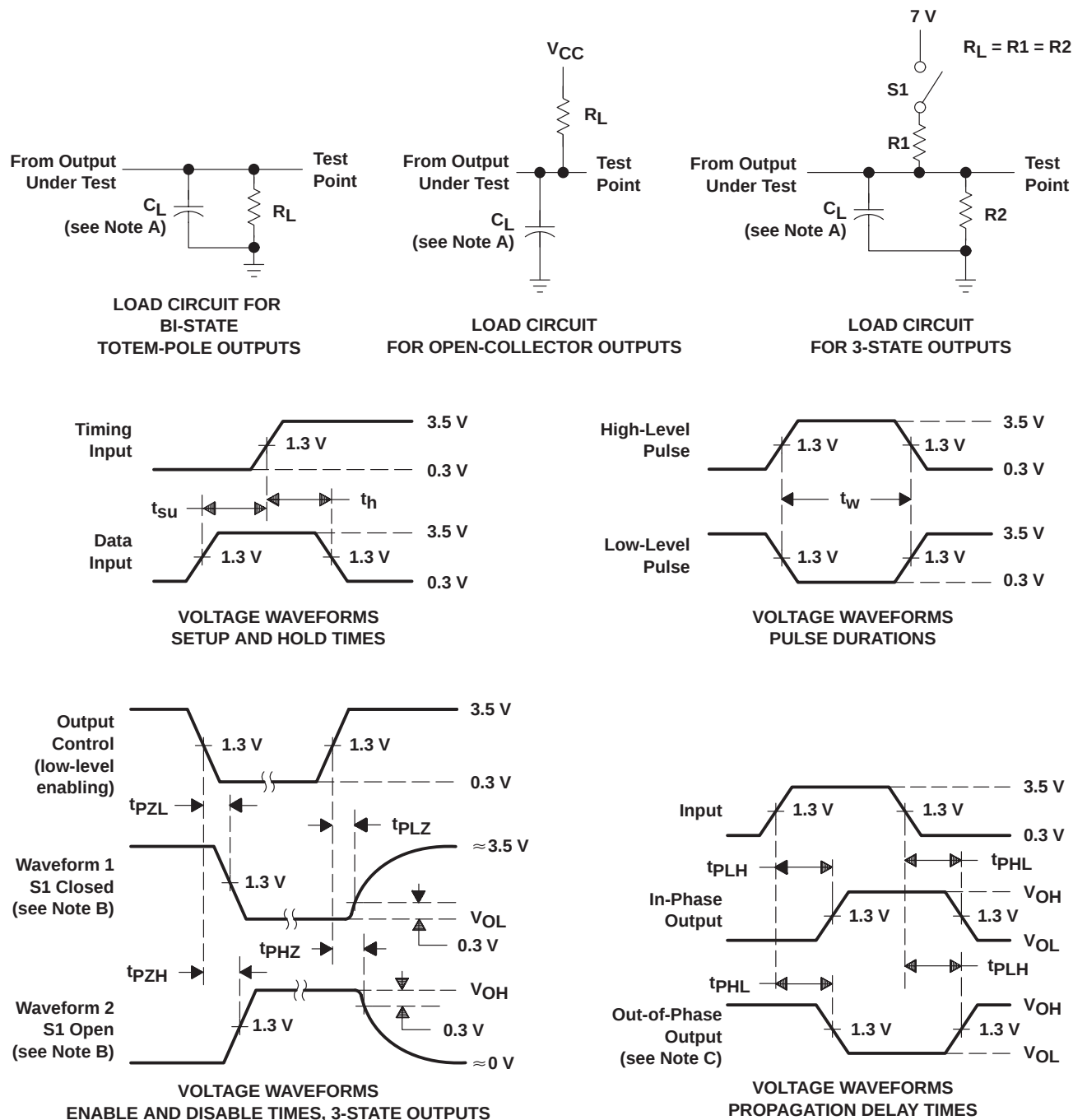
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74AS841A		
			MIN	MAX	
t _{PLH}	D	Q	1	6.5	ns
t _{PHL}			1	10.5	
t _{PLH}	LE	Q	2	12	ns
t _{PHL}			2	12	
t _{PZH}	$\overline{\text{OE}}$	Q	2	14	ns
t _{PZL}			2	16	
t _{PHZ}	$\overline{\text{OE}}$	Q	1	8	ns
t _{PLZ}			1	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS841DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS841	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

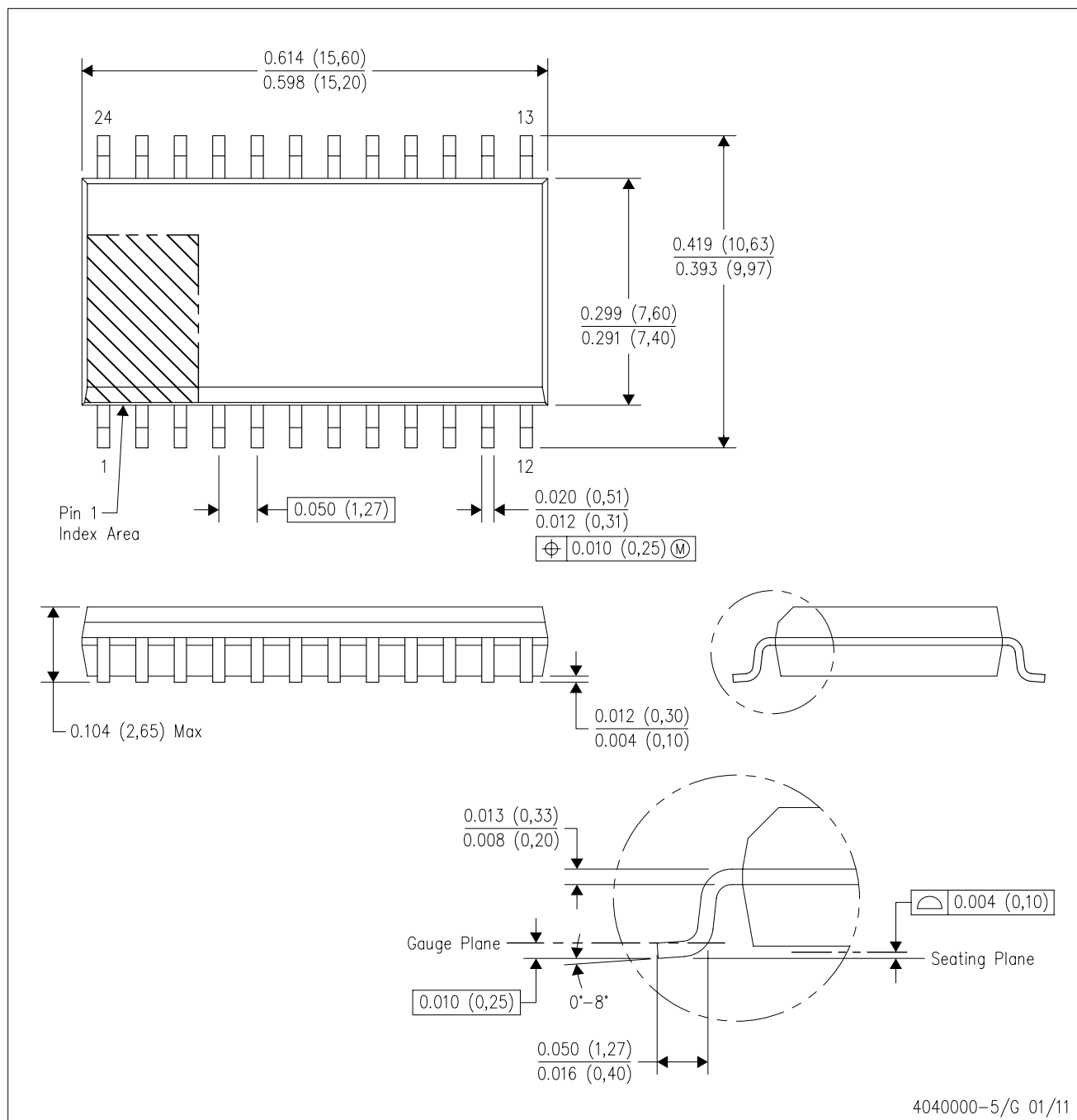
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated