Octal latched bidirectional Futurebus transceivers (3-State + open-collector)

74F8960/74F8961

FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE futurebus standards
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/down operation

DESCRIPTION

The 74F8960 and 74F8961 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired–OR bus. The B port inverting drivers are low–capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

Incident switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F8960 and 74F8961 A ports have TTL 3–state drivers and TTL receivers with a latch function. A separate High–level control input (VX) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, VX is simply tied to VCC.

The 74F8961 is the non–inverting version of 74F8960.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F8960	6.5ns	80mA
74F8961	6.5ns	80mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
28–pin plastic DIP (300 mil)[1]	N74F8960N, N748961N
28–pin PLCC[1]	N74F8960A, N74F8961A

NOTE: Thermal mounting techiques are recommended.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

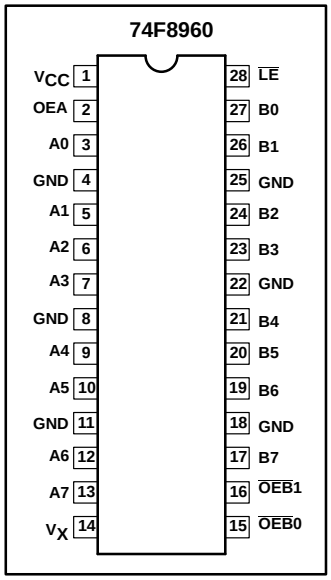
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A8	PNP latched inputs	3.5/0.117	70µA/70µA
B0 – B8	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A output enable input (active high)	1.0/0.033	20µA/20µA
$\overline{OEB}$0, $\overline{OEB}$1	B output enable inputs (active low)	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch enable input (active low)	1.0/0.033	20µA/20µA
A0 – A7	3–state outputs	150/40	3mA/24mA
B0 – B7	Open collector outputs	OC/166.7	OC/100mA

NOTES:
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
2. OC = Open collector.

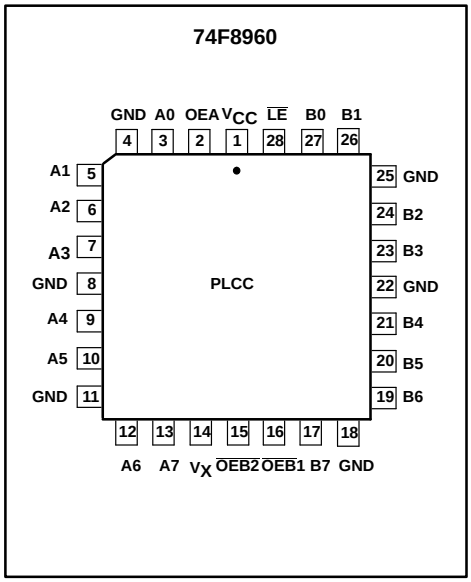
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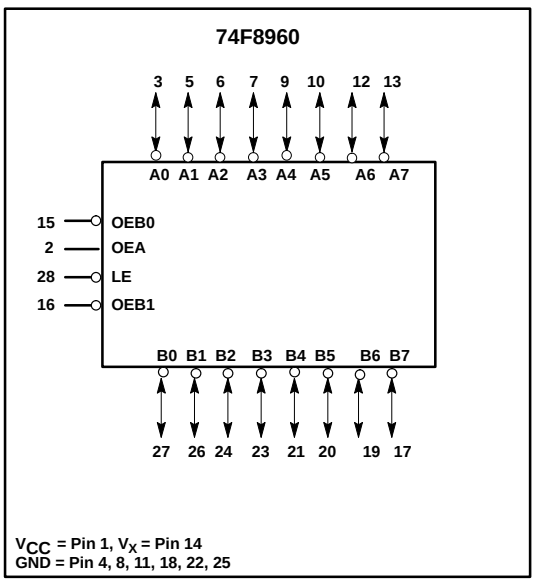
PIN CONFIGURATION



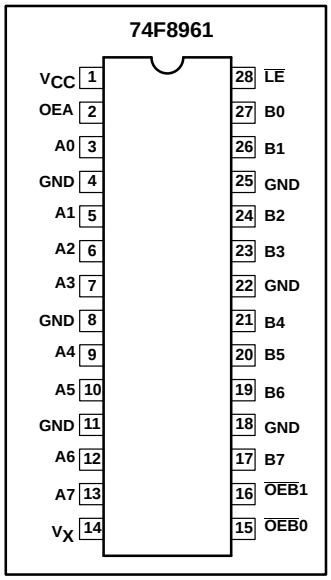
PIN CONFIGURATION PLCC



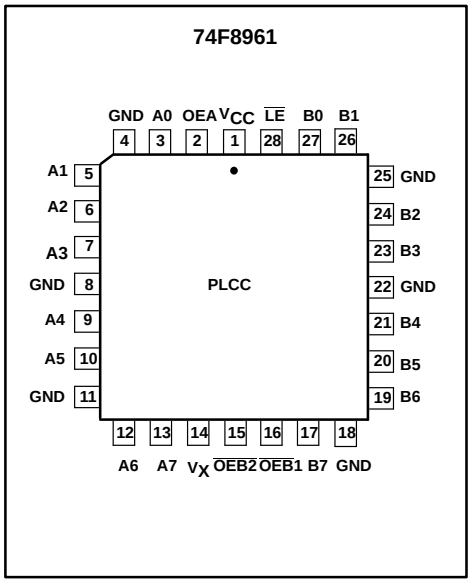
LOGIC SYMBOL



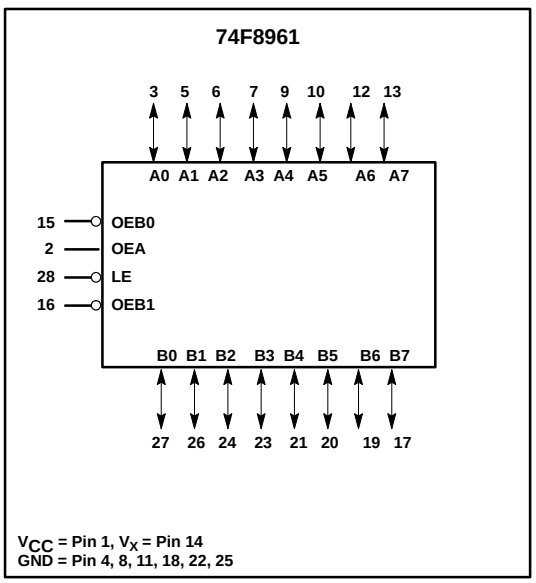
PIN CONFIGURATION



PIN CONFIGURATION PLCC



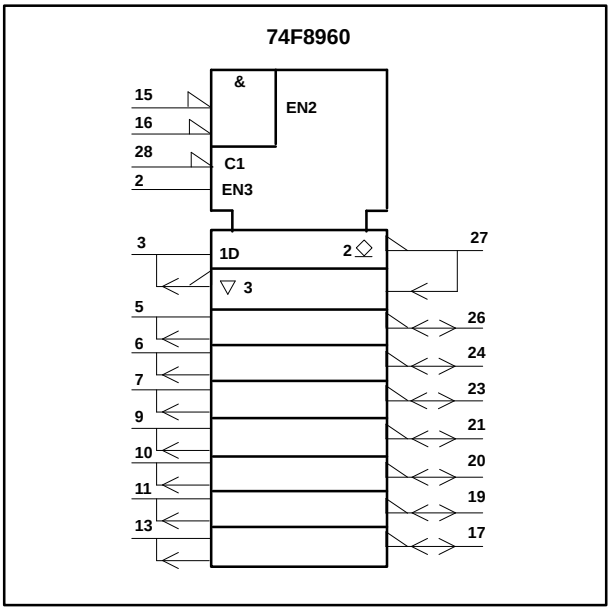
LOGIC SYMBOL



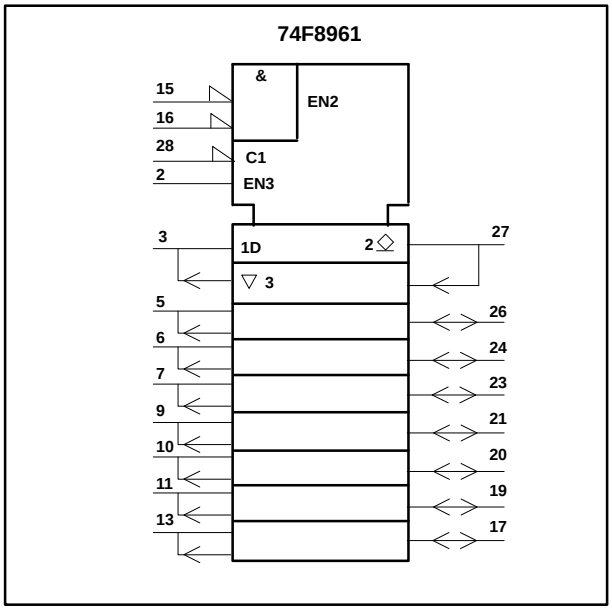
Octal latched bidirectional Futurebus transceivers (3-State + open-collector)

74F8960/74F8961

IEC/IEEE SYMBOL FOR 74F8960



IEC/IEEE SYMBOL FOR 74F8961



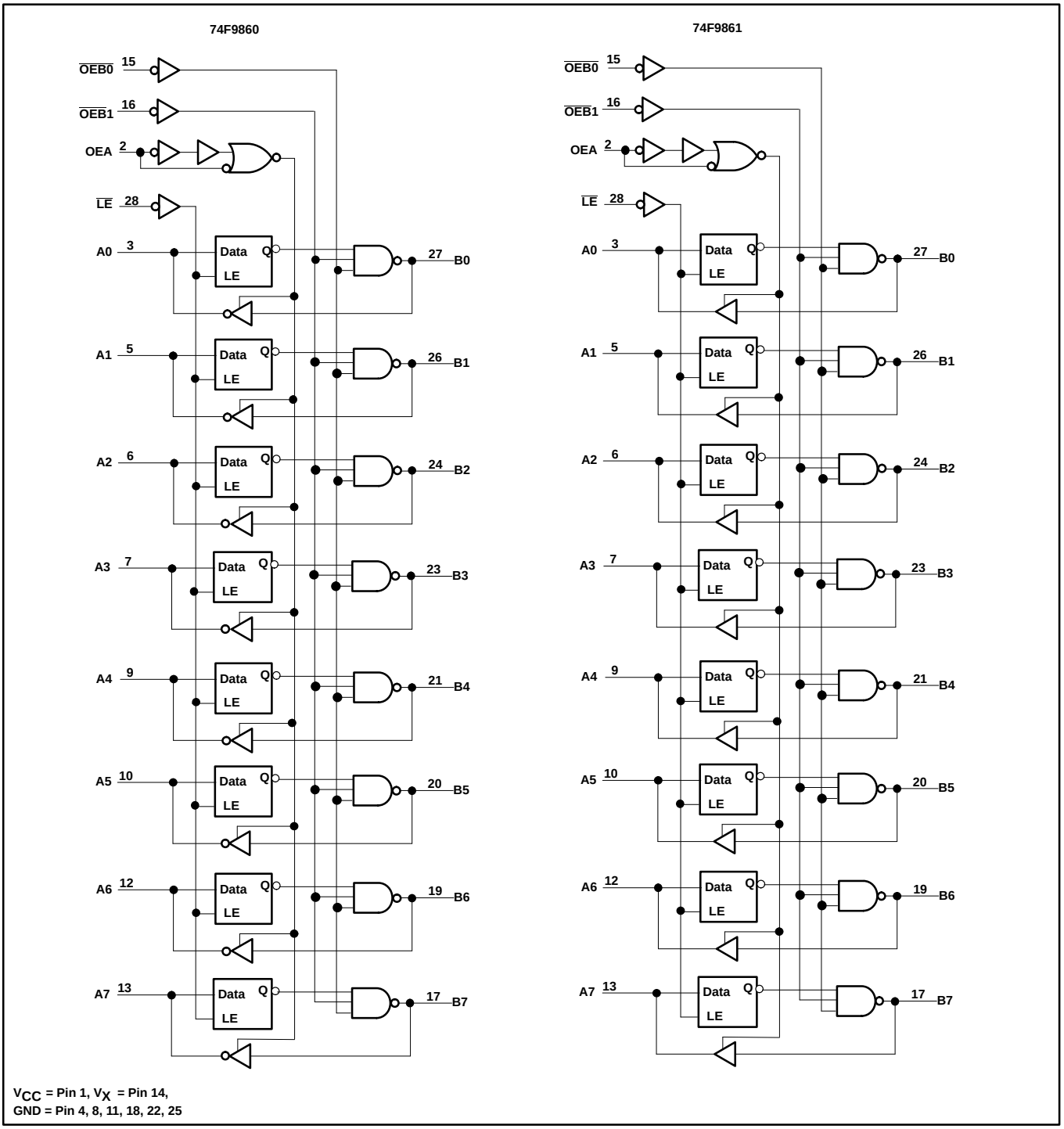
PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A7	3, 5, 6, 7, 9, 10, 12, 13	I/O	PNP latched input/3–state output (with V_X control option)
B0 – B7	27, 26, 24, 23, 21, 20, 19, 17	I/O	Data input with special threshold circuitry to reject noise/ open collector output, high current drive
$\overline{OEB}0$	15	Input	Enables the B outputs when both pins are low
$\overline{OEB}1$	16	Input	Enables the A outputs when high
$\overline{LE}$	28	Input	Latched when high (a special feature is buillt in for proper enabling times)
V_X	14	Input	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{cc}$ for normal use)

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LOGIC DIAGRAM



V_{CC} = Pin 1, V_X = Pin 14,
GND = Pin 4, 8, 11, 18, 22, 25

FUNCTION TABLE FOR 74F8960

INPUTS						LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$	OEA	$\overline{OEB0}$	$\overline{OEB1}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	L	A 3–state, data from A to B
L	X	L	L	L	L	L	Z	H**	
X	X	H	L	L	L	Qn	Z	$\overline{Q}$n	A 3–state, latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	L	H (2)	L	Z(2)	
–	–	H	H	L	L	Qn	$\overline{Q}$n	$\overline{Q}$n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3–state
l	X	L	L	H	X	l	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3–state, data from B to A
–	L	L	H	H	H	L	L	Z	
–	H	H	H	H	H	Qn	H	Z	
–	L	H	H	H	H	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3–state
l	X	L	L	X	H	l	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3–state, data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Qn	H	Z	
–	L	H	H	X	H	Qn	L	Z	

NOTES:
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. – = Input not externally driven
5. Z = High impedance (off) state
6. Q_n = High or low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition.
7. (1) = Condition will cause a feedback loop path: A to B and B to A.
8. (2) = The latch must be preconmditioned such that B inputs may assume a high or low level while $\overline{OEB}$0 and $\overline{OEB}$1 are low and $\overline{LE}$ is high.
9. H**= Goes to level of pullup voltage.
10. B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

FUNCTION TABLE FOR 74F8961

INPUTS						LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$	OEA	$\overline{OEB0}$	$\overline{OEB1}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	H**	A 3–state, data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A 3–state, latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	L	H (2)	L	Z(2)	
–	–	H	H	L	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3–state
I	X	L	L	H	X	I	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3–state, data from B to A
–	L	L	H	H	H	L	L	Z	
–	H	H	H	H	H	Qn	H	Z	
–	L	H	H	H	H	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3–state
I	X	L	L	X	H	I	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3–state, data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Qn	H	Z	
–	L	H	H	X	H	Qn	L	Z	

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_X	Threshold control		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}$, OEA, $\overline{LE}$	–0.5 to +7.0	V
		A0 – A7, B0 – B7	–0.5 to +5.5	V
I_{IN}	Input current		–40 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7	200	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
Tstg	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except B0 – B7	2.0			V
		B0 – B7	1.6			V
V_{IL}	Low–level input voltage	Except B0 – B7			0.8	V
		B0 – B7			1.475	V
I_{Ik}	Input clamp current	Except A0 – A7			–18	mA
		A0 – A7			–40	mA
I_{OH}	High–level output current	A0 – A7			–3	mA
I_{OL}	Low–level output current	A0 – A7			24	mA
		B0 – B7			100	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN.	LIMITS TYP.[2]	LIMITS MAX.	UNIT
I_{OH}	High–level output current	B0 – B7	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power–off output current	B0 – B7	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A0 – A7[4]	V_{CC} = MIN,	I_{OH} = –3mA, V_X =V_{CC}	2.5		V_{CC}	V
			V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –4mA, V_X =3.13V and 3.47V	2.5			V
V_{OL}	Low-level output voltage	A0 – A7[4]	V_{CC} = MIN,	I_{OL} = 20mA, V_X = V_{CC}			0.50	V
		B0 – B78	V_{IL} = MAX	I_{OL} = 100mA			1.15	V
			V_{IH} = MIN	I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 7.0V				100	µA
		A0–A7, B0 – B7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V				20	µA
		B0–B7	V_{CC} = MAX, V_I = 2.1V, Bn – An = 0V				100	µA
I_{IL}	Low–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				–20	µA
		B0 – B7	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{OZH} + I_{IH}	Off–state output current, high–level current applied	A0 – A7	V_{CC} = MAX, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied	A0 – A7	V_{CC} = MAX, V_I = 0.5V				–70	µA
I_X	High–level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}$n = 2.7V, A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–100		100	µA
			V_{CC} = MAX, V_X = 3.13 & 3.47V, $\overline{LE}$ = OEA = $\overline{OEB}$n = A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–10		10	µA
I_{OS}	Short circuit output current[3]	A0–A7 only 74F8960	V_{CC} = MAX, Bn = 1.3V, OEA = 2.0V, $\overline{OEB}$n = 2.7V		-60		-150	mA
		A0–A7 only 74F8961	V_{CC} = MAX, Bn = 1.8V, OEA = 2.0V, $\overline{OEB}$n = 2.7V					
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}				75	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8v and V_{IL} = 1.3V.

AC ELECTRICAL CHARACTERISTICS FOR 74F8960

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50p, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1, 2	4.5 6.0	6.0 10.0	8.5 13.5	3.5 7.5	9.5 14.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 4 Waveform 5	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.5	15.0 16.0	ns
t_{PHZ} t_{PLZ}	Output enable time from high or low, OEA to An	Waveform 4 Waveform 5	2.0 2.0	3.5 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 50pF, R_U = 9Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D = 50pF, R_L = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1, 2	3.5 3.5	5.5 5.0	8.0 8.0	2.0 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Bn	Waveform 1, 2	3.5 4.0	5.5 6.5	8.5 9.0	2.5 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Output enable/disable time $\overline{OEB}$n to Bn	Waveform 1, 2	2.5 3.5	4.5 5.5	7.5 8.5	1.5 3.5	8.0 9.0	ns
t_{TLH} t_{THL}	Transition time, Bn port 1.3V to 1.7V, 1.7V to 1.3V	Test circuit and waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 6.0	ns

AC SETUP REQUIREMENTS FOR 74F8960

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su}(H) t_{su}(L)	Setup time, high or low An to $\overline{LE}$	Waveform 3	5.0 3.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, high or low An to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
t_w(L)	$\overline{LE}$ pulse width, low	Waveform 3	4.5			5.0		ns

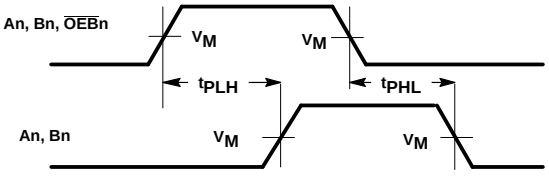
AC ELECTRICAL CHARACTERISTICS FOR 74F8961

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50p, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1, 2	5.5 4.5	8.0 6.0	12.0 9.0	5.5 4.5	12.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 4 Waveform 5	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.0	15.0 15.5	ns
t_{PHZ} t_{PLZ}	Output enable time from high or low, OEA to An	Waveform 4 Waveform 5	2.0 2.0	3.5 4.5	6.0 7.0	1.5 2.0	6.5 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 50pF, R_U = 9Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D = 50pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1, 2	3.0 3.0	5.0 4.5	7.0 7.5	2.5 2.5	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Bn	Waveform 1, 2	3.5 3.5	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Output enable/disable time $\overline{OEB}$n to Bn	Waveform 1, 2	3.0 3.5	4.5 5.5	7.0 9.0	2.5 3.5	8.0 10.0	ns
t_{TLH} t_{THL}	Transition time, Bn port 1.3V to 1.7V, 1.7V to 1.3V	Test circuit and waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 4.5	ns

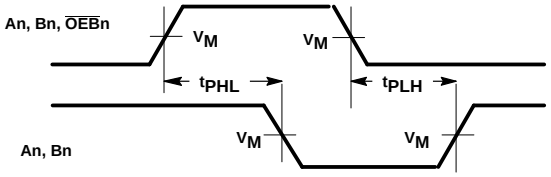
AC SETUP REQUIREMENTS FOR 74F8961

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su}(H) t_{su}(L)	Setup time, high or low An to $\overline{LE}$	Waveform 3	3.5 4.5			4.5 5.0		ns
t_h(H) t_h(L)	Hold time, high or low An to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
t_w(L)	$\overline{LE}$ pulse width, low	Waveform 3	4.0			5.0		ns

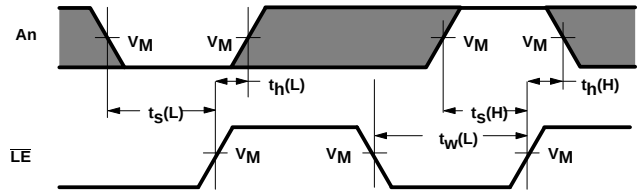
AC WAVEFORMS



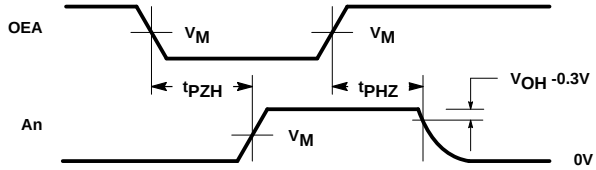
Waveform 1. Propagation delay for data to output



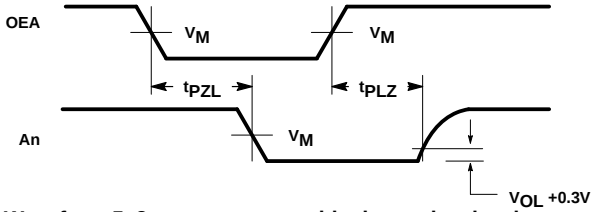
Waveform 2. Propagation delay for data to output



Waveform 3. Data setup and hold times and $\overline{LE}$ pulse width



Waveform 4. 3–state output enable time to high level and output disable time from high level



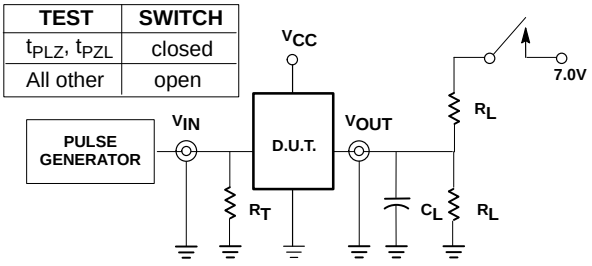
Waveform 5. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

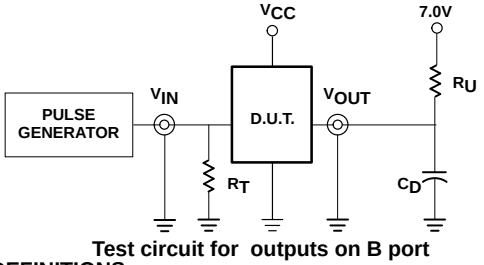
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

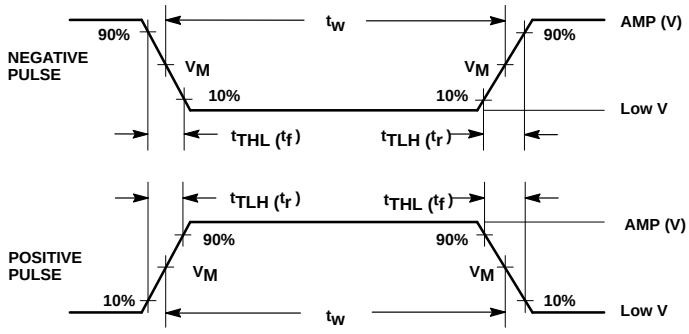
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on A port



Test circuit for outputs on B port



Input pulse definition

family 74F	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	3.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.