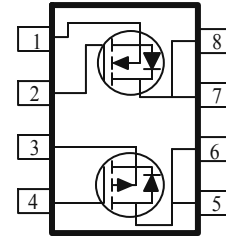


P & N-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
40	104 @ $V_{GS} = 4.5V$	3.7
	89 @ $V_{GS} = 10V$	4.0
-40	106 @ $V_{GS} = -4.5V$	-3.7
	69 @ $V_{GS} = -10V$	-4.6

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter			Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage			V _{DS}	40	-40	V
Gate-Source Voltage			V _{GS}	20	-20	
Continuous Drain Current ^a	T _A =25°C		I _D	4.0	-4.6	A
	T _A =70°C			3.3	-3.7	
Pulsed Drain Current ^b			I _{DM}	±50	±50	
Continuous Source Current (Diode Conduction) ^a			I _S	2.3	-2.1	A
Power Dissipation ^a	T _A =25°C		P _D	2.1	2.1	W
	T _A =70°C			1.3	1.3	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
	Steady-State		110	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits				Unit	
			Ch	Min	Typ	Max		
Static								
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	1			V	
		V _{GS} = V _{DS} , I _D = -250 uA	P	-1				
Gate-Body Leakage	I _{GSS}	V _{GS} = -20 V, V _{DS} = 0 V	P			±100	nA	
		V _{GS} = 20 V, V _{DS} = 0 V	N			±100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -32 V, V _{GS} = 0 V	P			-1	uA	
		V _{DS} = 32 V, V _{GS} = 0 V	N			1		
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	25			A	
		V _{DS} = -5 V, V _{GS} = -10 V	P	-45				
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.0 A	N			89	mΩ	
		V _{GS} = 4.5 V, I _D = 3.7 A				104		
		V _{GS} = -10 V, I _D = -4.6 A	P			69		
		V _{GS} = -4.5 V, I _D = -3.7 A				106		
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 7.8 A	N		40		S	
		V _{DS} = -15 V, I _D = -6.9 A	P		31			
Dynamic								
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =7.8A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-6.9A	N		3.6		nC	
Gate-Source Charge	Q _{gs}		P		13			
			N		1.8			
			P		5.8			
Gate-Drain Charge	Q _{gd}	N		1.3				
		P		12				
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =10V, I _D =1A , R _{GEN} =25Ω, P-Channel V _{DD} =-15V, V _{GS} =-10V, I _D =-1A R _{GEN} =15Ω	N		20		nS	
Rise Time	t _r		P		15			
			N		9			
			P		16			
Turn-Off Delay Time	t _{d(off)}		N		70			
			P		62			
Fall-Time	t _f		N		20			
			P		46			

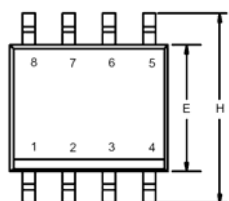
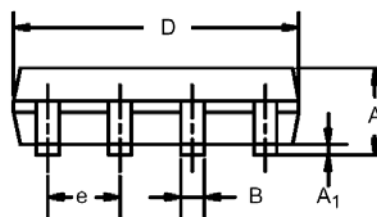
Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

