UPIO-M3U1xx I/O CARD USER'S GUIDE

1. Introduction

The Unified Development Platform (UDP) provides a development and demonstration platform for Silicon Laboratories microcontrollers, short-range wireless devices, and software tools, including the Silicon Laboratories Integrated Development Environment (IDE).

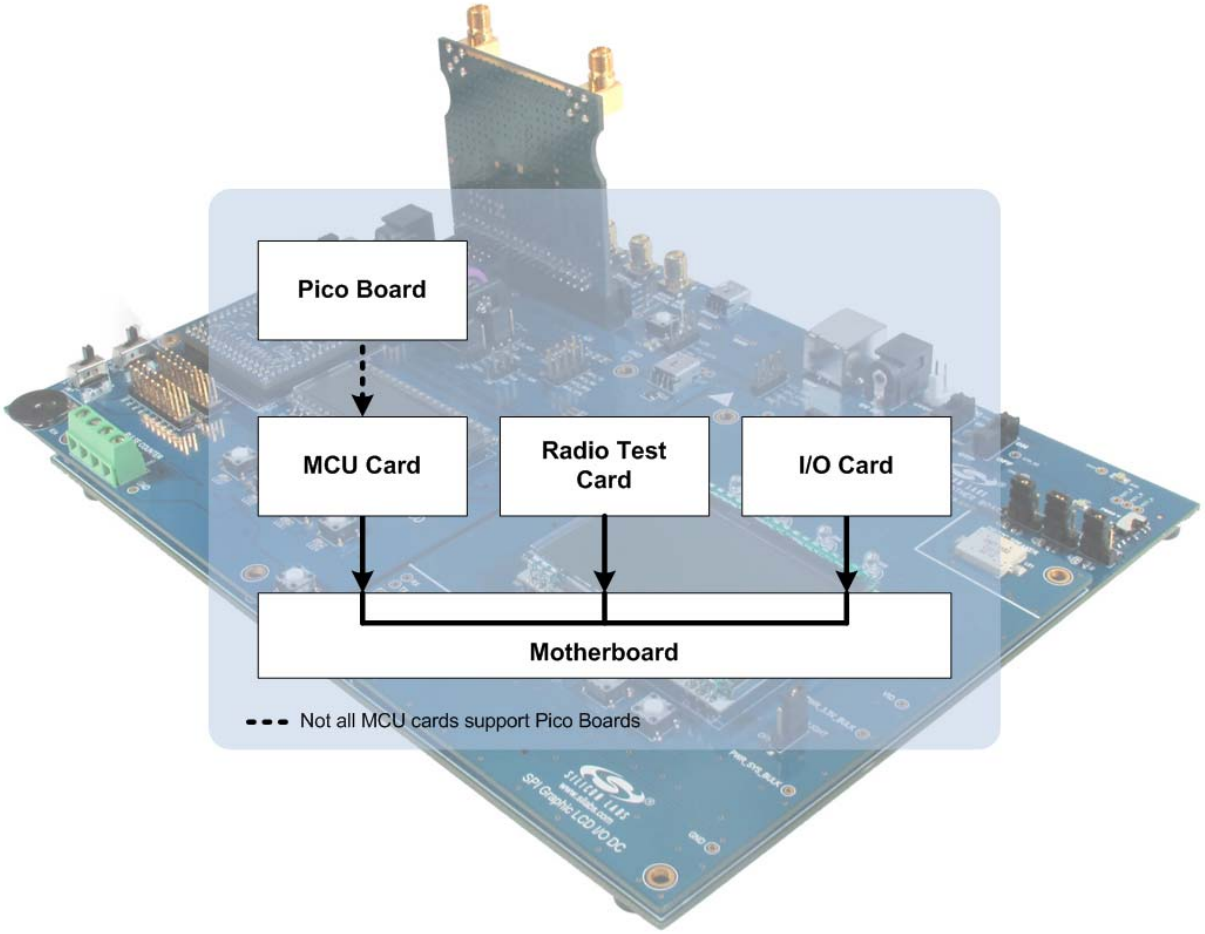


Figure 1. Unified Development Platform Block Diagram

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2. Relevant Documents

This document provides a hardware overview for the Unified Development Platform (UDP) system SiM3U1xx I/O card. Additional information on the UDP system can be found in the documents listed in this section.

2.1. Motherboard User's Guide

The UDP Motherboard User's Guide contains information on the motherboard features and can be found at www.silabs.com/udp.

2.2. Card User's Guides

The UDP MCU, I/O, and radio test card User's Guides can be found at www.silabs.com/udp.

3. Hardware Setup

Refer to Figure 2 for a diagram of the hardware configuration

1. Connect an MCU card to the UDP motherboard slot.
2. Connect the I/O card to the UDP motherboard slot.
3. (Optional) Connect a radio test card to the radio test card slot in the UDP motherboard.
4. (Optional) Connect an EZLink card to the EZLink card slot in the UDP motherboard.
5. Connect the USB Debug Adapter to the 2x5 debug connector on the MCU card with the 10-pin ribbon cable.
6. Connect one end of the USB cable to the USB connector on the USB Debug Adapter.
7. Connect the other end of the USB cable to a USB Port on the PC.
8. Connect the ac/dc power adapter to power jack J20 on the UDP motherboard. The board can also be powered from the J16 USB or J1 mini USB connectors.
9. Move the S3 power switch on the UDP motherboard to the ON position.

Notes:

- Use the Reset button in the IDE to reset the target when connected using a USB Debug Adapter.
- Remove power from the target board and the USB Debug Adapter before connecting or disconnecting the ribbon cable from the target board. Connecting or disconnecting the cable when the devices have power can damage the device and/or the USB Debug Adapter.
- The MCU card can be used alone without the motherboard. However, the motherboard must be powered if an MCU card is connected.

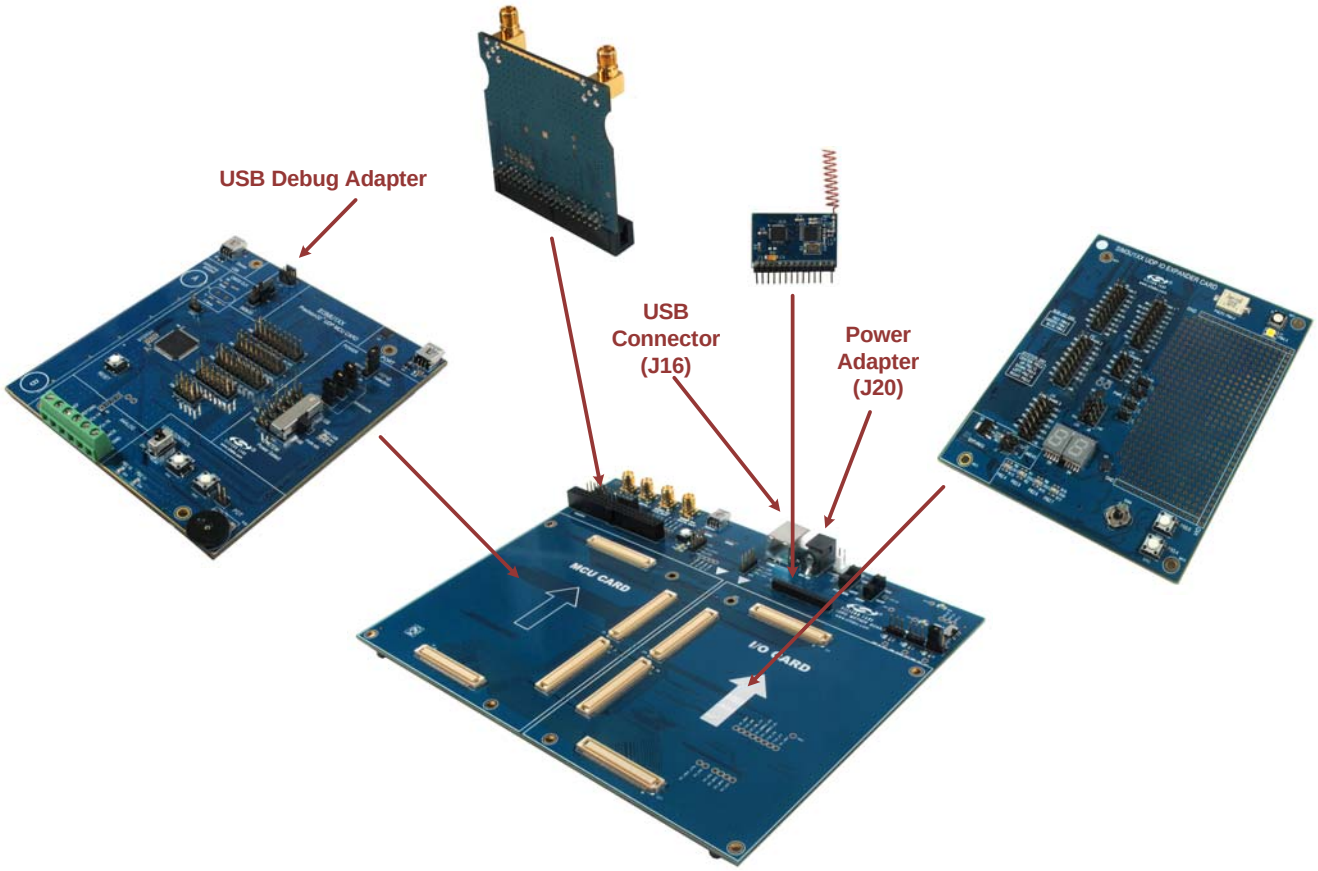


Figure 2. Hardware Setup using the Unified Development Platform

4. UPIO-M3U1xx I/O Card Overview

The SiM3U1xx I/O card expands the development hardware of the SiM3U1xx or SiM3C1xx devices. The card connects to the I/O Card expansion slot on the UDP motherboard and provides complete access to the MCU resources. Each expansion board has a unique ID that can be read out of an EEPROM or MCU on the board, which enables software tools to recognize the connected hardware and automatically select the appropriate firmware image.

Figure 3 shows the SiM3U1xx I/O card.

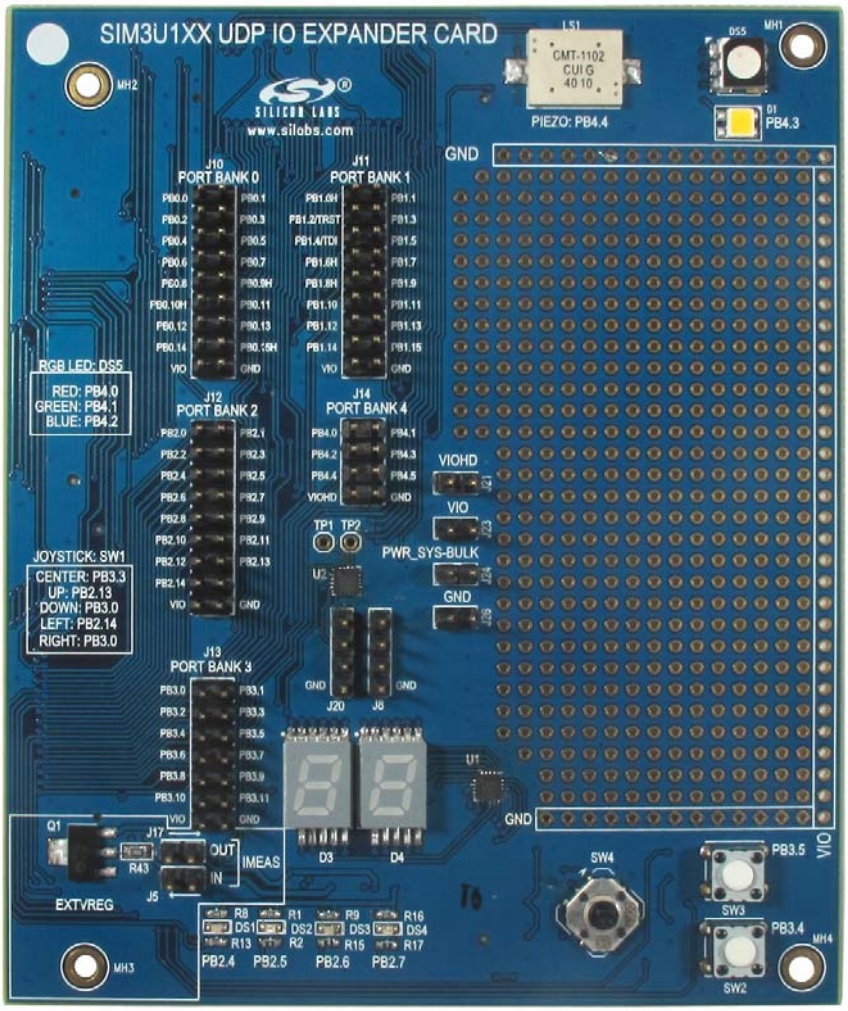


Figure 3. UPIO-M3U1xx I/O Card

Figure 4 highlights some of the features of the SiM3U1xx I/O card.

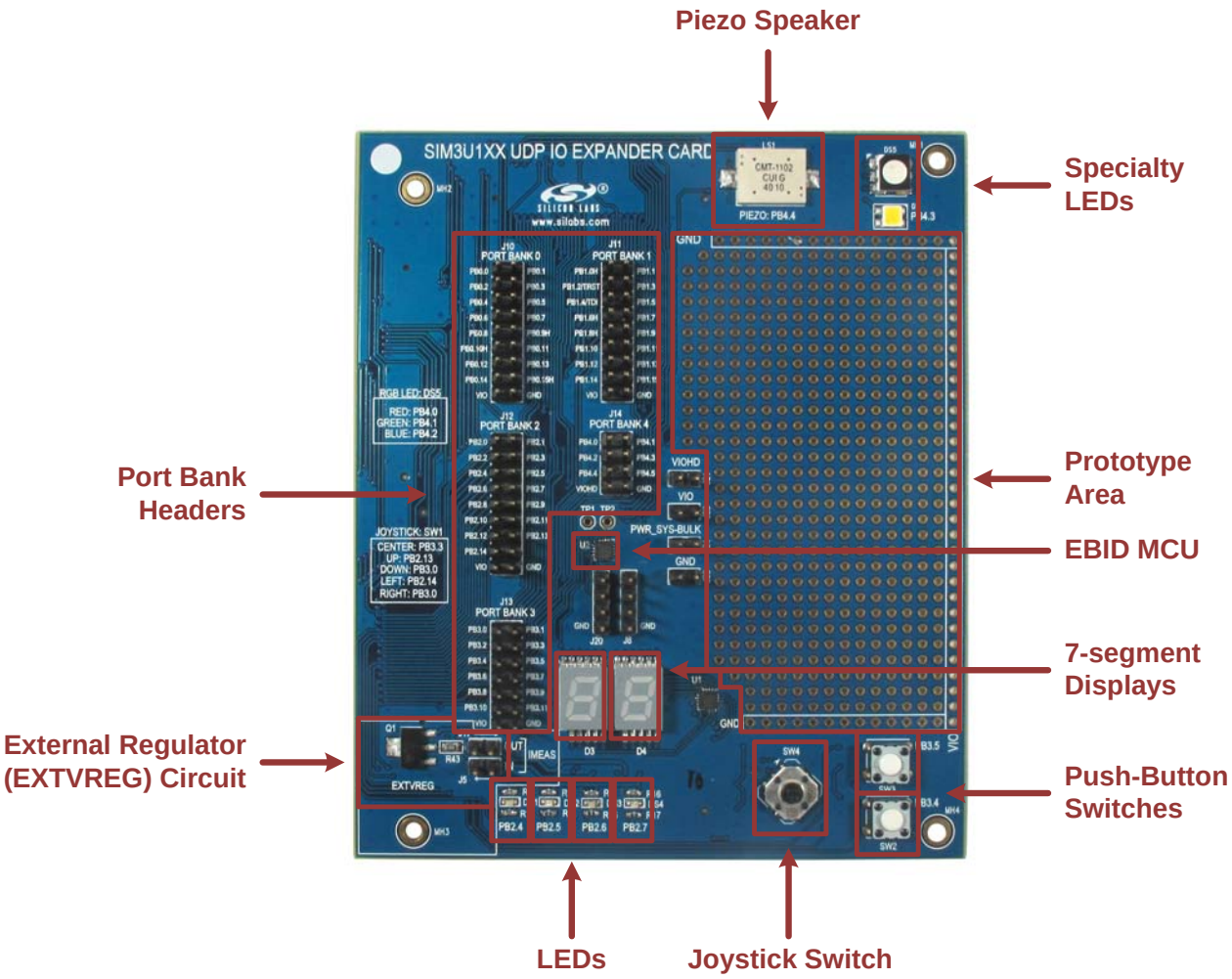


Figure 4. UPIO-M3U1xx I/O Card Features

4.1. 7-Segment Displays

The I/O card has two 7-segment displays driven by a Silicon Labs C8051F990 MCU. The C8051F990 is powered by the UDP motherboard and communicates to a UDP MCU card via I2C through the UDP connector.

Debug connections to the C8051F990 are available via the J8 header. Table 2 shows the header connections.

Table 1. J8 Header Connections

J8 Pin Number	J8 Pin Description
1	C8051F990 VDD pin (PWR_SYS_BULK)
2	C8051F990 C2CK
3	C8051F990 C2D
4	GND

4.2. Switches and LEDs

The I/O card has two push-button switches (SW2 and SW3) and six LEDs (DS1-5 and D1). The switches are normally open and pull the port pin voltage to ground when pressed. DS5 integrates a red, green and blue LED into a single component. D1 is a bright white LED. Table 2 shows the port pin connections.

Table 2. Switch and LED Connections

SW or LED	GPIO Pin
Push-Button Switch (SW2)	PB3.4
Push-Button Switch (SW3)	PB3.4
Red LED (DS1)	PB2.4
Yellow LED (DS2)	PB2.5
Green LED (DS3)	PB2.6
Blue LED (DS4)	PB2.7
Red LED (DS5)	PB4.0
Green LED (DS5)	PB4.1
Blue LED (DS5)	PB4.2
Bright White LED (DS6)	PB4.3

4.3. Joystick Switch

The I/O card has five-position joystick switch (SW1). The joystick is normally open and pulls a port pin voltage to ground when the joystick placed in one of the five positions. Table 3 show the port pin connections to the joystick.

Table 3. Joystick Switch Connections

Joystick Position	GPIO Pin
Center	PB3.3
Up	PB2.13
Down	PB3.0
Left	PB2.14
Right	PB3.1

4.4. Piezo Buzzer

The I/O card has a piezo buzzer (LS1) connected to PB4.4 that resonates audibly when the voltage input is toggled periodically.

4.5. External Regulator Circuit

The I/O card has a BJT transistor connected to four port pins to implement a regulator circuit with the SiM3U1xx EXTVREG module. The positive supply to the circuit can be 5 V from the UDP motherboard or PB3.8. PB3.9 connects to the negative supply and the collector of the BJT. The positive and negative supply are used to create a voltage drop across R42 to regulate the collector current.

PB3.10 is connected to the output of the regulator circuit and the emitter of the BJT. PB3.11 is connected the base of the BJT and enables and disables the regulator circuit.

4.6. EBID MCU

The I/O card has a unique ID that can be read out from the Silicon Labs C8051F990 MCU (U2). This MCU enables software tools to recognize the connected hardware and automatically select the appropriate firmware image.

5. Using the I/O Card with the UDP Motherboard

5.1. Current Measurement

The power measurement circuitry on the UDP motherboard consists of a Silicon Labs C8051F351 8051 MCU that measures both input voltage and current consumption of the MCU card, I/O expander, and radio test card. When using the I/O card, install a shorting block on the UDP Motherboard J15 and J13 connecting the two left pins together.

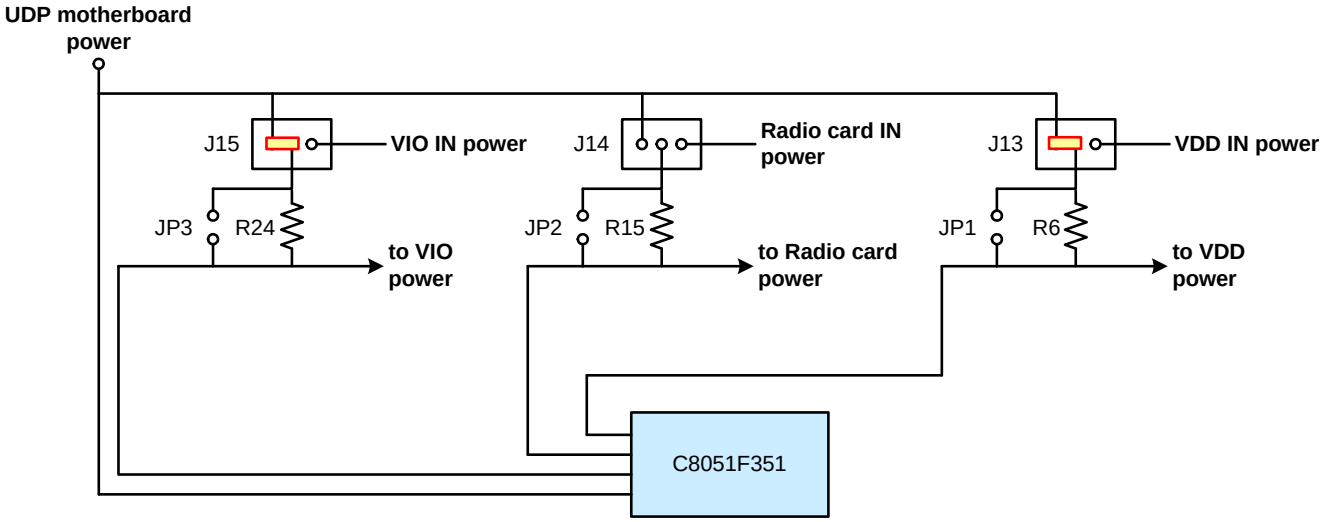


Figure 5. Power Measurement Diagram

5.2. I/O Card Header Connections

The I/O card has four connectors with 100 pins each. These 400 pins are directly tied to the UDP motherboard and MCU cards. These signals are named and designed to support a wide variety of features and applications, and the UPIO-M3U1xx card implements a subset of these connections.

The MCU cards and I/O cards are designed so that a maximum number of functions are shared between each card. This allows a particular type of I/O card to be shared amongst all MCU cards that connect to the same signals.

The I/O card slot includes the following components:

J1	MCU card connector H1
J2	MCU card connector H2
J3	MCU card connector H3
J4	MCU card connector H4

The UPIO-M3U1xx card implements the signals described in Table 5, Table 6, and Table 7, Table 8 in the Appendix.

5.3. Shorting Blocks: Factory Defaults

The UPIO-M3U1xx I/O Card has a factory pre-installed shorting block on J5. Figure 6 shows the position of the factory default shorting block.

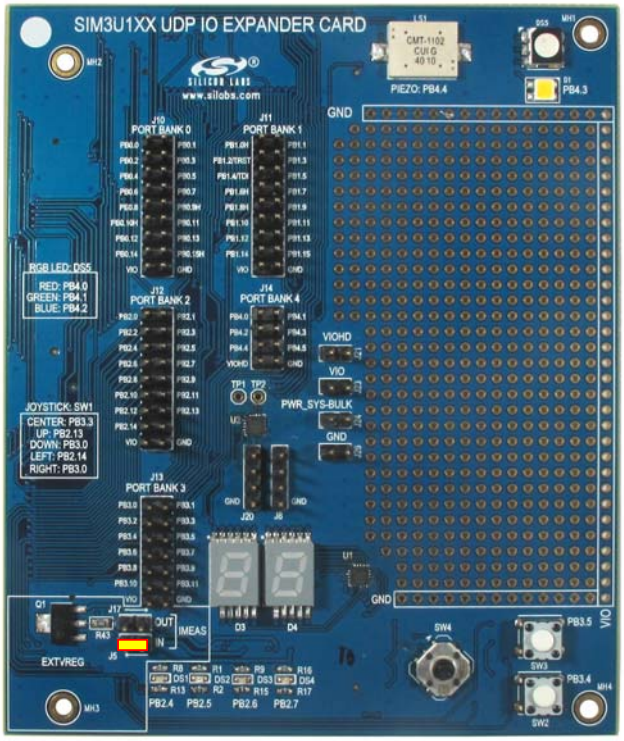


Figure 6. Shorting Blocks: Factory Defaults

6. Schematics

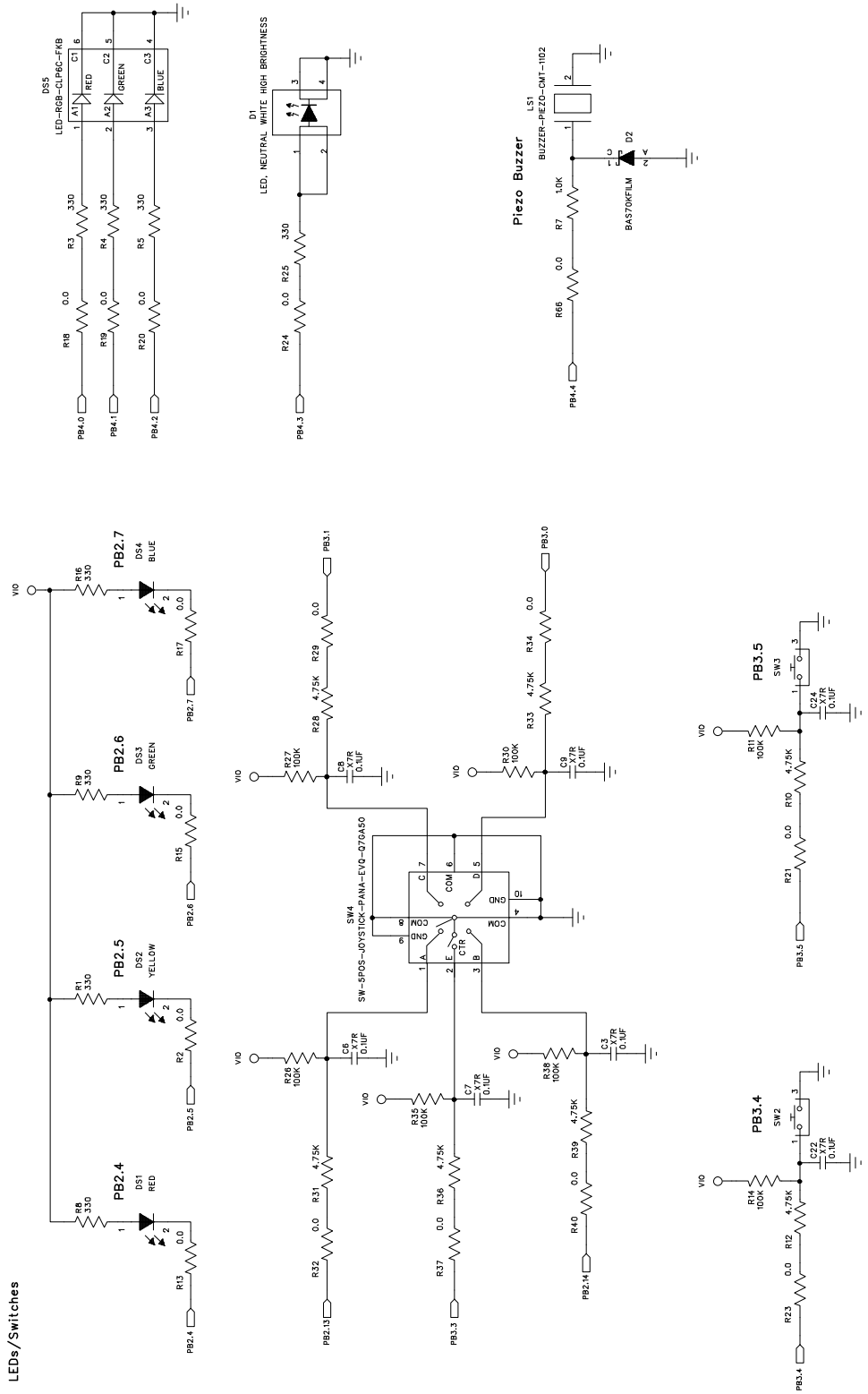


Figure 7. UPIO-M3U1xx I/O Card Schematic (1 of 4)

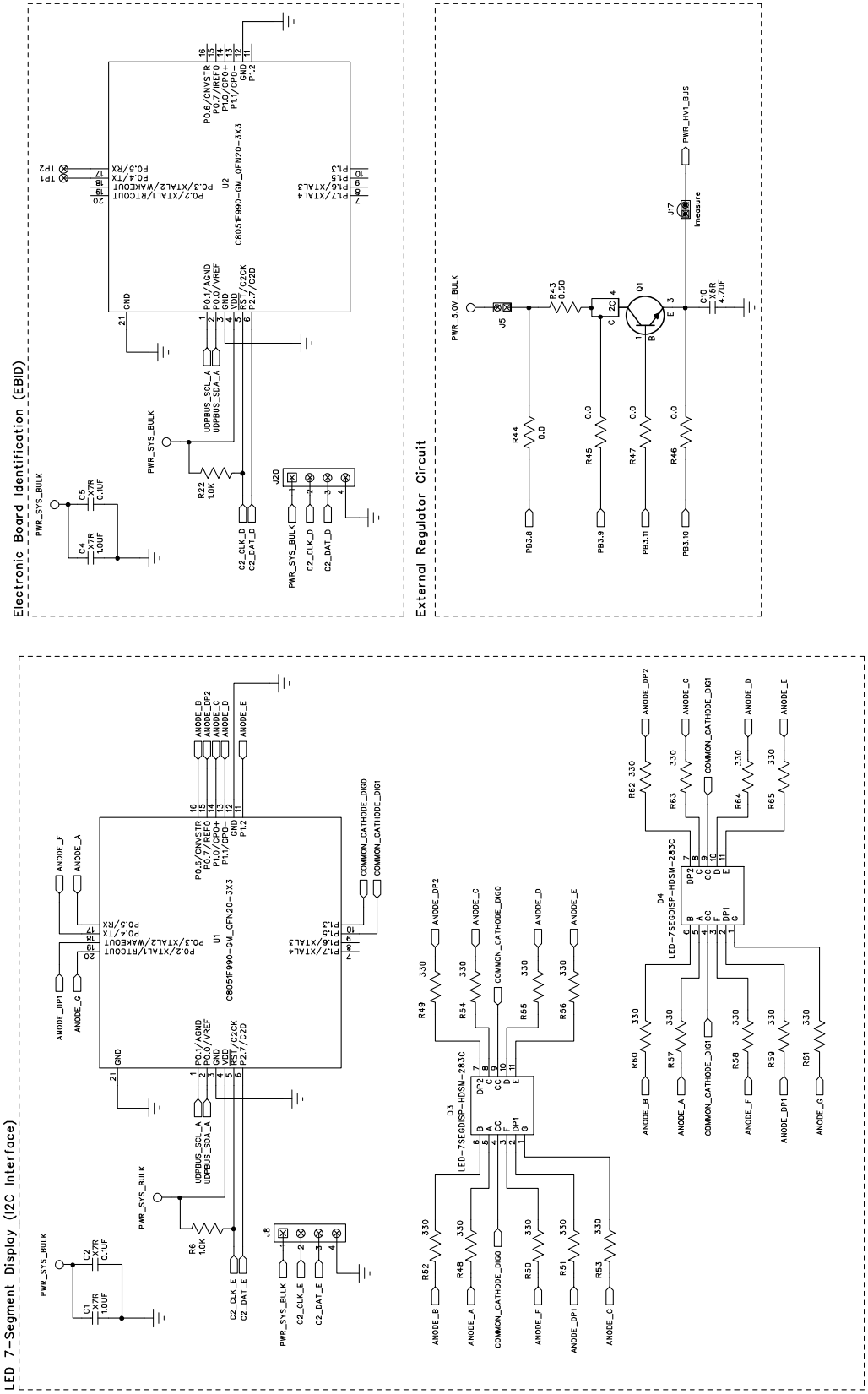


Figure 8. UPIO-M3U1xx I/O Card Schematic (2 of 4)

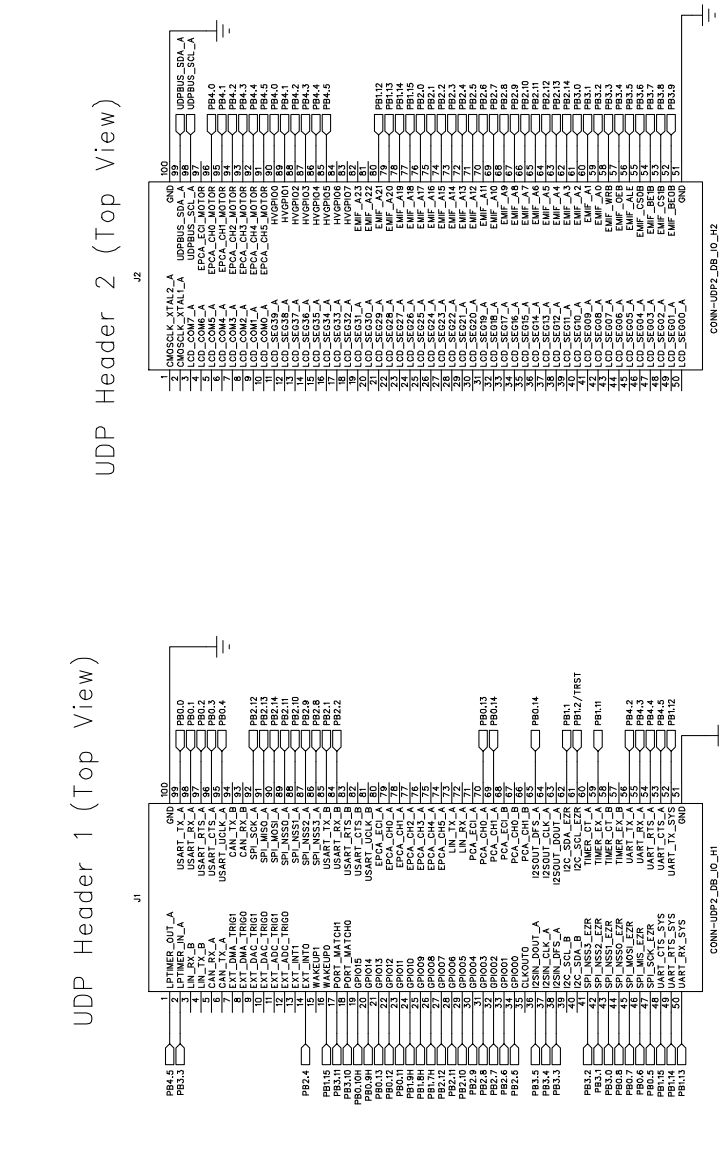


Figure 9. UPIO-M3U1xx I/O Card Schematic (3 of 4)

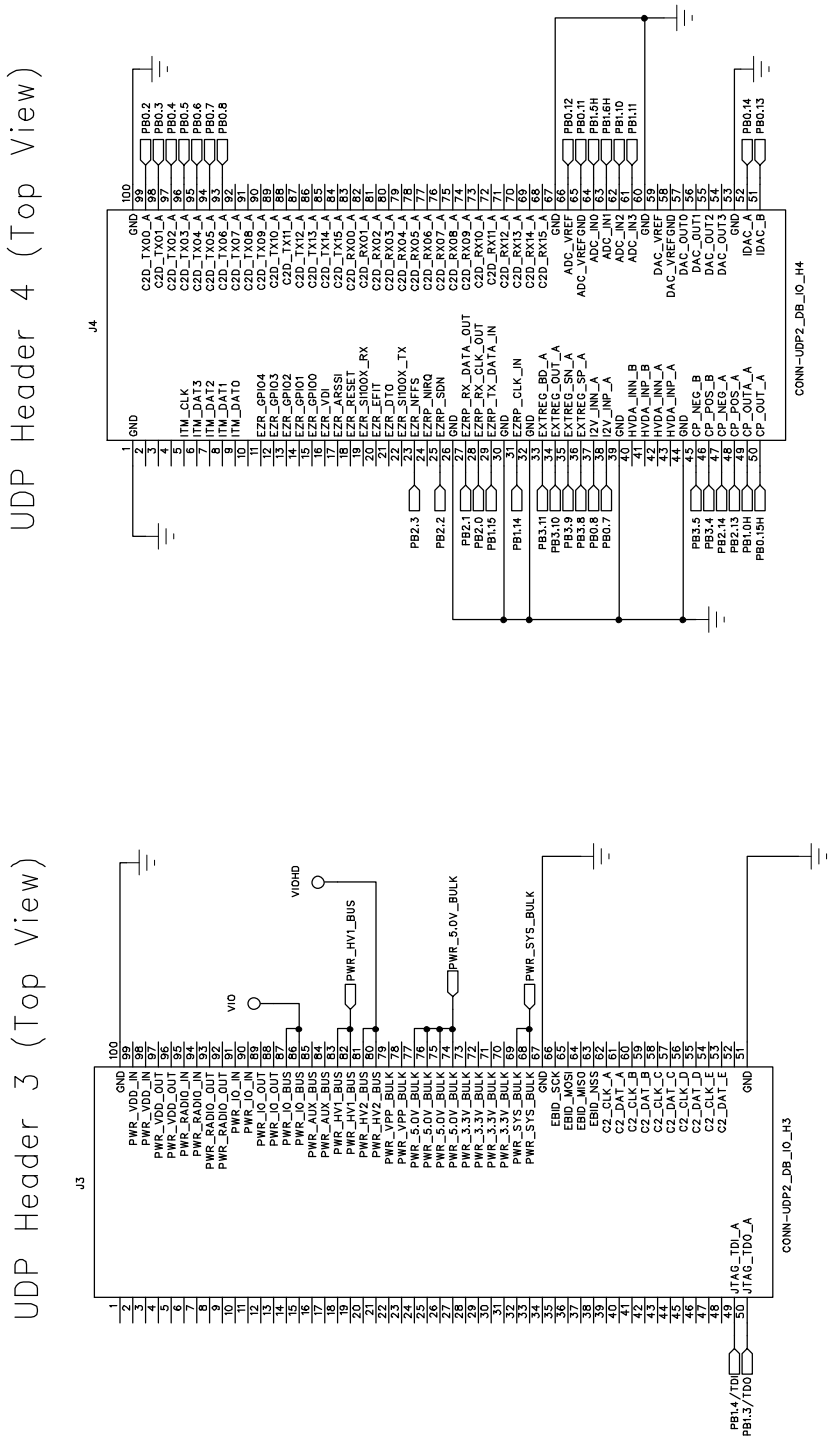


Figure 10. UPIO-M3U1xx I/O Card Schematic (4 of 4)

7. Bill of Materials

Table 4. UPIO-M3U1xx Card Bill of Materials

Reference	Part Number	Source	Description
LS1	CMT-1102	CUI Inc	BUZZER, PIEZO, 25V(max), 4.1KHZ, SMD, RoHS
U1-2	C8051F990-GM	Silicon Labs	MIXED SIGNAL, MCU, QFN20-3X3, RoHS.
C2-3 C5-9 C22 C24	C0603C104J3RACTU	Kemet	CAP, 0.1UF, X7R, CERAMIC, 0603, 25V, ±5%, OR EQ, RoHS
C1 C4	C1608X7R1C105K	TDK Corporation	CAP CERAMIC, 1.0UF, X7R, 0603, 16V, ±10%, OR EQ, RoHS
C10	ECJ-1VB0J475M	Panasonic ECG	CAP, 4.7UF, X5R, CERAMIC, 0603, 6.3V, ±20%, OR EQ, RoHS
J1 J2 J3 J4	FX8-100P-SV1(91)	Hirose Electric Co Ltd	CONN, HDR, 100POS, 0.6MM, GOLD, SMD, RoHS
D2	BAS70KFILM	STMicroelectronics	DIODE SCHOTTKY, SS SGL SOD-523, RoHS
J5 J17 J21 J23 J24 J26	PBC02SAAN	Sullins Connector Solutions	STAKE HEADER, 1X2, 0.1"CTR, GOLD, OR EQ, RoHS
J8 J20	PBC04SAAN	Sullins Connector Solutions	STAKE HEADER, 1X4, 0.1" CTRS, OR EQ, RoHS
J14	PBC04DAAN	Sullins Connector Solutions	STAKE HEADER, 2X4, 0.1"CTR, OR EQ, RoHS
J13	PBC07DAAN	Sullins Connector Solutions	STAKE HEADER, 2X7, 0.1" CTR, GOLD, OR EQ, RoHS
J10 J11 J12	PBC09DAAN	Sullins Connector Solutions	STAKE HEADER, 2X9, 0.1' CTR, GOLD, OR EQ, RoHS
D3-4	HDSM-283C	Avago Technologies	LED, 7SEG DISP COMMON CATHODE, 0.28" SMD, RED OR EQ, RoHS
DS4	LTST-C190TBKT	Lite-On Inc	LED 468NM, BLUE, SMT0603, OR EQ, RoHS
DS3	SML-LX0603GW-TR	Lumex Opto/Components Inc	LED, 565NM, GREEN DIFF, SMT0603, OR EQ, RoHS
D1	MLEAWT-A1-R250-0003E5	Cree Inc	LED, NEUTRAL WHITE HIGH BRIGHT-NESS
DS1	SML-LX0603IW-TR	Lumex Opto/Components Inc	LED, RED DIFF, 635NM, SMT0603, OR EQ, RoHS
DS2	LTST-C190YK	Lite-On Inc	LED, YELLOW CLEAR, SMT0603, OR EQ, RoHS
DS5	CLP6C-FKB-CM1Q1H1BB7R3R3	Cree Inc	DIODE, RGB LED, 6-PLCC
R2 R13 R15 R17-21 R23-24 R29 R32 R34 R37 R40 R44-47 R66	RC0603JR-070RL	Yageo	RES, 0.0, SMT, 0603, 1/10W, ±5%, OR EQ, RoHS
R43	WSL2010R5000FEA18	Vishay/Dale	RES, 0.05 OHM, 2010, 1W, ±1%, OR EQ, RoHS

Table 4. UPIO-M3U1xx Card Bill of Materials (Continued)

Reference	Part Number	Source	Description
R11 R14 R26-27 R30 R35 R38	ERJ-3EKF1003V	Panasonic ECG	RES, 100K, SMT, 0603, 1/10W, ±1%, OR EQ, RoHS
R6-7 R22	RC0603JR-071KL	Yageo	RES, 1.0K OHM, SMT, 0603, 0W, ±5%, RoHS
R1 R3-5 R8-9 R16 R25 R48-65	RT0603DRD07330R	Yageo	RES, 330, SMT, 0603, 1/10W, ±0.5%, OR EQ, RoHS
R10 R12 R28 R31 R33 R36 R39	ERJ-3EKF4751V	Panasonic ECG	RES, 4.75K OHM, SMT, 0603, 1/10W, ±1%, OR EQ, RoHS
SW4	EVQ-Q7GA50	Panasonic ECG	5POS SPST JOYSTICK
SW2-3	EVQ-PAD04M	Panasonic ECG	SWITCH, LIGHT TOUCH, 130GF, 6MM SQ, RoHS
Q1	STN724	STMicroelectronics	TRANS, NPN, SW 3A, 30V, SOT223, STF724, RoHS

APPENDIX—PIN DESCRIPTIONS

Table 5. UPIO-M3U1xx Card H1 Pin Descriptions (J1)

I/O Card Pin	Signal Name	Description
1	LPTIMER_OUT_A	PB4.5 header
2	LPTIMER_IN_A	PB3.3 header
3	LIN_RX_B	
4	LIN_TX_B	
5	CAN_RX_A	
6	CAN_TX_A	
7	EXT_DMA_TRIG1	
8	EXT_DMA_TRIG0	
9	EXT_DAC_TRIG1	
10	EXT_DAC_TRIG0	
11	EXT_ADC_TRIG1	
12	EXT_ADC_TRIG0	
13	EXT_INT1	
14	EXT_INT0	PB2.4 header/Red DS1 LED
15	WAKEUP1	
16	WAKEUP0	PB1.15 header
17	PORT_MATCH1	PB3.11/External Voltage Regulator base drive output
18	PORT_MATCH0	PB3.10/External Voltage Regulator OUT output
19	GPIO15	PB0.10H header
20	GPIO14	PB0.9H header
21	GPIO13	PB0.13 header
22	GPIO12	PB0.12 header
23	GPIO11	PB0.11 header
24	GPIO10	PB1.9H header
25	GPIO09	PB1.8H header
26	GPIO08	PB1.7H header
27	GPIO07	PB2.12 header
28	GPIO06	PB2.11 header
29	GPIO05	PB2.10 header
30	GPIO04	PB2.9 header
31	GPIO03	PB2.8 header
32	GPIO02	PB2.7 header/Blue DS4 LED
33	GPIO01	PB2.6 header/Green DS3 LED
34	GPIO00	PB2.5 header/Yellow DS2 LED

Table 5. UPIO-M3U1xx Card H1 Pin Descriptions (J1) (Continued)

I/O Card Pin	Signal Name	Description
35	CLKOUT0	
36	I2SIN_DOUT_A	PB3.5 header
37	I2SIN_CLK_A	PB3.4 header
38	I2SIN_DFS_A	PB3.3 header
39	I2C_SCL_B	
40	I2C_SDA_B	
41	SPI_NSS3_EZR	PB3.2 header
42	SPI_NSS2_EZR	PB3.1 header
43	SPI_NSS1_EZR	PB3.0 header
44	SPI_NSS0_EZR	PB0.8 header
45	SPI_MOSI_EZR	PB0.7 header
46	SPI_MISO_EZR	PB0.6 header
47	SPI_SCK_EZR	PB0.5 header
48	UART_CTS_SYS	PB1.15 header
49	UART_RTS_SYS	PB1.14 header
50	UART_RX_SYS	PB1.13 header
51	GND	
52	UART_TX_SYS	PB1.12 header
53	UART_CTS_A	PB4.5 header
54	UART_RTS_A	PB4.4 header
55	UART_RX_A	PB4.3 header
56	UART_TX_A	PB4.2 header
57	TIMER_EX_B	
58	TIMER_CT_B	
59	TIMER_EX_A	PB1.11 header
60	TIMER_CT_A	
61	I2C_SCL_EZR	PB1.2/TRST header
62	I2C_SDA_EZR	PB1.1 header
63	I2SOUT_DOUT_A	
64	I2SOUT_CLK_A	
65	I2SOUT_DFS_A	PB0.14 header
66	PCA_CH1_B	
67	PCA_CH0_B	
68	PCA_ECI_B	
69	PCA_CH1_A	PB0.14 header
70	PCA_CH0_A	PB0.13 header
71	PCA_ECI_A	

Table 5. UPIO-M3U1xx Card H1 Pin Descriptions (J1) (Continued)

I/O Card Pin	Signal Name	Description
72	LIN_RX_A	
73	LIN_TX_A	
74	EPCA_CH5_A	
75	EPCA_CH4_A	
76	EPCA_CH3_A	
77	EPCA_CH2_A	
78	EPCA_CH1_A	
79	EPCA_CH0_A	
80	EPCA_ECI_A	
81	USART_UCLK_B	
82	USART_CTS_B	
83	USART_RTS_B	
84	USART_RX_B	PB2.2 header
85	USART_TX_B	PB2.1 header
86	SPI_NSS3_A	PB2.8 header
87	SPI_NSS2_A	PB2.9 header
88	SPI_NSS1_A	PB2.10 header
89	SPI_NSS0_A	PB2.11 header
90	SPI_MOSI_A	PB2.14/Joystick left
91	SPI_MISO_A	PB2.13/Joystick up
92	SPI_SCK_A	PB2.12 header
93	CAN_RX_B	
94	CAN_TX_B	
95	USART_UCLK_A	PB0.4 header
96	USART_CTS_A	PB0.3 header
P	USART_RTS_A	PB0.2 header
98	USART_RX_A	PB0.1 header
99	USART_TX_A	PB0.0 header
100	GND	

Table 6. UPIO-M3U1xx Card H2 Pin Descriptions (J2)

I/O Card Pin	Signal Name	Description
1	CMOSCLK_XTAL2_A	
2	CMOSCLK_XTAL1_A	
3	LCD_COM7_A	
4	LCD_COM6_A	
5	LCD_COM5_A	
6	LCD_COM4_A	
7	LCD_COM3_A	
8	LCD_COM2_A	
9	LCD_COM1_A	
10	LCD_COM0_A	
11	LCD_SEG39_A	
12	LCD_SEG38_A	
13	LCD_SEG37_A	
14	LCD_SEG36_A	
15	LCD_SEG35_A	
16	LCD_SEG34_A	
17	LCD_SEG33_A	
18	LCD_SEG32_A	
19	LCD_SEG31_A	
20	LCD_SEG30_A	
21	LCD_SEG29_A	
22	LCD_SEG28_A	
23	LCD_SEG27_A	
24	LCD_SEG26_A	
25	LCD_SEG25_A	
26	LCD_SEG24_A	
27	LCD_SEG23_A	
28	LCD_SEG22_A	
29	LCD_SEG21_A	
30	LCD_SEG20_A	
31	LCD_SEG19_A	
32	LCD_SEG18_A	
33	LCD_SEG17_A	
34	LCD_SEG16_A	
35	LCD_SEG15_A	
36	LCD_SEG14_A	
37	LCD_SEG13_A	

Table 6. UPIO-M3U1xx Card H2 Pin Descriptions (J2) (Continued)

I/O Card Pin	Signal Name	Description
38	LCD_SEG12_A	
39	LCD_SEG11_A	
40	LCD_SEG10_A	
41	LCD_SEG09_A	
42	LCD_SEG08_A	
43	LCD_SEG07_A	
44	LCD_SEG06_A	
45	LCD_SEG05_A	
46	LCD_SEG04_A	
47	LCD_SEG03_A	
48	LCD_SEG02_A	
49	LCD_SEG01_A	
50	LCD_SEG00_A	
51	GND	
52	EMIF_BE0B	PB3.9 header/External regulator circuit collector
53	EMIF_CS1B	PB3.8 header/External regulator circuit supply
54	EMIF_BE1B	PB3.7 header
55	EMIF_CS0B	PB3.6 header
56	EMIF_ALE	PB3.5 header
57	EMIF_OEB	PB3.4 header
58	EMIF_WRB	PB3.3 header
59	EMIF_A0	PB3.2 header
60	EMIF_A1	PB3.1 header/Joystick right
61	EMIF_A2	PB3.0 header/Joystick down
62	EMIF_A3	PB2.14 header
63	EMIF_A4	PB2.13 header
64	EMIF_A5	PB2.12 header
65	EMIF_A6	PB2.11 header
66	EMIF_A7	PB2.10 header
67	EMIF_A8	PB2.9 header
68	EMIF_A9	PB2.8 header
69	EMIF_A10	PB2.7 header
70	EMIF_A11	PB2.6 header
71	EMIF_A12	PB2.5 header
72	EMIF_A13	PB2.4 header
73	EMIF_A14	PB2.3 header
74	EMIF_A15	PB2.2 header

Table 6. UPIO-M3U1xx Card H2 Pin Descriptions (J2) (Continued)

I/O Card Pin	Signal Name	Description
75	EMIF_A16	PB2.1 header
76	EMIF_A17	PB2.0 header
77	EMIF_A18	PB1.15 header
78	EMIF_A19	PB1.14 header
79	EMIF_A20	PB1.13 header
80	EMIF_A21	PB1.12 header
81	EMIF_A22	
82	EMIF_A23	
83	HVGPIO7	
84	HVGPIO6	
85	HVGPIO5	PB4.5 header
86	HVGPIO4	PB4.4 header/Piezo Buzzer
87	HVGPIO3	PB4.3 header/Bright white D1 LED
88	HVGPIO2	PB4.2 header/Blue DS5 LED
89	HVGPIO1	PB4.1 header/Green DS5 LED
90	HVGPIO0	PB4.0 header/Red DS5 LED
91	EPCA_CH5_MOTOR	PB4.5 header
92	EPCA_CH4_MOTOR	PB4.4 header
93	EPCA_CH3_MOTOR	PB4.3 header
94	EPCA_CH2_MOTOR	PB4.2 header
95	EPCA_CH1_MOTOR	PB4.1 header
96	EPCA_CH0_MOTOR	PB4.0 header
97	EPCA_ECI_MOTOR	
98	UDPBUS_SCL_A	UDP motherboard I2C A clock
99	UDPBUS_SDA_A	UDP motherboard I2C A data
100	GND	

Table 7. UPIO-M3U1xx Card H3 Pin Descriptions (J3)

I/O Card Pin	Signal Name	Description
1	H3_100	
2	H3_99	
3	H3_98	
4	H3_97	
5	H3_96	
6	H3_95	
7	H3_94	
8	H3_93	
9	H3_92	
10	H3_91	
11	H3_90	
12	H3_89	
13	H3_88	
14	H3_87	
15	H3_86	
16	H3_85	
17	H3_84	
18	H3_83	
19	H3_82	
20	H3_81	
21	H3_80	
22	H3_79	
23	H3_78	
24	H3_77	
25	H3_76	
26	H3_75	
27	H3_74	
28	H3_73	
29	H3_72	
30	H3_71	
31	H3_70	
32	H3_69	
33	H3_68	
34	H3_67	
35	H3_66	
36	H3_65	

Table 7. UPIO-M3U1xx Card H3 Pin Descriptions (J3) (Continued)

I/O Card Pin	Signal Name	Description
37	H3_64	
38	H3_63	
39	H3_62	
40	H3_61	
41	H3_60	
42	H3_59	
43	H3_58	
44	H3_57	
45	H3_56	
46	H3_55	
47	UART_SYS_EN	
48	VCP_EN	
49	JTAG_TDI_A	PB1.4/TDI header
50	JTAG_TDO_A	PB1.3/TDO header
51	GND	
52	nc	
53	C2_DAT_E	
54	C2_CLK_E	
55	C2_DAT_D	
56	C2_CLK_D	
57	C2_DAT_C	
58	C2_CLK_C	
59	C2_DAT_B	
60	C2_CLK_B	
61	C2_DAT_A	
62	C2_CLK_A	
63	EBID_NSS	
64	EBID_MISO	
65	EBID_MOSI	
66	EBID_SCK	
67	GND	
68	PWR_SYS_BULK	3.3 V power supply for EBID devices
69	PWR_SYS_BULK	
70	VCC_3.3V	
71	VCC_3.3V	
72	VCC_3.3V	
73	VCC_3.3V	

Table 7. UPIO-M3U1xx Card H3 Pin Descriptions (J3) (Continued)

I/O Card Pin	Signal Name	Description
74	PWR_5.0_BULK	5.0 V power from the UDP motherboard
75	PWR_5.0_BULK	
76	PWR_5.0_BULK	
77	PWR_5.0_BULK	
78	PWR_VPP_BULK	
79	PWR_VPP_BULK	
80	PWR_HV2_BUS	High Drive I/O power 2
81	PWR_HV2_BUS	
82	PWR_HV1_BUS	High Drive I/O power 1
83	PWR_HV1_BUS	
84	PWR_AUX_BUS	
85	PWR_AUX_BUS	
86	PWR_IO_BUS	Connects power from the MCU card to the radio and I/O cards
87	PWR_IO_BUS	
88	PWR_IO_OUT	
89	PWR_IO_OUT	
90	PWR_IO_IN	
91	PWR_IO_IN	
92	PWR_RADIO_OUT	
93	PWR_RADIO_OUT	
94	PWR_RADIO_IN	
95	PWR_RADIO_IN	
96	PWR_VDD_OUT	
97	PWR_VDD_OUT	
98	PWR_VDD_IN	
99	PWR_VDD_IN	
100	GND	

Table 8. UPIO-M3U1xx Card H4 Pin Descriptions (J4)

I/O Card Pin	Signal Name	Description
1	GND	
2	H4_99	
3	H4_98	
4	H4_97	
5	ITM_CLK	
6	ITM_DAT3	
7	ITM_DAT2	
8	ITM_DAT1	
9	ITM_DAT0	
10	H4_91	
11	EZR_GPIO4	
12	EZR_GPIO3	
13	EZR_GPIO2	
14	EZR_GPIO1	
15	EZR_GPIO0	
16	EZR_VDI	
17	EZR_ARSSI	
18	EZR_RESET	
19	EZR_SI100X_RX	
20	EZR_FFIT	
21	EZR_DTO	
22	EZR_SI100X_TX	
23	EZR_NFFS	PB2.3 header
24	EZRP_NIRQ	
25	EZRP_SDN	PB2.2 header
26	GND	
27	EZRP_RX_DATA_OUT	PB2.1 header
28	EZRO_RX_CLK_OUT	PB2.0 header
29	EZRP_TX_DATA_IN	PB1.15 header
30	GND	
31	EZRP_CLK_IN	PB1.14 header
32	GND	
33	EXTREG_BD_A	PB3.11 header/External Voltage Regulator base drive output
34	EXTREG_OUT_A	PB3.10 header/External Voltage Regulator OUT output
35	EXTREG_SN_A	PB3.9 header/External Voltage Regulator SN input

Table 8. UPIO-M3U1xx Card H4 Pin Descriptions (J4) (Continued)

I/O Card Pin	Signal Name	Description
36	EXTREG_SP_A	PB3.8 header/External Voltage Regulator SP input
37	I2V_INN_A	PB0.8 header
38	I2V_INP_A	PB0.7 header
39	GND	
40	HVDA_INN_B	
41	HVDA_INP_B	
42	HVDA_INN_A	
43	HVDA_INP_A	
44	GND	
45	CP_NEG_B	PB3.5 header/Switch SW3
46	CP_POS_B	PB3.4 header/Switch SW2
47	CP_NEG_A	PB2.14 header
48	CP_POS_A	PB2.13 header
49	CP_OUTA_A	PB1.0H header
50	CP_OUT_A	PB0.15H header
51	IDAC_B	PB0.13 header
52	IDAC_A	PB0.14 header
53	GND	
54	DAC_OUT3	
55	DAC_OUT2	
56	DAC_OUT1	
57	DAC_OUT0	
58	DAC_VREFGND	
59	DAC_VREF	
60	GND	
61	ADC_IN3	PB1.11 header
62	ADC_IN2	PB1.10 header
63	ADC_IN1	PB1.6H header
64	ADC_IN0	PB1.5H header
65	ADC_VREFGND	PB0.11 header
66	ADC_VREF	PB1.12 header
67	GND	
68	C2D_RX15_A	
69	C2D_RX14_A	
70	C2D_RX13_A	
71	C2D_RX12_A	
72	C2D_RX11_A	

Table 8. UPIO-M3U1xx Card H4 Pin Descriptions (J4) (Continued)

I/O Card Pin	Signal Name	Description
73	C2D_RX10_A	
74	C2D_RX09_A	
75	C2D_RX08_A	
76	C2D_RX07_A	
77	C2D_RX06_A	
78	C2D_RX05_A	
79	C2D_RX04_A	
80	C2D_RX03_A	
81	C2D_RX02_A	
82	C2D_RX01_A	
83	C2D_RX00_A	
84	C2D_TX15_A	
85	C2D_TX14_A	
86	C2D_TX13_A	
87	C2D_TX12_A	
88	C2D_TX11_A	
89	C2D_TX10_A	
90	C2D_TX09_A	
91	C2D_TX08_A	
92	C2D_TX07_A	
93	C2D_TX06_A	PB0.8 header
94	C2D_TX05_A	PB0.7 header
95	C2D_TX04_A	PB0.6 header
96	C2D_TX03_A	PB0.5 header
97	C2D_TX02_A	PB0.4 header
98	C2D_TX01_A	PB0.3 header
99	C2D_TX00_A	PB0.2 header
100	GND	

NOTES:

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