

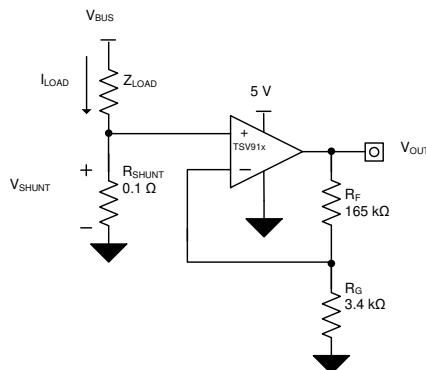
TSV91xA-Q1 Automotive Rail-to-Rail Input/Output, 8-MHz Operational Amplifiers

1 Features

- Rail-to-rail input and output
- Low noise: 18 nV/√Hz at 1 kHz
- Low power consumption: 550 μA (typical)
- High-gain bandwidth: 8 MHz
- Operating supply voltage from 2.5 V to 5.5 V
- Low input bias current: 1 pA (typical)
- Low input offset voltage: 1.5 mV (maximum)
- Low offset voltage drift: ±0.5 μV/°C (typical)
- ESD internal protection: ±4-kV human-body model (HBM)
- Extended temperature range: –40°C to 125°C

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- [Infotainment and cluster](#)
- [Passive safety](#)
- [Body electronics and lighting](#)
- [HEV/EV inverter and motor control](#)
- [On-board \(OBC\) and wireless charger](#)
- [Powertrain current sensor](#)
- [Advanced driver assistance systems \(ADAS\)](#)
- [Single-supply, low-side, unidirectional current-sensing circuit](#)



Low-Side Motor Control

3 Description

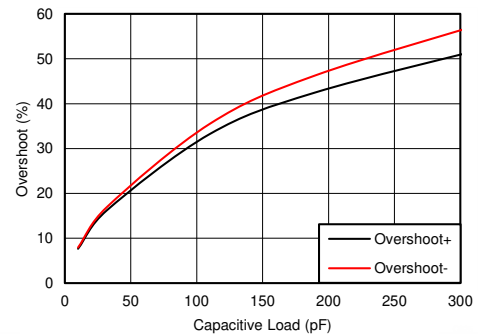
The TSV91xA-Q1 family, which includes single-, dual-, and quad-channel operational amplifiers (op amps), is specifically designed for general-purpose automotive applications. Featuring rail-to-rail input and output (RRIO) swings, wide bandwidth (8 MHz), and low offset voltage (0.3 mV, typical), this family is designed for a variety of applications that require a good balance between speed and power consumption. The op amps are unity-gain stable and feature an ultra-low input bias current, which enables the family to be used in applications with high-source impedances. The low input bias current allows the devices to be used for sensor interfaces, and active filtering.

The robust design of the TSV91xA-Q1 provides ease-of-use to the circuit designer. Features include a unity-gain stable, integrated RFI-EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
TSV911A-Q1	SOT-23 (5) ⁽²⁾	1.60 mm × 2.90 mm
TSV912A-Q1	SOIC (8)	3.91 mm × 4.90 mm
	VSSOP (8) ⁽²⁾	3.00 mm × 3.00 mm
TSV914A-Q1	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	4.40 mm × 5.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) Package is preview only for TSV91xA-Q1.



Small-Signal Overshoot vs Load Capacitance



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4 Revision History

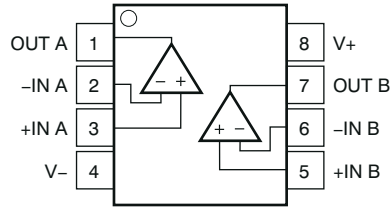
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Deleted preview tag from TSSOP package in <i>Device Information</i> table.....	1
• Deleted package preview note from TSV914-Q1 pinout drawing and <i>Pin Functions</i> table	4
• Added note 4 to differential input voltage in <i>Absolute Maximum Ratings</i> table.....	6
• Added thermal information for TSSOP (14) to <i>Thermal Information: TSV914A-Q1</i> table.....	7

Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS			
		DBV	D	DGK	PW
TSV911A-Q1	1	5	—	—	—
TSV912A-Q1	2	—	8	8	—
TSV914A-Q1	4	—	14	—	14

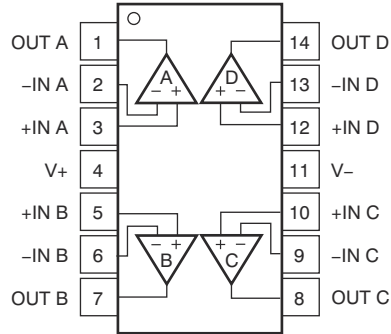
5 Pin Configuration and Functions



**Figure 5-1. TSV912A-Q1 D and DGK Package
8-Pin SOIC and VSSOP
Top View**

Table 5-1. Pin Functions: TSV912A-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply



**Figure 5-2. TSV914A-Q1 D and PW Package
14-Pin SOIC and TSSOP
Top View**

Table 5-2. Pin Functions: TSV914A-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
-IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
-IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V-	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage				6	V
Signal input pins	Voltage ⁽²⁾	Common-mode	(V-) – 0.5	(V+) + 0.5	V
		Differential ⁽⁴⁾	(V+) – (V-) + 0.2		
	Current ⁽²⁾		–10	10	mA
Output short-circuit ⁽³⁾			Continuous		mA
Specified, T _A			–40	125	°C
Junction, T _J				150	°C
Storage, T _{stg}			–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.
- (4) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

6.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _S	Supply voltage		2.5	5.5	V
	Specified temperature		–40	125	°C

6.4 Thermal Information: TSV912A-Q1

THERMAL METRIC ⁽¹⁾		TSV912A-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	157.6	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	104.6	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	99.7	TBD	°C/W
ψ _{JT}	Junction-to-top characterization parameter	55.6	TBD	°C/W
ψ _{JB}	Junction-to-board characterization parameter	99.2	TBD	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: TSV914A-Q1

THERMAL METRIC ⁽¹⁾		TSV914A-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	62.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67	76.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.4	13.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.6	76.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics: V_S (Total Supply Voltage) = $(V_+) - (V_-) = 2.5\text{ V to }5.5\text{ V}$

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$V_S = 5\text{ V}$		± 0.3	± 1.5	mV
		$V_S = 5\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$			± 3	
dV_{OS}/dT	Drift	$V_S = 5\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$		± 0.5		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 2.5\text{ V to }5.5\text{ V}$, $V_{CM} = (V_-)$		± 7		$\mu\text{V}/\text{V}$
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	$V_S = 2.5\text{ V to }5.5\text{ V}$	$(V_-) - 0.1$		$(V_+) + 0.1$	V
CMRR	Common-mode rejection ratio	$V_S = 5.5\text{ V}$ $(V_-) - 0.1\text{ V} < V_{CM} < (V_+) - 1.4\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$	80	103		dB
		$V_S = 5.5\text{ V}$, $V_{CM} = -0.1\text{ V to }5.6\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$	57	75		
		$V_S = 2.5\text{ V}$, $(V_-) - 0.1\text{ V} < V_{CM} < (V_+) - 1.4\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$		88		
		$V_S = 2.5\text{ V}$, $V_{CM} = -0.1\text{ V to }1.9\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$		70		
INPUT BIAS CURRENT						
I_B	Input bias current			± 5		pA
I_{OS}	Input offset current			± 5		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	$V_S = 5\text{ V}$, $f = 0.1\text{ Hz to }10\text{ Hz}$		4.77		μV_{PP}
e_n	Input voltage noise density	$V_S = 5\text{ V}$, $f = 10\text{ kHz}$		12		$\text{nV}/\sqrt{\text{Hz}}$
		$V_S = 5\text{ V}$, $f = 1\text{ kHz}$		18		
i_n	Input current noise density	$f = 1\text{ kHz}$		23		$\text{fA}/\sqrt{\text{Hz}}$
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_S = 2.5\text{ V}$, $(V_-) + 0.04\text{ V} < V_O < (V_+) - 0.04\text{ V}$ $R_L = 10\text{ k}\Omega$		100		dB
		$V_S = 5.5\text{ V}$, $(V_-) + 0.05\text{ V} < V_O < (V_+) - 0.05\text{ V}$ $R_L = 10\text{ k}\Omega$	104	130		
		$V_S = 2.5\text{ V}$, $(V_-) + 0.06\text{ V} < V_O < (V_+) - 0.06\text{ V}$ $R_L = 2\text{ k}\Omega$		100		
		$V_S = 5.5\text{ V}$, $(V_-) + 0.15\text{ V} < V_O < (V_+) - 0.15\text{ V}$ $R_L = 2\text{ k}\Omega$		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	$V_S = 5\text{ V}$, $G = 1$		8		MHz
ϕ_m	Phase margin	$V_S = 5\text{ V}$, $G = 1$		55		$^\circ$
SR	Slew rate	$V_S = 5\text{ V}$, $G = 1$ $R_L = 2\text{ k}\Omega$ $C_L = 100\text{ pF}$		4.5		$\text{V}/\mu\text{s}$
t_s	Settling time	To 0.1%, $V_S = 5\text{ V}$, 2-V step, $G = 1$ $C_L = 100\text{ pF}$		0.5		μs
		To 0.01%, $V_S = 5\text{ V}$, 2-V step, $G = 1$ $C_L = 100\text{ pF}$		1		
t_{OR}	Overload recovery time	$V_S = 5\text{ V}$, $V_{IN} \times \text{gain} > V_S$		0.2		μs
THD + N	Total harmonic distortion + noise ⁽¹⁾	$V_S = 5\text{ V}$, $V_O = 1\text{ V}_{RMS}$, $G = 1$, $f = 1\text{ kHz}$		0.0008%		

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from supply rails	$V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$			20	mV
		$V_S = 5.5\text{ V}$, $R_L = 2\text{ k}\Omega$			60	
I_{SC}	Short-circuit current	$V_S = 5\text{ V}$		± 50		mA
Z_O	Open-loop output impedance	$V_S = 5\text{ V}$, $f = 10\text{ MHz}$		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$V_S = 5.5\text{ V}$, $I_O = 0\text{ mA}$		550	750	μA
		$V_S = 5.5\text{ V}$, $I_O = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to 125°C			1100	

 (1) Third-order filter; bandwidth = 80 kHz at -3 dB .

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

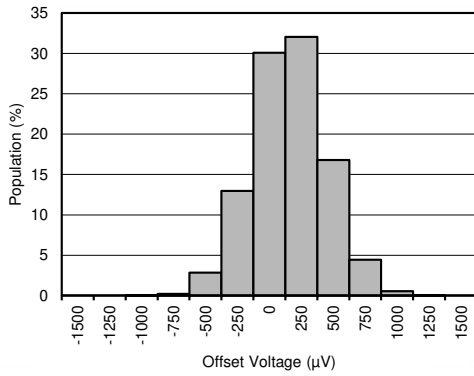
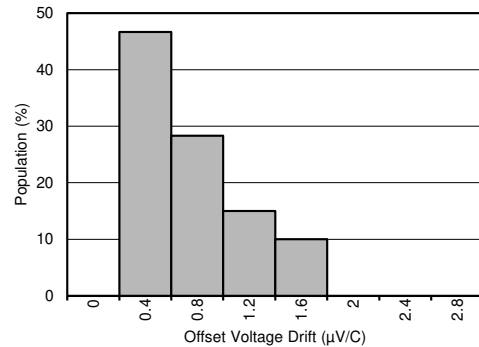


Figure 6-1. Offset Voltage Production Distribution



$T_A = -40^\circ\text{C}$ to 125°C

Figure 6-2. Offset Voltage Drift Distribution

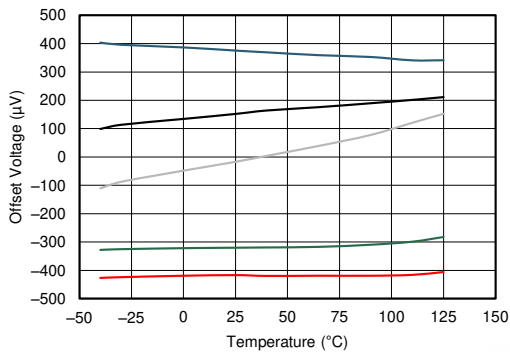
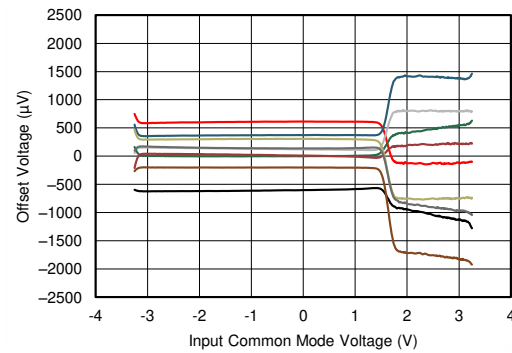
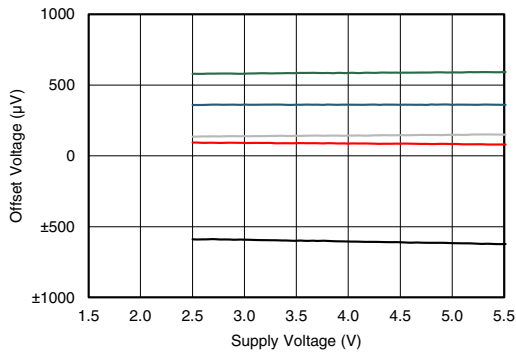


Figure 6-3. Offset Voltage vs Temperature



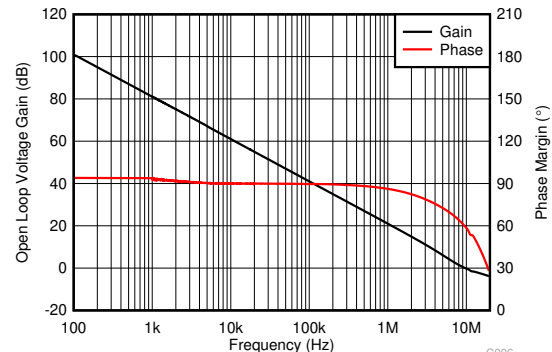
$V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$

Figure 6-4. Offset Voltage vs Common-Mode Voltage



$V_S = 2.5\text{ V}$ to 5.5 V

Figure 6-5. Offset Voltage vs Power Supply



$C_L = 10\text{ pF}$

Figure 6-6. Open-Loop Gain and Phase vs Frequency

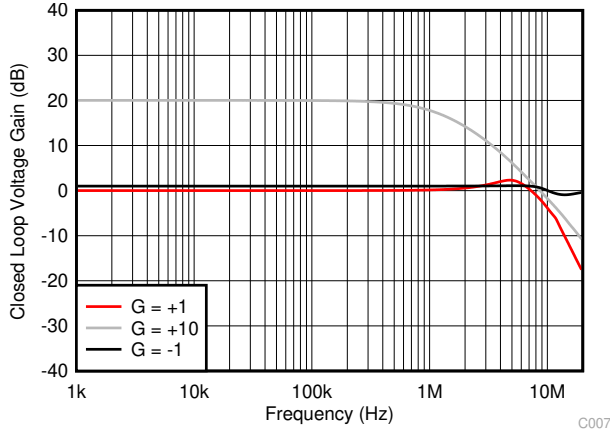


Figure 6-7. Closed-Loop Gain vs Frequency

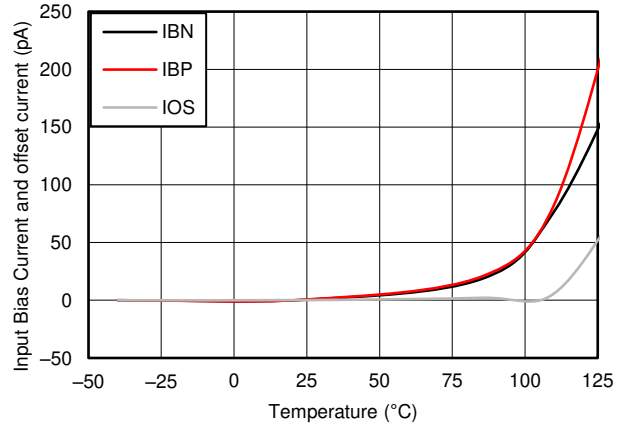


Figure 6-8. Input Bias Current vs Temperature

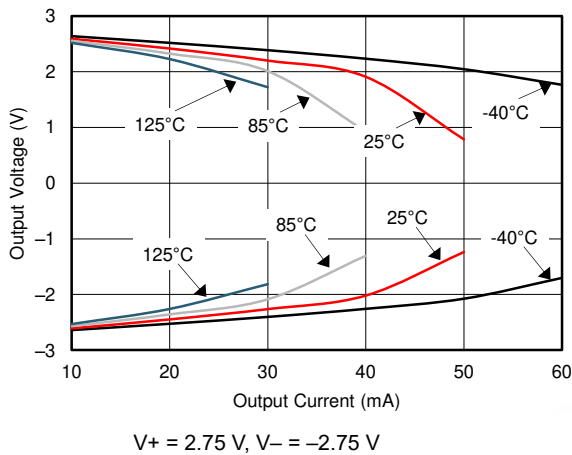


Figure 6-9. Output Voltage Swing vs Output Current

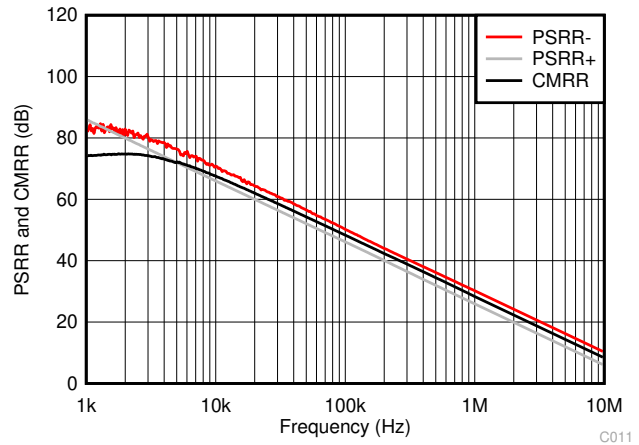


Figure 6-10. CMRR and PSRR vs Frequency (Referred to Input)

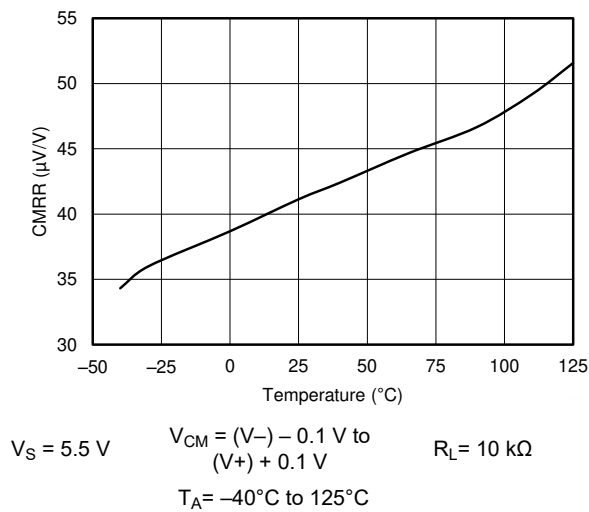


Figure 6-11. CMRR vs Temperature

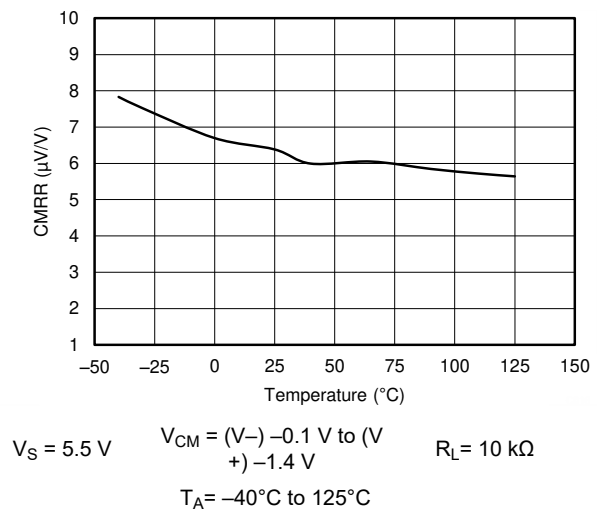
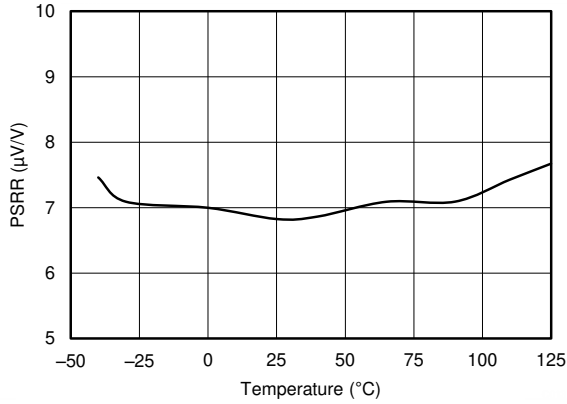
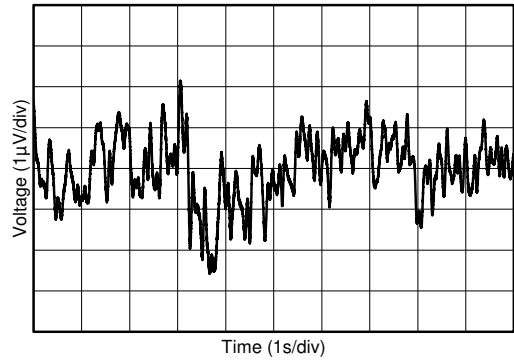


Figure 6-12. CMRR vs Temperature



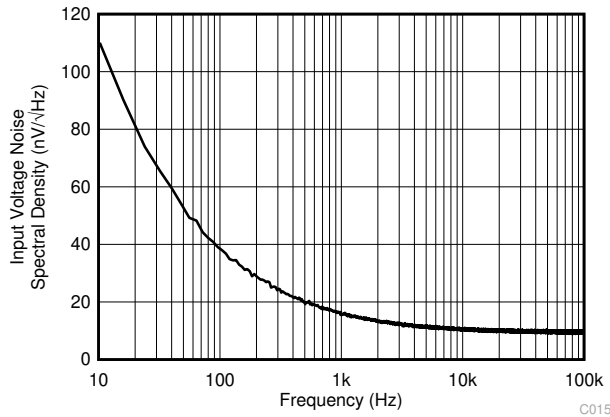
$V_S = 2.5\text{ V to }5.5\text{ V}$

Figure 6-13. PSRR vs Temperature



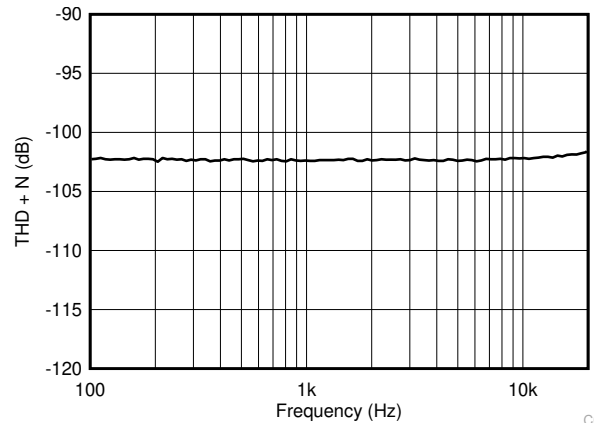
$V_S = 2.5\text{ V to }5.5\text{ V}$

Figure 6-14. 0.1-Hz to 10-Hz Input Voltage Noise



C015

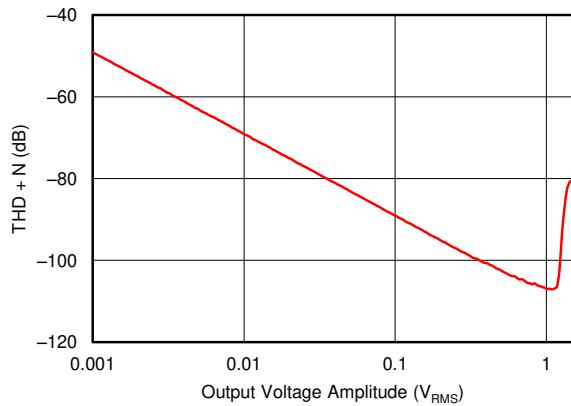
Figure 6-15. Input Voltage Noise Spectral Density vs Frequency



C017

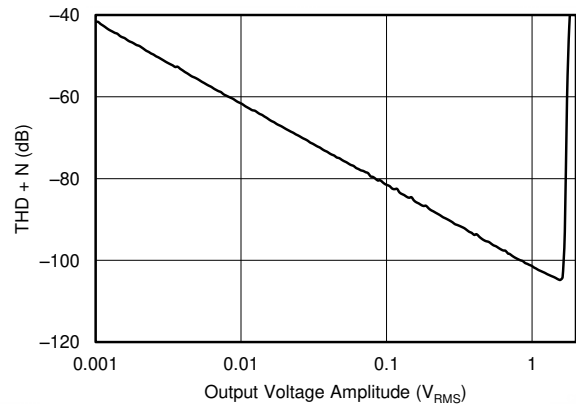
$V_S = 5.5\text{ V}$ $V_{CM} = 2.5\text{ V}$ $R_L = 2\text{ k}\Omega$
 $G = 1$ $V_{OUT} = 0.5 V_{RMS}$ $BW = 80\text{ kHz}$

Figure 6-16. THD + N vs Frequency



$V_S = 5.5\text{ V}$ $V_{CM} = 2.5\text{ V}$ $R_L = 2\text{ k}\Omega$
 $G = 1$ $BW = 80\text{ kHz}$ $f = 1\text{ kHz}$

Figure 6-17. THD + N vs Amplitude



$V_S = 5.5\text{ V}$ $V_{CM} = 2.5\text{ V}$ $R_L = 2\text{ k}\Omega$
 $G = -1$ $BW = 80\text{ kHz}$ $f = 1\text{ kHz}$

Figure 6-18. THD + N vs Amplitude

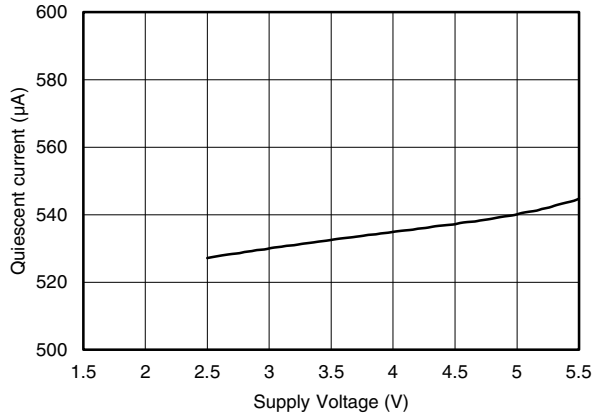


Figure 6-19. Quiescent Current vs Supply Voltage

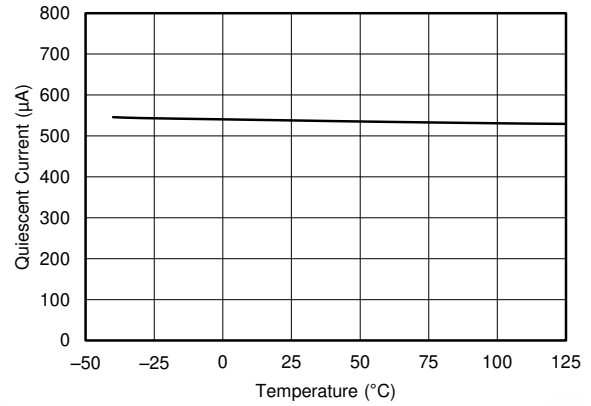


Figure 6-20. Quiescent Current vs Temperature

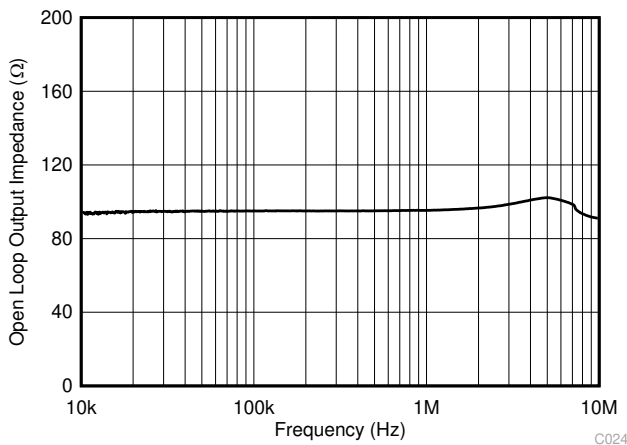
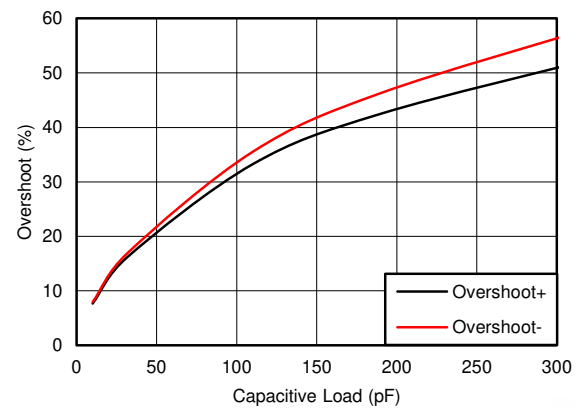
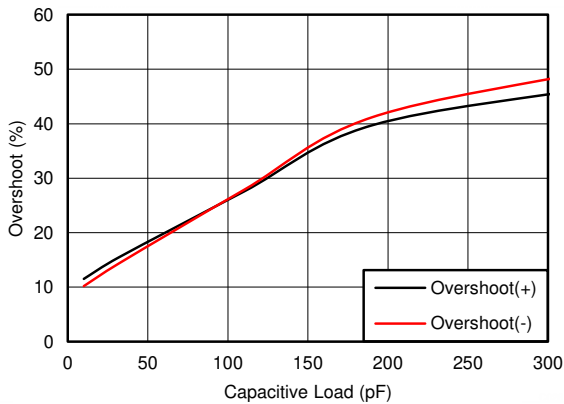


Figure 6-21. Open-Loop Output Impedance vs Frequency



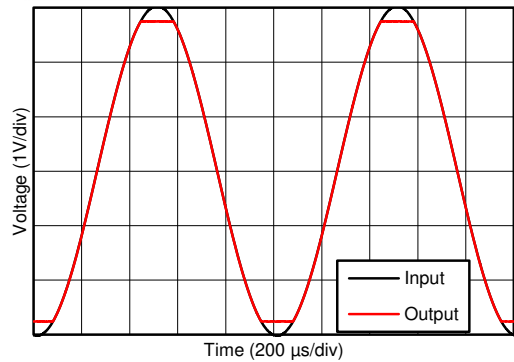
$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $G = 1\text{ V/V}$
 $R_L = 10\text{ k}\Omega$ $V_{OUT\text{ step}} = 100\text{ mV}_{p-p}$

Figure 6-22. Small-Signal Overshoot vs Load Capacitance



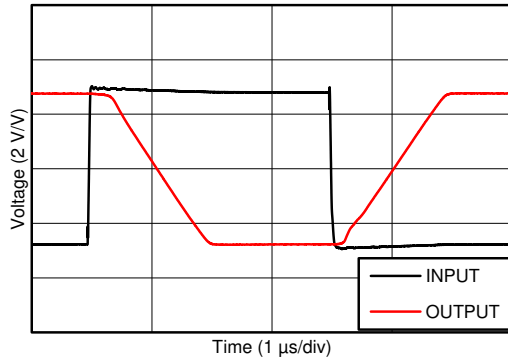
$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $R_L = 10\text{ k}\Omega$
 $G = -1\text{ V/V}$ $V_{OUT\text{ step}} = 100\text{ mV}_{p-p}$

Figure 6-23. Small-Signal Overshoot vs Load Capacitance



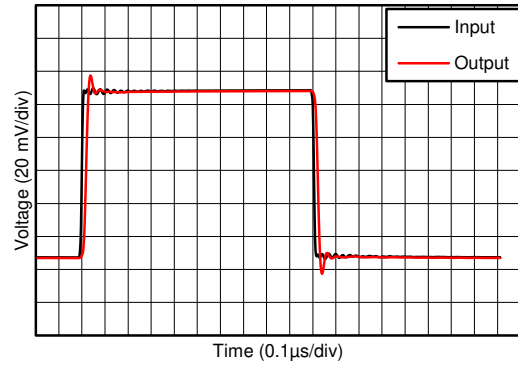
$V_+ = 2.75\text{ V}, V_- = -2.75\text{ V}$

Figure 6-24. No Phase Reversal



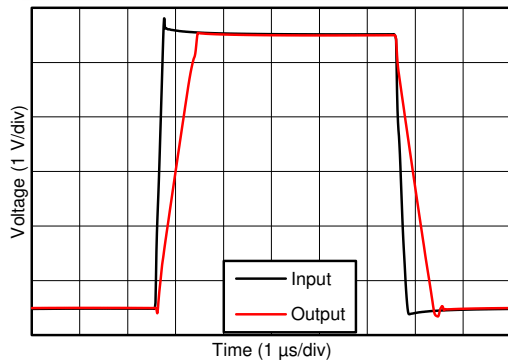
$V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $G = -10\text{ V/V}$

Figure 6-25. Overload Recovery



$V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $G = 1\text{ V/V}$

Figure 6-26. Small-Signal Step Response



$V_+ = 2.75\text{ V}$ $V_- = -2.75\text{ V}$ $C_L = 100\text{ pF}$
 $G = 1\text{ V/V}$

Figure 6-27. Large-Signal Step Response

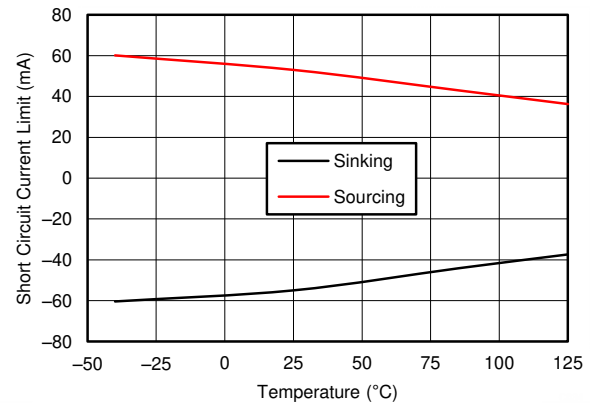


Figure 6-28. Short-Circuit Current vs Temperature

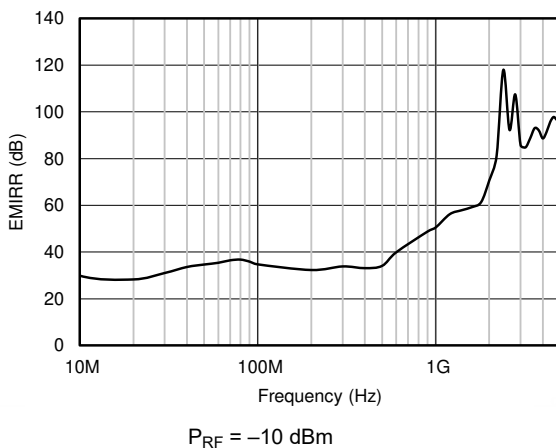


Figure 6-29. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

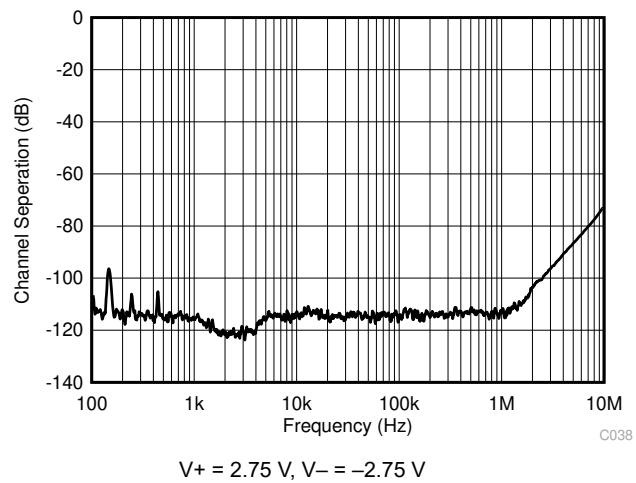
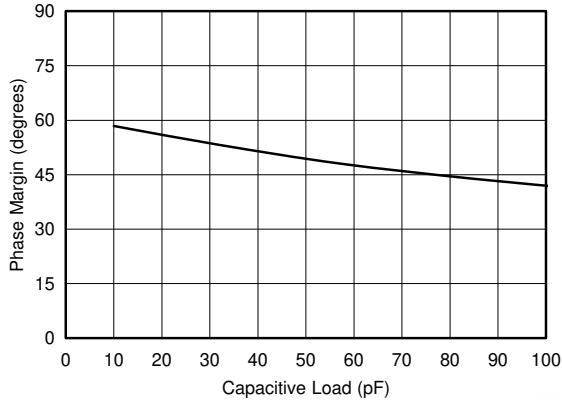
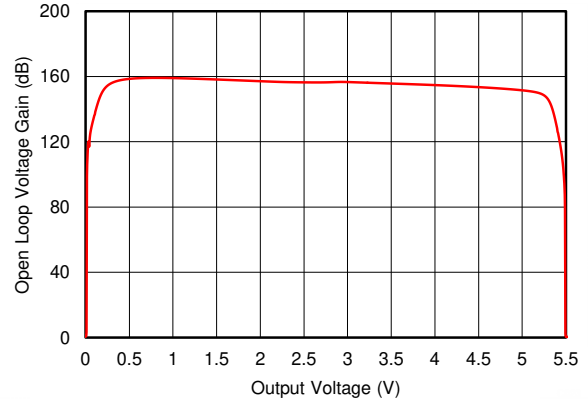


Figure 6-30. Channel Separation vs Frequency



$V_S = 5.5 \text{ V}$

Figure 6-31. Phase Margin vs Capacitive Load



A.

$V_S = 5.5 \text{ V}$

Figure 6-32. Open Loop Voltage Gain vs Output Voltage

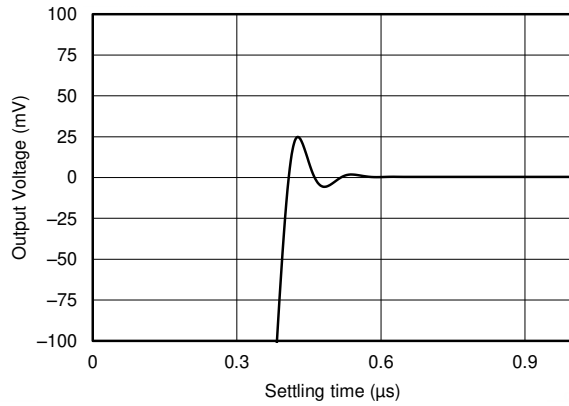


Figure 6-33. Large Signal Settling Time (Positive)

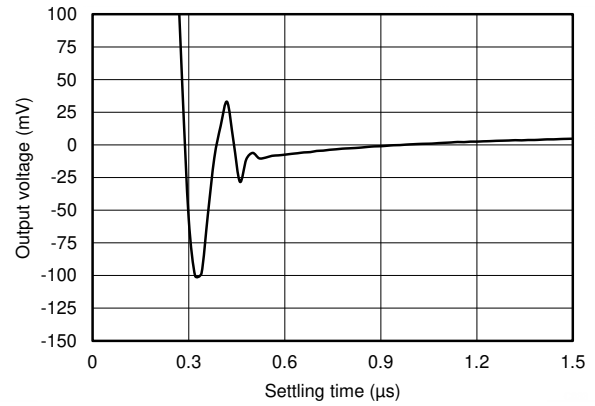


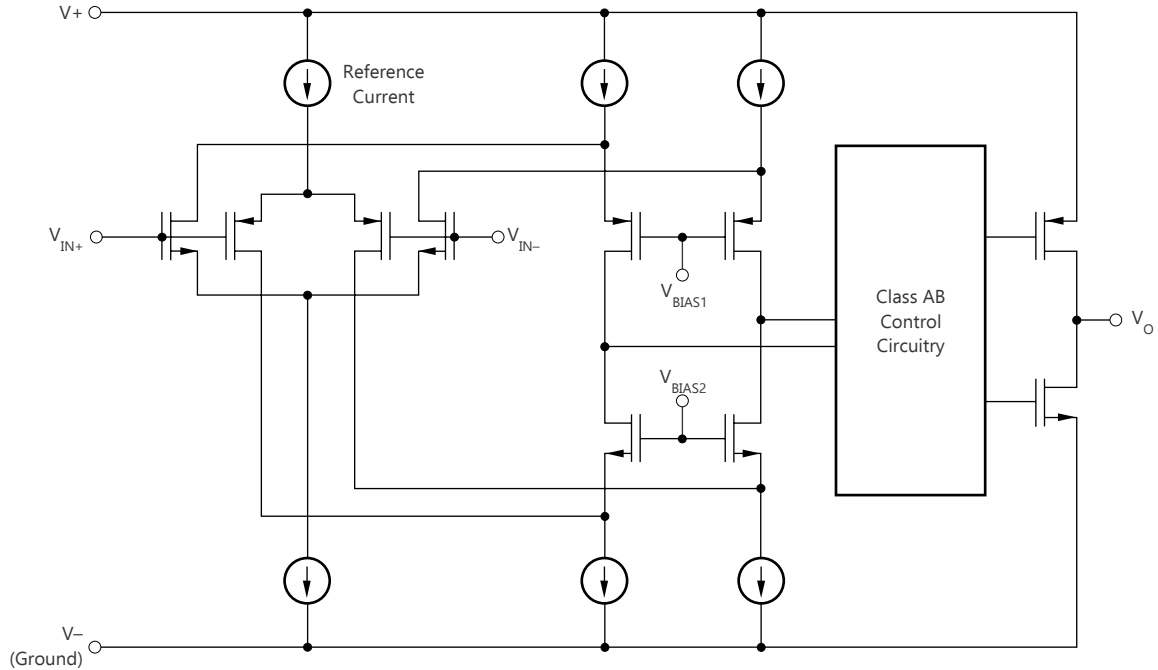
Figure 6-34. Large Signal Settling Time (Negative)

7 Detailed Description

7.1 Overview

The TSV91xA-Q1 series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose automotive applications. The input common-mode voltage range includes both rails and allows the TSV91xA-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications and are designed for driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TSV91xA-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 2.5 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Section 7.2](#). The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.4$ V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately $(V+) - 1.4$ V. There is a small transition region, typically $(V+) - 1.2$ V to $(V+) - 1$ V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from $(V+) - 1.4$ V to $(V+) - 1.2$ V on the low end, and up to $(V+) - 1$ V to $(V+) - 0.8$ V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

7.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TSV91xA-Q1 series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 k Ω , the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

7.3.3 Packages With an Exposed Thermal Pad

The TSV91xA-Q1 family is available in packages such as the WSON-8 (DSG) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V $-$ or left floating. Attaching the thermal pad to a potential other than V $-$ is not allowed, and the performance of the device is not assured when doing so.

7.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TSV91xA-Q1 series is approximately 200 ns.

7.4 Device Functional Modes

The TSV91xA-Q1 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.5 V (± 1.25 V) and 5.5 V (± 2.75 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TSV91xA-Q1 series features 8-MHz bandwidth and 4.5-V/ μ s slew rate with only 550 μ A of supply current per channel, providing good AC performance at low power consumption. DC applications are well served with a low input noise voltage of 18 nV / $\sqrt{\text{Hz}}$ at 1 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

8.2 Typical Application

Figure 8-1 shows the TSV91xA-Q1 configured in a low-side, motor-control application.

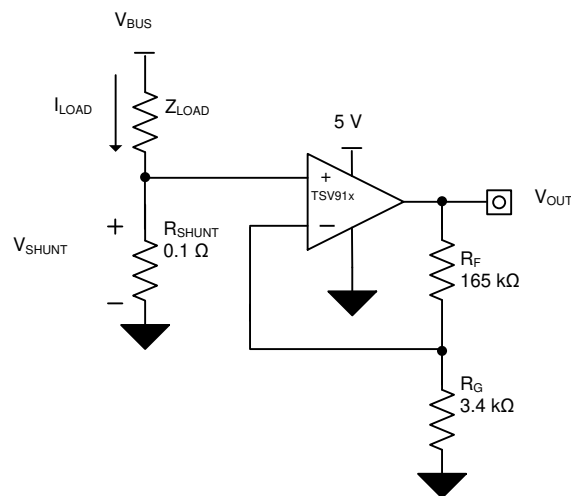


Figure 8-1. TSV91xA-Q1 in a Low-Side, Motor-Control Application

8.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

8.2.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 8-1](#) is shown in [Equation 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [Equation 2](#), R_{SHUNT} is 100 m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TSV91xA-Q1 to produce an output voltage of approximately 0 V to 4.95 V. The gain required by the TSV91xA-Q1 to produce the necessary output voltage is calculated using [Equation 3](#):

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using [Equation 3](#), the required gain is calculated to be 49.5 V/V, which is set with resistors R_F and R_G . [Equation 4](#) is used to size the resistors, R_F and R_G , to set the gain of the TSV91xA-Q1 to 49.5 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F as 165 k Ω and R_G as 3.4 k Ω provides a combination that equals roughly 49.5 V/V. [Figure 8-2](#) shows the measured transfer function of the circuit shown in [Figure 8-1](#).

8.2.3 Application Curve

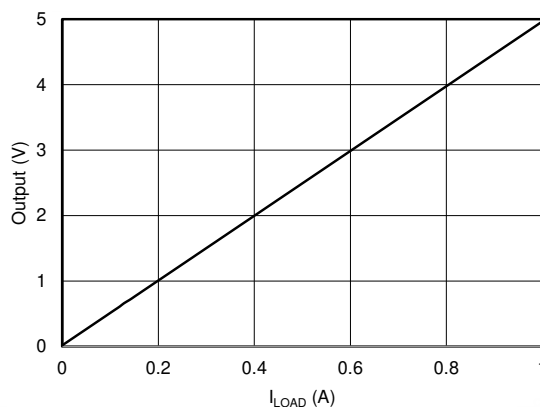


Figure 8-2. Low-Side, Current-Sense, Transfer Function

9 Power Supply Recommendations

The TSV91xA-Q1 series is specified for operation from 2.5 V to 5.5 V (± 1.25 V to ± 2.75 V); many specifications apply from -40°C to 125°C . [Section 6.7](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Section 10.2](#).

9.1 Input and ESD Protection

The TSV91xA-Q1 series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the [Absolute Maximum Ratings](#) table. [Figure 9-1](#) shows how a series input resistor is added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

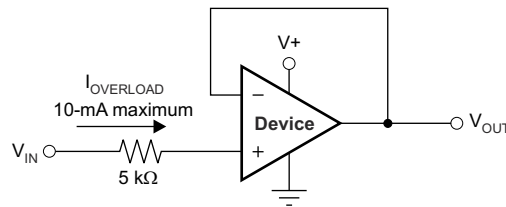


Figure 9-1. Input Current Protection

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 10-2](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

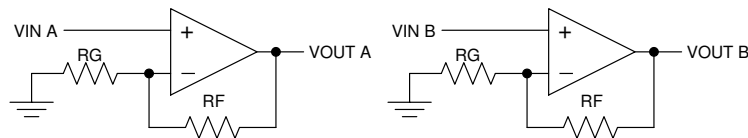


Figure 10-1. Schematic Representation of Layout Example

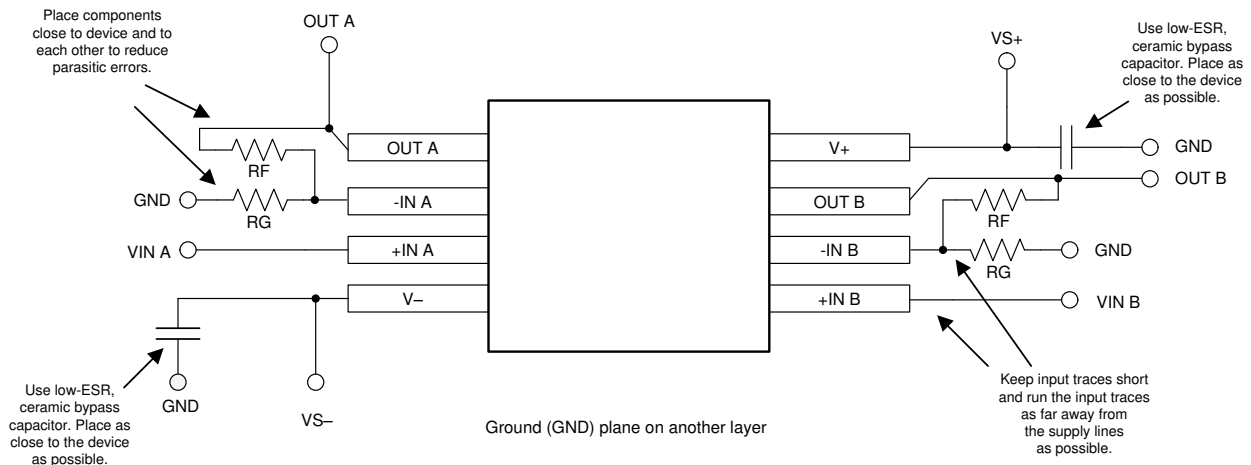


Figure 10-2. Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TSV912A-Q1	Click here	Click here	Click here	Click here	Click here
TSV914A-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSV912AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS912Q	Samples
TSV914AQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AQD	Samples
TSV914AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T914AQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSV912AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TSV914AQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TSV914AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSV912AQDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TSV914AQDRQ1	SOIC	D	14	2500	853.0	449.0	35.0
TSV914AQPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

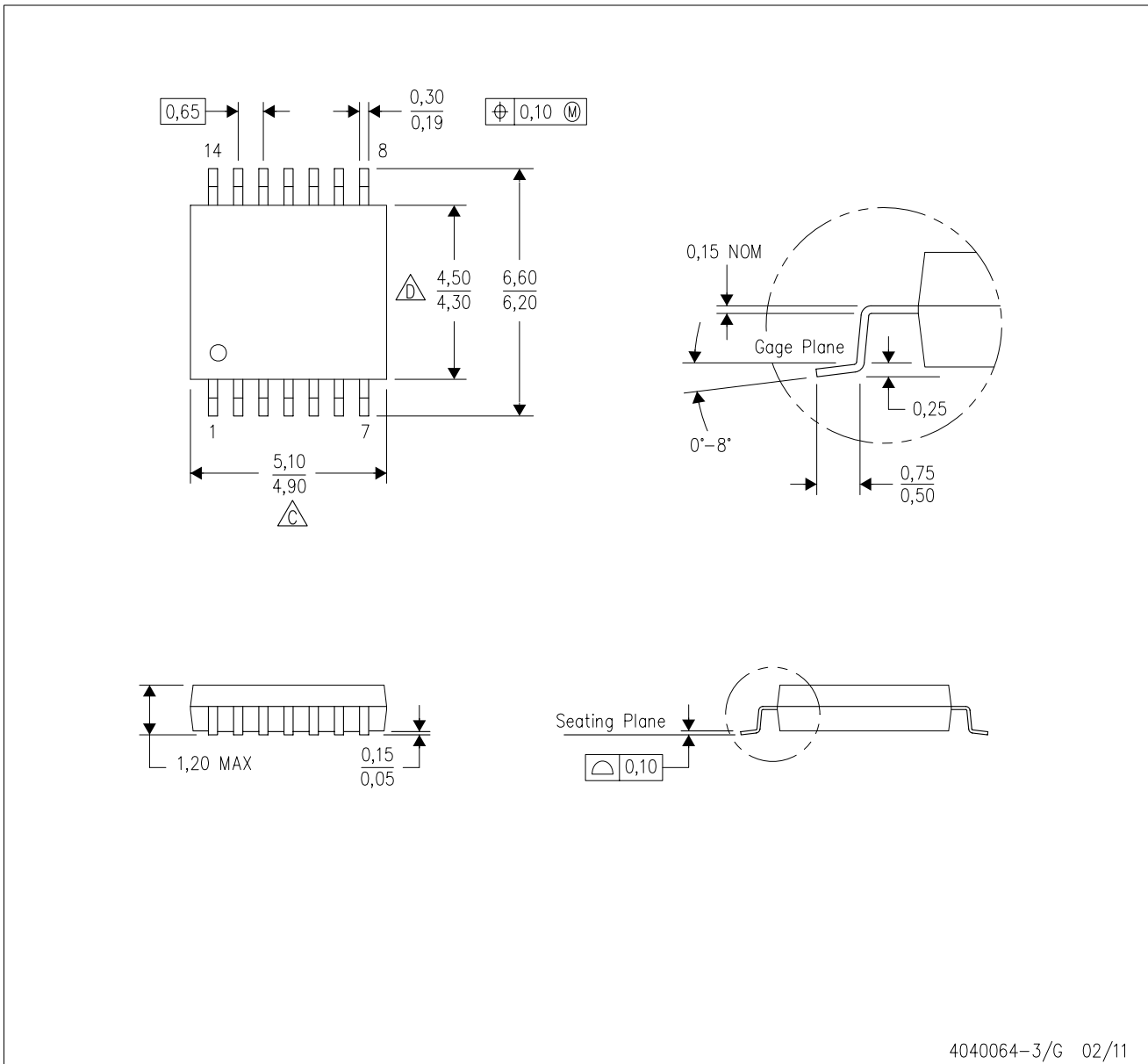


4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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