LM1815 Adaptive Variable Reluctance Sensor Amplifier

Check for Samples: LM1815

FEATURES

- **Adaptive Hysteresis**
- **Single Supply Operation**
- **Ground Referenced Input**
- **True Zero Crossing Timing Reference**
- **Operates from 2V to 12V Supply Voltage**
- **Handles Inputs from 100 mV_{P-P} to over 120V_{P-P} with External Resistor**
- **CMOS Compatible Logic**

APPLICATIONS

- **Position Sensing with Notched Wheels**
- **Zero Crossing Switch**
- **Motor Speed Control**
- **Tachometer**
- **Engine Testing**

DESCRIPTION

The LM1815 is an adaptive sense amplifier and default gating circuit for motor control applications. The sense amplifier provides a one-shot pulse output whose leading edge coincides with the negative-going zero crossing of a ground referenced input signal such as from a variable reluctance magnetic pick-up coil.

In normal operation, this timing reference signal is processed (delayed) externally and returned to the LM1815. A Logic input is then able to select either the timing reference or the processed signal for transmission to the output driver stage.

The adaptive sense amplifier operates with a positive-going threshold which is derived by peak detecting the incoming signal and dividing this down. Thus the input hysteresis varies with input signal amplitude. This enables the circuit to sense in situations where the high speed noise is greater than the low speed signal amplitude. Minimum input signal is 150mV_{P-P}.

Connection Diagram

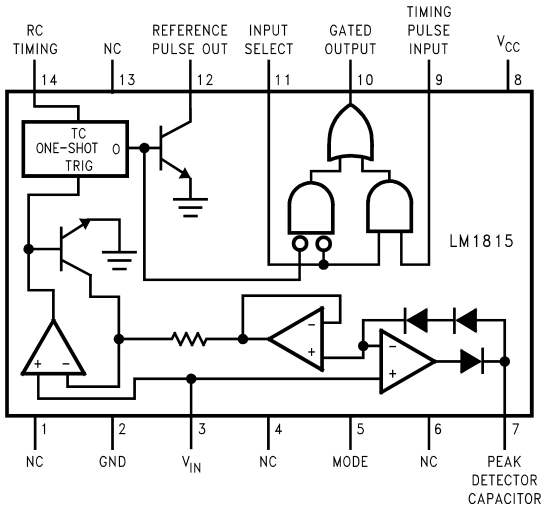

Figure 1. Top View
14-Lead SOIC or PDIP
See D or NFF0014A Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Absolute Maximum Ratings[1][2]

Supply Voltage	12V
Power Dissipation[3]	1250 mW
Operating Temperature Range	$-40°C \le T_A \le +125°C$
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Junction Temperature	+150°C
Input Current	±30 mA
Lead Temperature (Soldering, 10 sec.)	260°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For operation at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W (DIP), 120°C/W (SO-14) junction to ambient.

Electrical Characteristics

(T_A = 25°C, V_{CC} = 10V, unless otherwise specified, see Figure 17)

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage		2.5	10	12	V
Supply Current	Pin 3 = -0.1V, Pin 9 = 2V, Pin 11 = 0.8V		3.6	6	mA
Reference Pulse Width	f_{IN} = 1Hz to 2kHz, R = 150kΩ, C = 0.001µF	70	100	130	µs
Logic Input Bias Current	V_{IN} = 2V, (Pin 9 and Pin 11)			5	µA
Signal Input Bias Current	V_{IN} = 0V dc, (Pin 3)		-200		nA
Logic Threshold	(Pin 9 and Pin 11)	0.8	1.1	2.0	V
V_{OUT} High	R_L = 1kΩ, (Pin 10)	7.5	8.6		V
V_{OUT} Low	I_{SINK} = 0.1mA, (Pin 10)		0.3	0.4	V
Output Leakage Pin 12	V_{12} = 11V		0.01	10	µA
Saturation Voltage P12	I_{12} = 2mA		0.2	0.4	V
Input Zero Crossing Threshold	All Modes, V_{SIGNAL} = 1V pk-pk	-25	0	25	mV[1]
Minimum Input Arming Threshold	Mode 1, Pin 5 = Open	30	45	60	mV[1]
	Mode 2, Pin 5 = V_{CC}	200	300	450	mV[1]
	Mode 3, Pin 5 = Gnd	-25	0	25	mV[1]
Adaptive Input Arming Threshold	Mode 1, Pin 5 = Open V_{SIGNAL} ≥ 230mV pk-pk[2]	40	80	90	%[1]
	Mode 2, Pin 5 = V_{CC} V_{SIGNAL} ≥ 1.0V pk-pk[2]		80		%[1]
	Mode 3, Pin 5 = Gnd V_{SIGNAL} ≥ 150mV pk-pk[2]		80		%[1]

(1) The Min/Typ Max limits are relative to the positive voltage peak seen at V_{IN} Pin 3.
(2) Tested per Figure 17, V_{SIGNAL} is a Sine Wave; F_{SIGNAL} is 1000Hz.

Typical Performance Characteristics

Mode 1 Minimum Arming Threshold vs Temperature

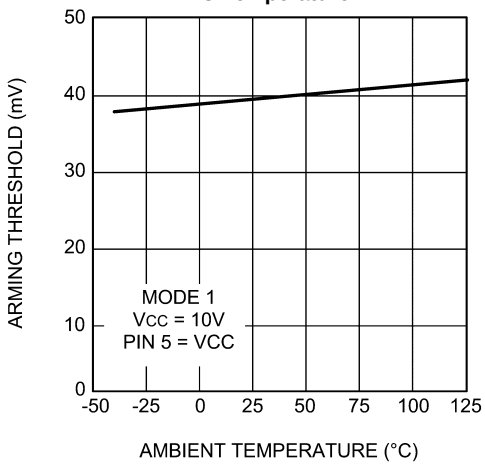


Figure 2.

Mode 2 Minimum Arming Threshold vs Temperature

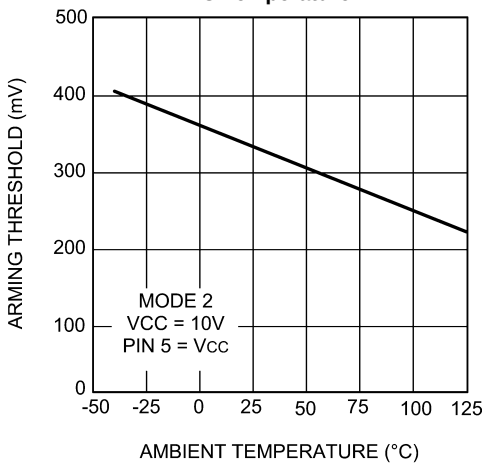


Figure 3.

Mode 3 Minimum Arming Threshold vs Temperature

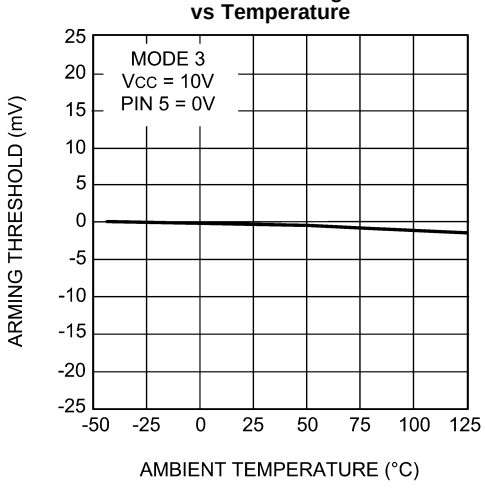


Figure 4.

Mode 1 Minimum Arming Threshold vs V_{CC}

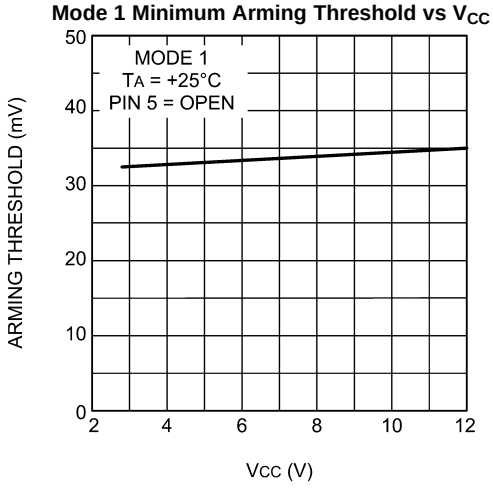


Figure 5.

Mode 2 Minimum Arming Threshold vs V_{CC}

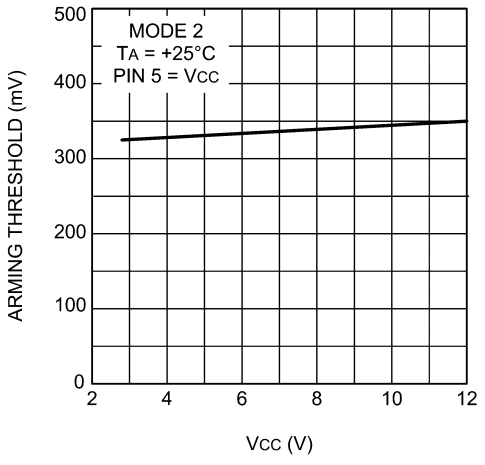


Figure 6.

Pin 3 V_{IN} vs V_{SIGNAL}

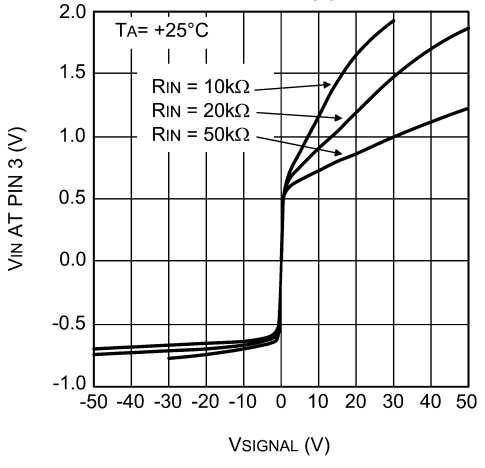


Figure 7.

Typical Performance Characteristics (continued)

Pin 3 V_{IN} vs V_{SIGNAL}, R_{IN} = 10kΩ

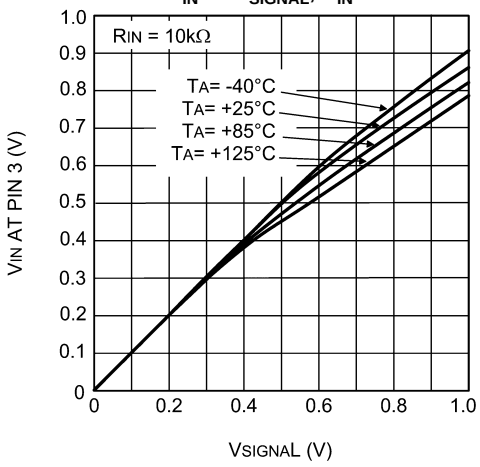


Figure 8.

Pin 3 V_{IN} vs V_{SIGNAL}, R_{IN} = 20kΩ

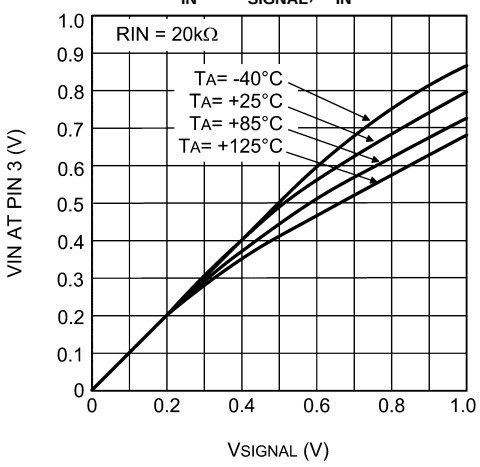


Figure 9.

Pin 3 V_{IN} vs V_{SIGNAL}, R_{IN} = 50kΩ

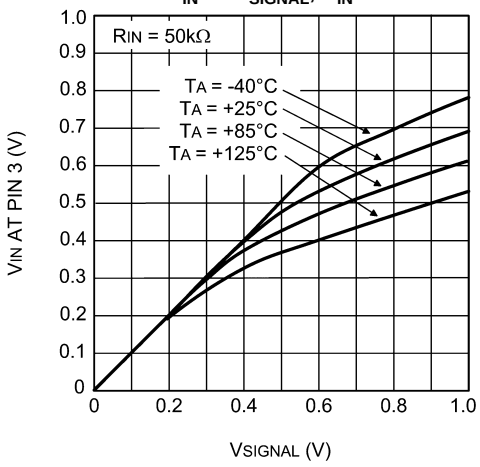


Figure 10.

Pin 3 Bias Current vs Temperature

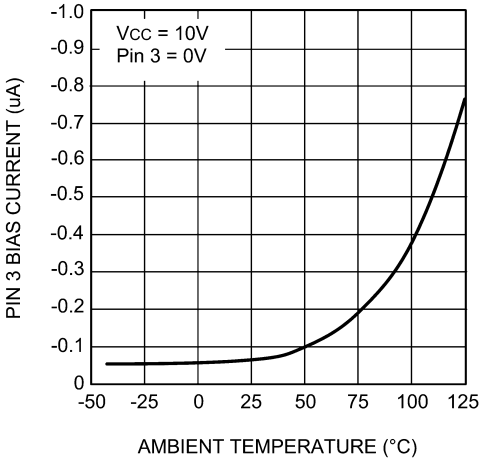


Figure 11.

Peak Detector Charge Current vs Temperature

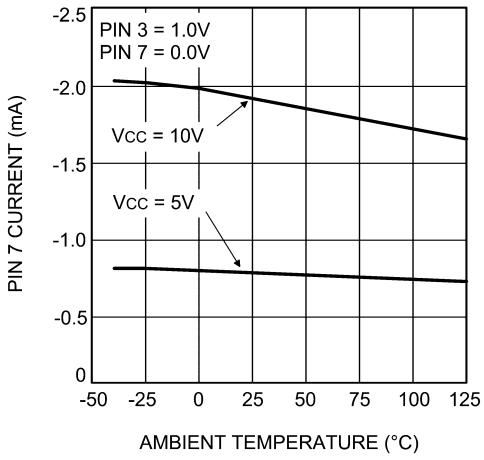


Figure 12.

Peak Detector Charge Current vs V_{CC}

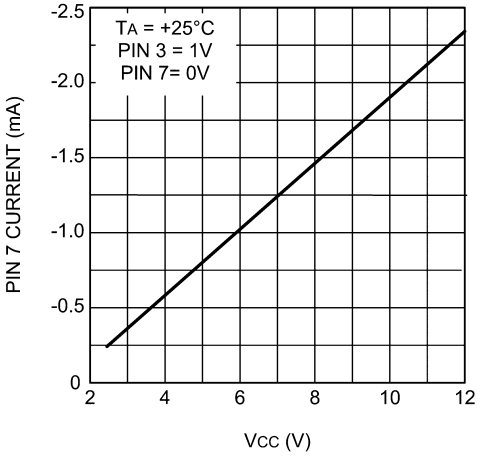


Figure 13.

Typical Performance Characteristics (continued)

Peak Detector Voltage vs Pin 3 V_{IN}, Mode 1

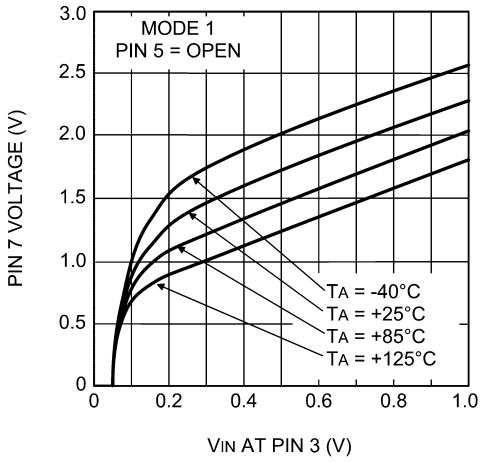


Figure 14.

Peak Detector Voltage vs Pin 3 V_{IN}, Mode 2

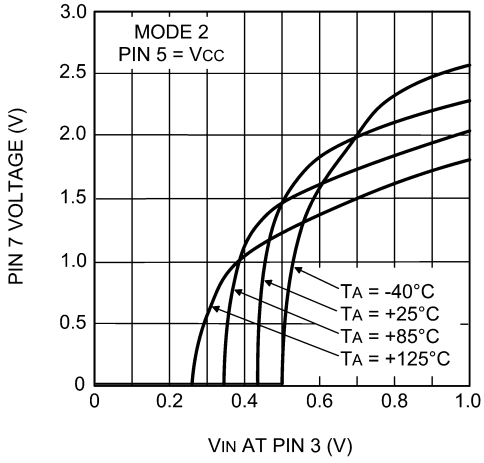


Figure 15.

Peak Detector Voltage vs Pin 3 V_{IN}, Mode 3

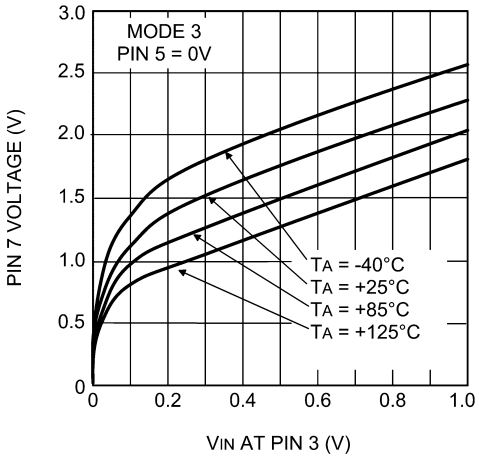


Figure 16.

TRUTH TABLE

Signal Input Pin 3	RC Timing Pin 14	Input Select Pin 11	Timing Input Pin 9	Gated Output Pin 10
± Pulses	RC	L	X	Pulses = RC
X	X	H	H	H
X	X	H	L	L
± Pulses	L	L	L	Zero Crossing

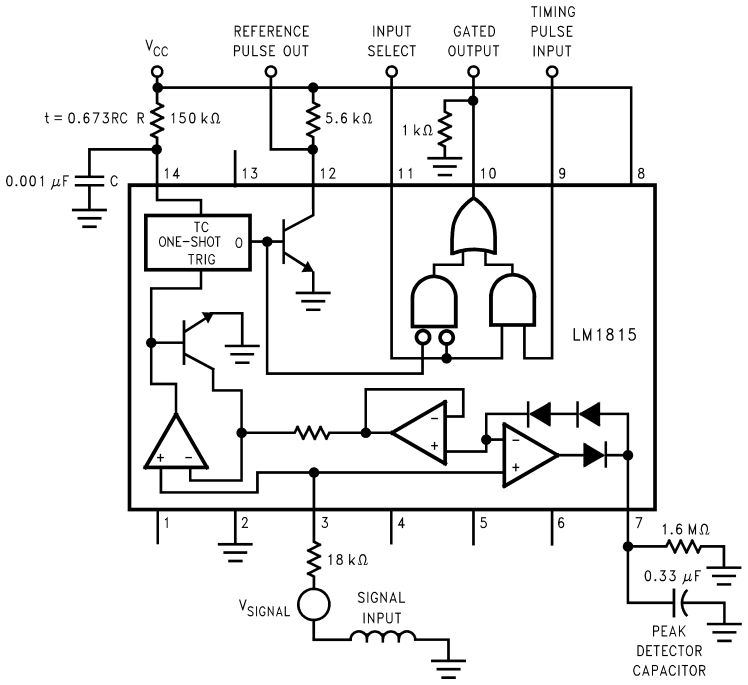
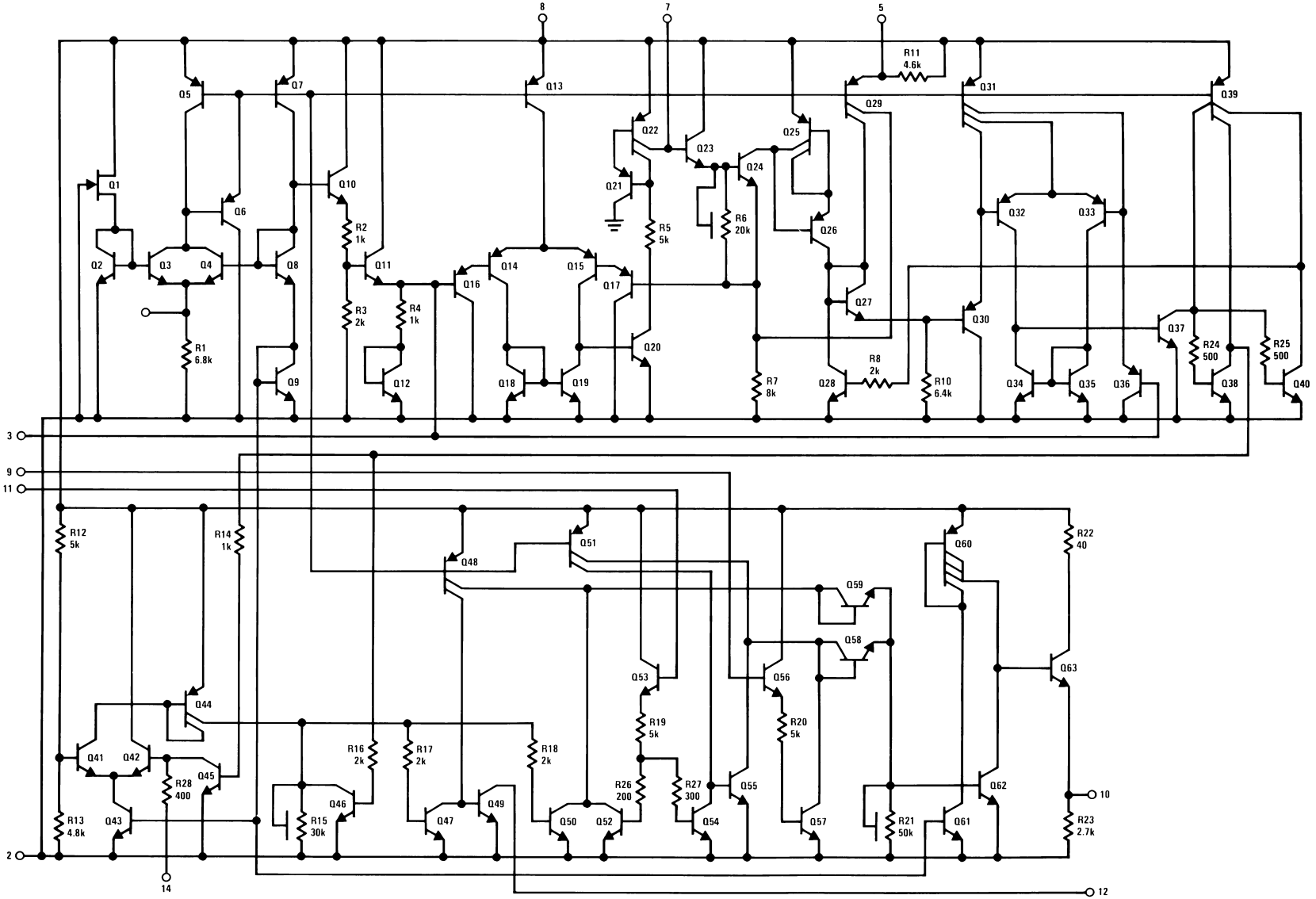


Figure 17. LM1815 Adaptive Sense Amplifier

Schematic Diagram



APPLICATION HINTS

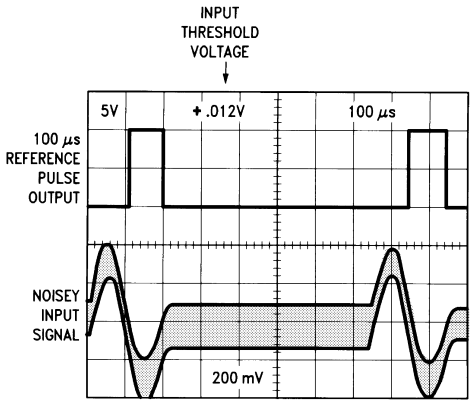


Figure 18. LM1815 Oscillograms

INPUT VOLTAGE CLAMP

The signal input voltage at pin 3 is internally clamped. Current limit for the Input pin is provided by an external resistor which should be selected to allow a peak current of ±3 mA in normal operation. Positive inputs are clamped by a 1kΩ resistor and series diode (see R4 and Q12 in the internal schematic diagram), while an active clamp limits pin 3 to typically 350mV below Ground for negative inputs (see R2, R3, Q10, and Q11 in the internal schematic diagram). Thus for input signal transitions that are more than 350mV below Ground, the input pin current (up to 3mA) will be pulled from the V+ supply. If the V+ pin is not adequately bypassed the resulting voltage ripple at the V+ pin will disrupt normal device operation. Likewise, for input signal transitions that are more than 500mV above Ground, the input pin current will be dumped to Ground through device pin 2. Slight shifts in the Ground potential at device pin 2, due to poor grounding techniques relative to the input signal ground, can cause unreliable operation. As always, adequate device grounding, and V+ bypassing, needs to be considered across the entire input voltage and frequency range for the intended application.

INPUT CURRENT LIMITING

As stated earlier, current limiting for the Input pin is provided by a user supplied external resistor. For purposes of selecting the appropriate resistor value the Input pin should be considered to be a zero ohm connection to ground. For applications where the input voltage signal is not symmetrical with relationship to Ground the worst case voltage peak should be used.

Minimum Rext = [(Vin peak)/3mA]

In the application example shown in Figure 17 (Rext = 18kΩ) the recommended maximum input signal voltage is ±54V (i.e. 108Vp-p).

OPERATION OF ZERO CROSSING DETECTOR

The LM1815 is designed to operate as a zero crossing detector, triggering an internal one shot on the negative-going edge of the input signal. Unlike other zero crossing detectors, the LM1815 cannot be triggered until the input signal has crossed an "arming" threshold on the positive-going portion of the waveform. The arming circuit is reset when the chip is triggered, and subsequent zero crossings are ignored until the arming threshold is exceeded again. This threshold varies depending on the connection at pin 5. Three different modes of operation are possible:

MODE 1, PIN 5 OPEN

The adaptive mode is selected by leaving device pin 5 open circuit. For input signals of less than ±135mV (i.e. 270 mVp-p) and greater than typically ±75mV (i.e. 150mVp-p), the input arming threshold is typically at 45mV. Under these conditions the input signal must first cross the 45mV threshold in the positive direction to arm the zero crossing detector, and then cross zero in the negative direction to trigger it.

If the signal is less than 30mV peak (minimum rating in Electrical Characteristics), the one shot is ensured to not trigger.

Input signals of greater than ±230mV (i.e. 460 mVp-p) will cause the arming threshold to track at 80% of the peak input voltage. A peak detector capacitor at device pin 7 stores a value relative to the positive input peaks to establish the arming threshold. Input signals must exceed this threshold in the positive direction to arm the zero crossing detector, which can then be triggered by a negative-going zero crossing.

The peak detector tracks rapidly as the input signal amplitude increases, and decays by virtue of the resistor connected externally at pin 7 track decreases in the input signal.

If the input signal amplitude falls faster than the voltage stored on the peak detector capacitor there may be a loss of output signal until the capacitor voltage has decayed to an appropriate level.

Note that since the input voltage is clamped, the waveform observed at pin 3 is not identical to the waveform observed at the variable reluctance sensor. Similarly, the voltage stored at pin 7 is not identical to the peak voltage appearing at pin 3.

MODE 2, PIN 5 CONNECTED TO V+

The input arming threshold is fixed at 200mV minimum when device pin 5 is connected to the positive supply. The chip has no output for signals of less than ±200 mV (i.e. 400mVp-p) and triggers on the next negative-going zero crossing when the arming threshold is has been exceeded.

MODE 3, PIN 5 GROUNDED

With pin 5 grounded, the input arming threshold is set to 0V, ±25mV maximum. Positive-going zero crossings arm the chip, and the next negative-going zero crossing triggers it. This is the very basic form of zero-crossing detection.

ONE SHOT TIMING

The one shot timing is set by a resistor and capacitor connected to pin 14. The recommended maximum resistor value is 150kohms. The capacitor value can be changed as needed, as long as the capacitor type does not present any signfigant leakage that would adversely affect the RC time constant.

The output pulse width is:

$$\text{pulse width} = 0.673 \times R \times C \quad (1)$$

For a given One Shot pulse width, the recommended maximum input signal frequency is:

$$F_{in(max)} = 1/(1.346 \times R \times C) \quad (2)$$

In the application example shown in Figure 17 (R=150kohms, C=0.001µF) the recommended maximum input frequency will typically be 5kHz. Operating with input frequencies above the recommended Fin (max) value may result in unreliable performance of the One Shot circuitry. For those applications where the One Shot circuit is not required, device pin 14 can be tied directly to Ground.

LOGIC INPUTS

In some systems it is necessary to externally generate pulses, such as during stall conditions when the variable reluctance sensor has no output. External pulse inputs at pin 9 are gated through to pin 10 when Input Select (pin 11) is pulled high. Pin 12 is a direct output for the one shot and is unaffected by the status of pin 11.

Input/output pins 9, 11, 10, and 12 are all CMOS logic compatible. In addition, pins 9, 11, and 12 are TTL compatible. Pin 10 is not ensured to drive a TTL load.

Pins 1, 4, 6 and 13 have no internal connections and can be grounded.

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1815MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM1815M	Samples
LM1815N/NOPB	OBSOLETE	PDIP	NFF	14		TBD	Call TI	Call TI		LM1815N	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

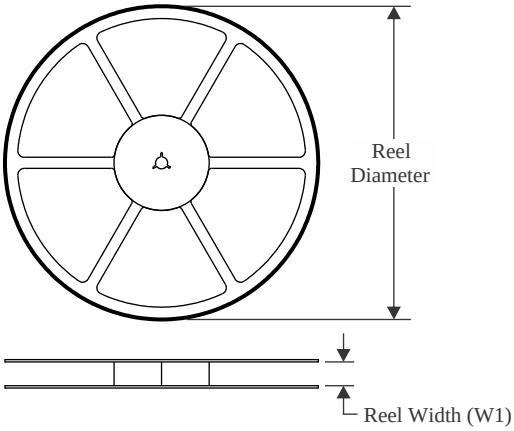
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

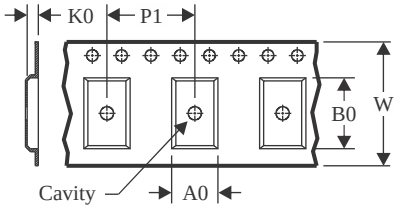
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

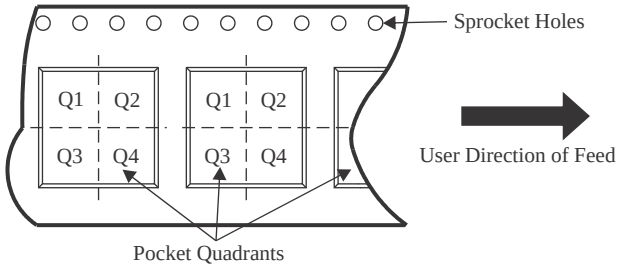


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

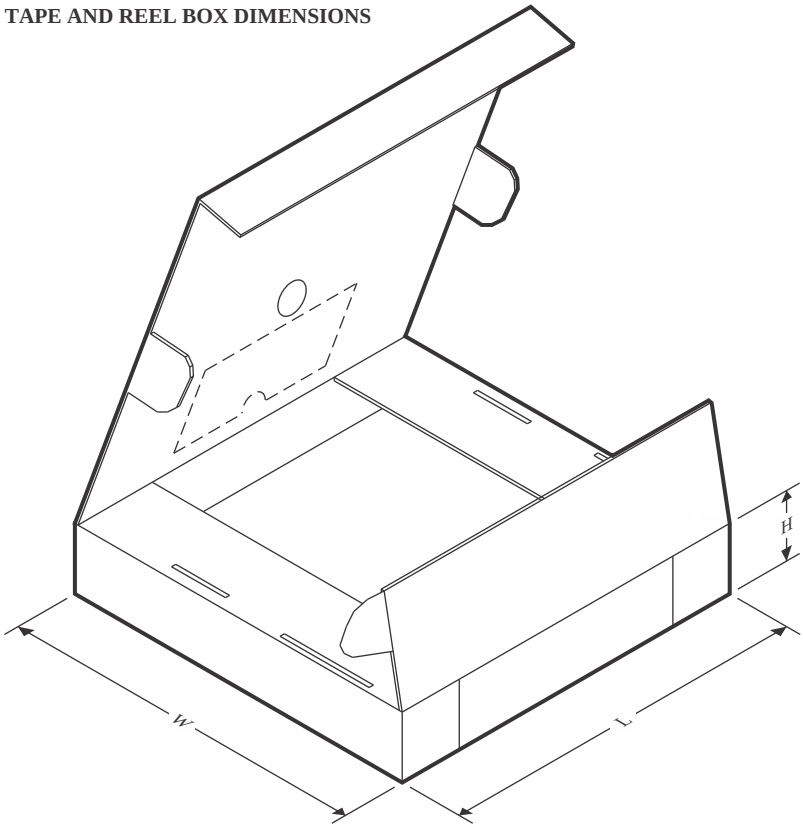
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM1815MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

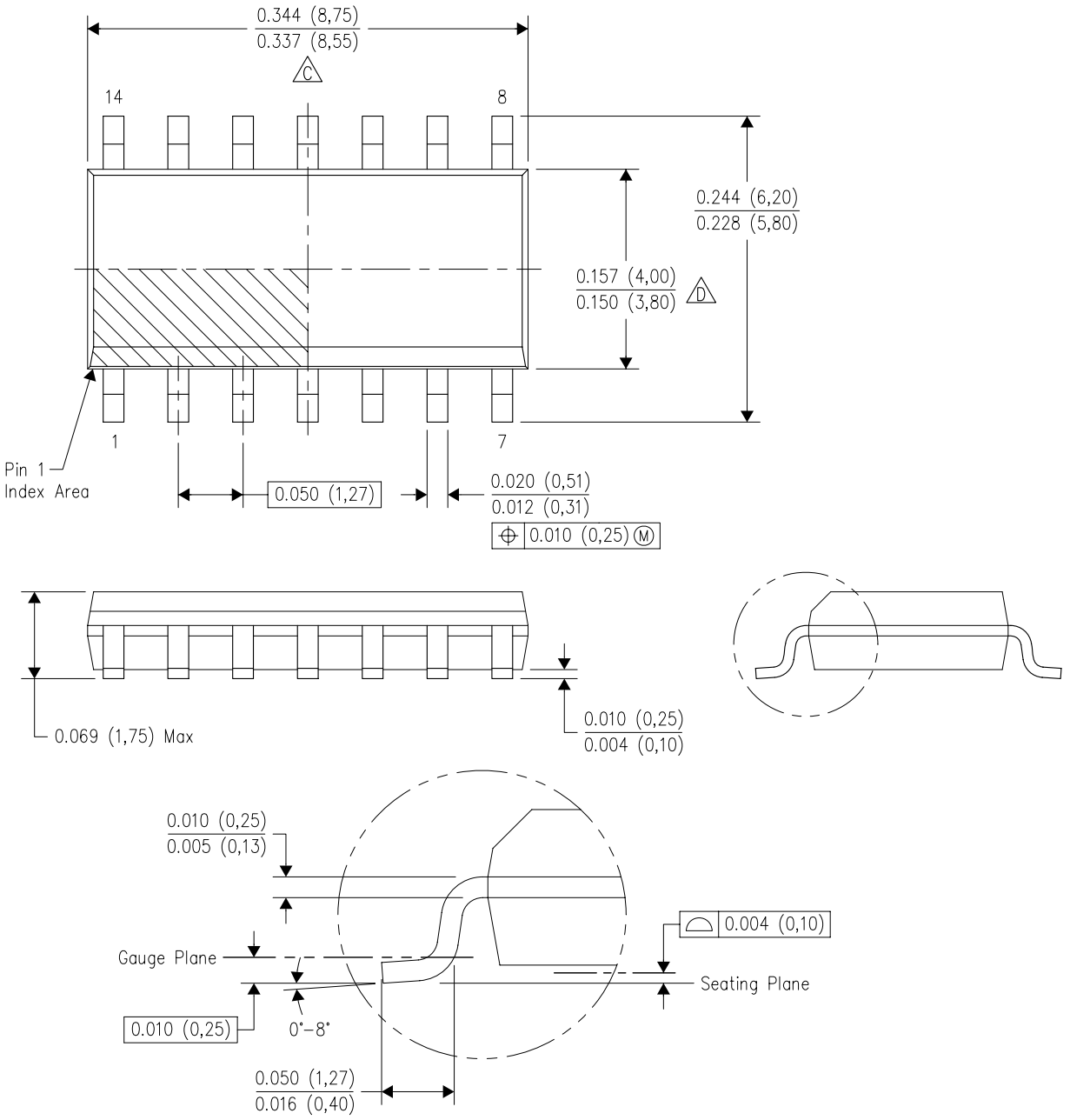
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM1815MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

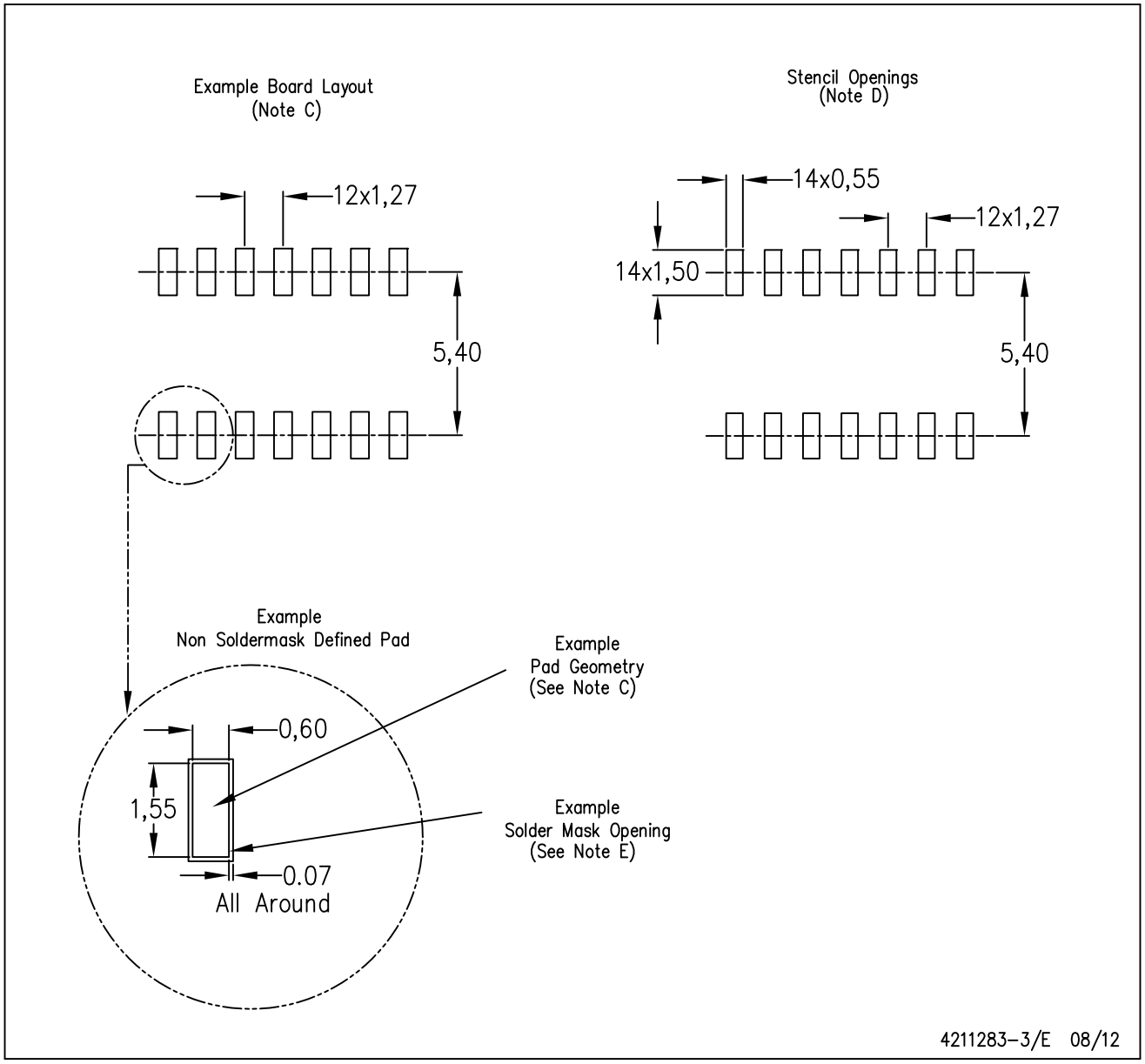
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

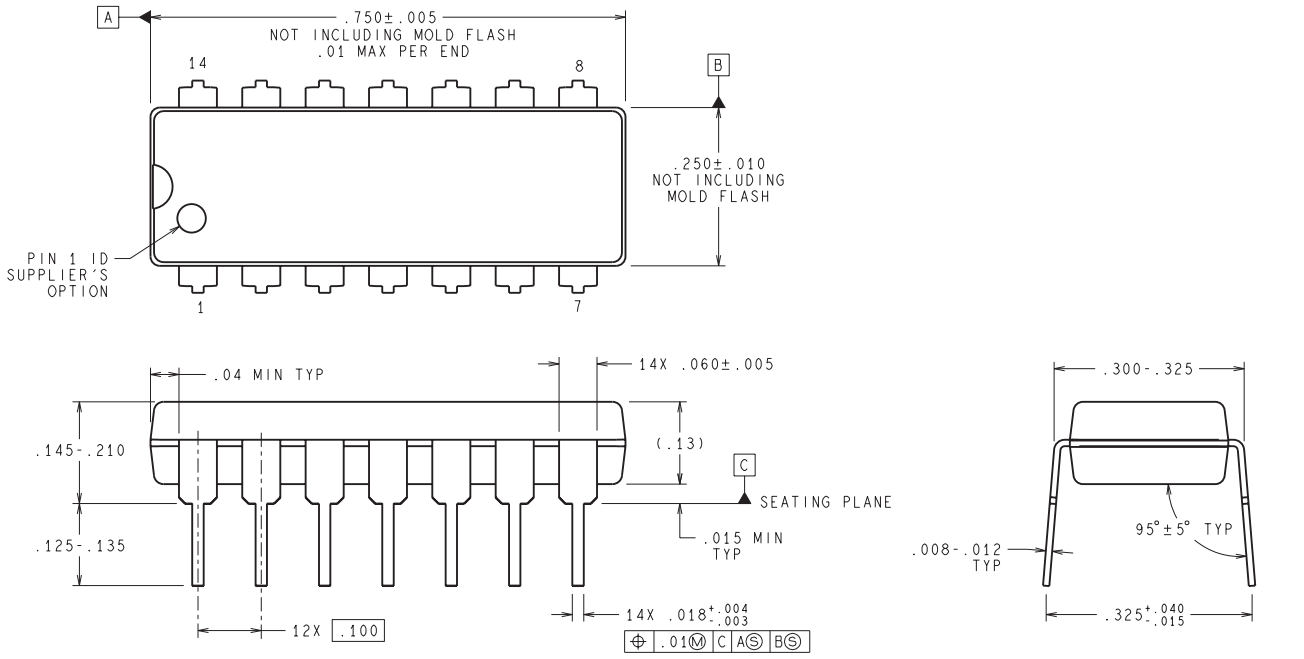
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

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