

1. Features

- SPI Interface with clock speeds up to 50MHz/160MHz for high throughput applications
- IEEE 802.3az Energy Efficient Ethernet (EEE)
- Support interface for EEPROM
- Built-in integrated 3.3V to 1.8V low noise regulator for core and analog blocks
- Supports wake-up on LAN (WOL)
- Integrated 10/100M transceiver With HP Auto-MDIX
- Supports back pressure mode for half-duplex
- IEEE802.3x flow control for full-duplex mode
- Supports wakeup frame, link status change and magic packet events for remote wake up
- Support 100M Fiber interface.
- Integrated 16K Byte SRAM
- Supports IP/TCP/UDP checksum generation and checking
- Supports automatically load vendor ID and product ID from EEPROM
- Optional EEPROM configuration
- Very low power consumption mode:
- EMI (Class B) and HBM ESD Rating 8KV
- Support Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$ (DM9051INP)
- Compatible with 5V/3.3V tolerant I/O
- DSP architecture PHY Transceiver.
- 0.18um process

2. General Description

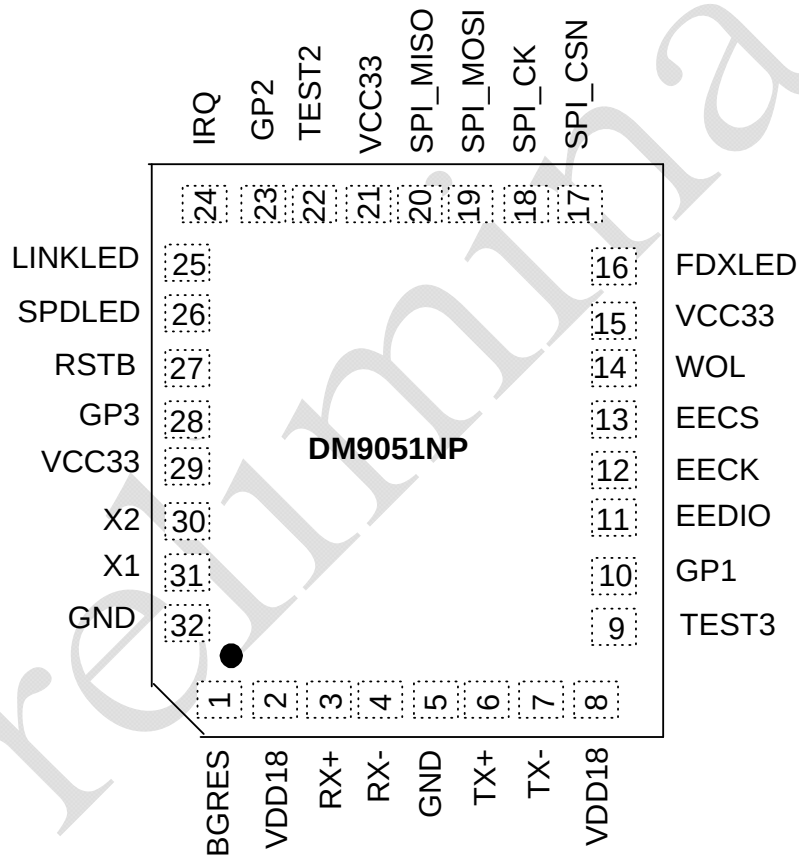
The DM9051 is a fully integrated and cost-effective low pin count single chip Fast Ethernet controller with SPI interface, a 10/100M PHY and 4K Dword SRAM. It is designed with low power and high performance SPI interface that support 5V/3.3V IO tolerance. The DM9051 supports SPI interfaces to internal memory accesses for various processors. The PHY of

the DM9051 can interface to the UTP3, 4, 5 in 10Base-T and UTP5 in 100Base-TX with HP Auto-MDIX. It is fully compliant with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9051 to take the maximum advantage of its abilities. The DM9051 also supports IEEE 802.3x full-duplex flow control.

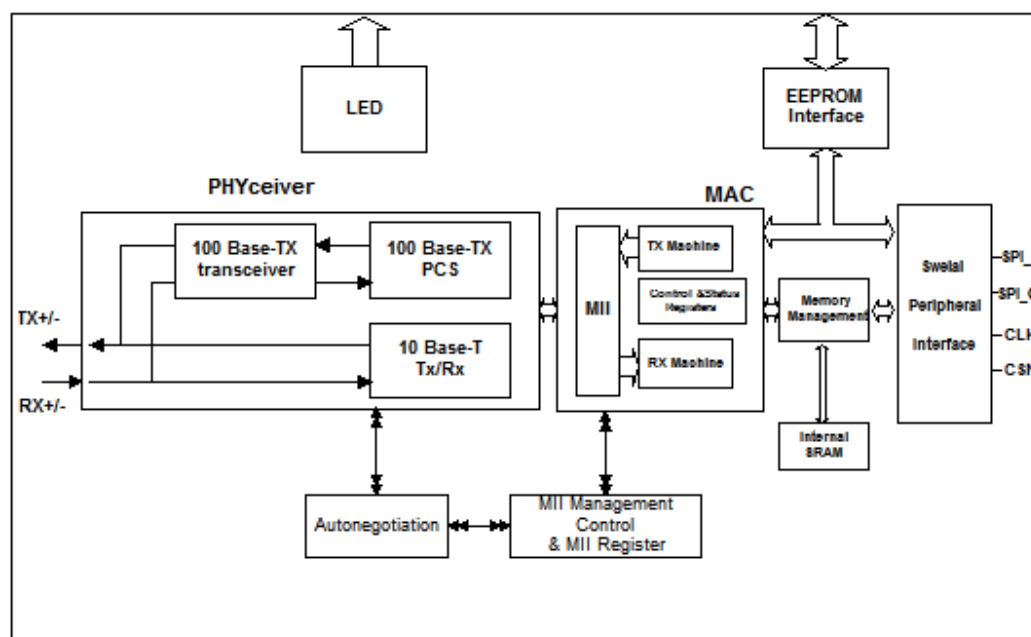
3. Applications

- Smart meter
- Industrial Control Sensor Devices
- Security, Motion Control
- Building Automation
- Voice over IP (VoIP)
- Internet Radio

4. Pin Configuration



5. Block Diagram



6. Order Information

Part Number	Pin Count	Package
DM9051NP	32	QFN
DM9051INP	32	QFN

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