

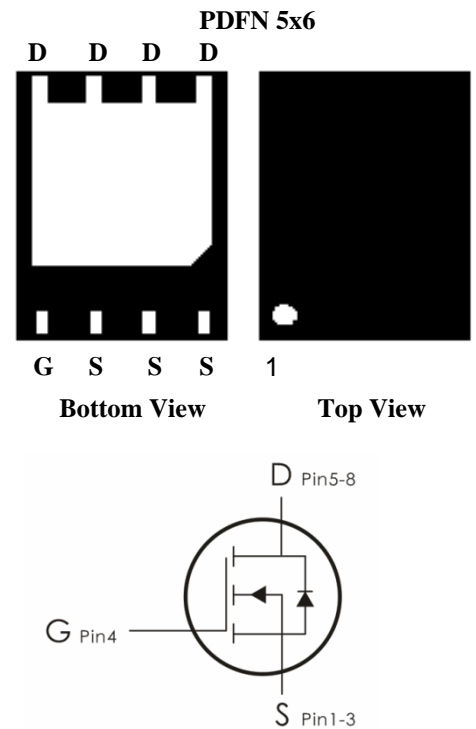
Description:

This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.

Features:

- 1) $V_{DS}=40V, I_D=270A, R_{DS(on)} < 1.1m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra $R_{DS(on)}$.
- 5) Excellent package for good heat dissipation.



Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage ⁶	± 20	V
I_D	Drain Current- $T_C=25^\circ C$ (Silicon Limited)	270	A
	Drain Current- $T_C=25^\circ C$	100	
I_{DM}	Pulsed Drain Current ¹	350	
E_{AS}	Single Pulse Avalanche Energy ⁵	256	mJ
P_D	Power Dissipation	138.8	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.9	$^\circ C/W$
$R_{\theta JA}^*$	Thermal Resistance Junction to ambient ³	25	$^\circ C/W$

Package Marking and Ordering Information:

Part NO.	Marking	Package
N1D1R1NG	D1R1N	PDFN5*6-8

Electrical Characteristics: ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250 \mu A$	40	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS}=0V, V_{DS}=32V$	---	---	25	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0A$	---	---	± 100	nA
On Characteristics						
$V_{GS(th)}$	GATE-Source Threshold Voltage	$V_{GS}=V_{DS}, I_D=250 \mu A$	1	---	2.2	V
$R_{DS(on)}$	Drain-Source On Resistance ²	$V_{GS}=10V, I_D=20A$	---	0.7	1.1	m Ω
		$V_{GS}=4.5V, I_D=20A$	---	1.4	1.85	
G_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=20A$		120		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20V, V_{GS}=0V, f=1MHz$	---	11600	18560	pF
C_{oss}	Output Capacitance		---	1330		
C_{rss}	Reverse Transfer Capacitance		---	40		
R_g	Gate Resistance	$f=1.0MHz$		3	6	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=20V, V_{GS}=10V, I_D=30A, R_G=1.6 \Omega$	---	15		ns
t_r	Rise Time		---	64		ns
$t_{d(off)}$	Turn-Off Delay Time		---	140		ns
t_f	Fall Time		---	22		ns
Q_g	Total Gate Charge	$V_{GS}=10V, V_{DS}=20V, I_D=20A$	---	172	275	nC
Q_{gs}	Gate-Source Charge		---	30		nC
Q_{gd}	Gate-Drain "Miller" Charge		---	17		nC
Drain-Source Diode Characteristics						

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SD}	Source-Drain Diode Forward Voltage ²	$V_{GS}=0V, I_S=20A$	---		1.3	V
trr	Continuous Source Current	$I_S=20A, V_{GS}=0V$ $di/dt=100A/\mu s$	---	54		ns
qrr	Pulsed Source Current		---	80		nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 60°C/W at steady state.
4. Package limitation current is 100A .
5. Starting $T_j=25^\circ\text{C}$, $V_{DD}=30V$, $L=0.5\text{mH}$, $R_G=25\Omega$
6. The negative V_{GS} rating of N-ch device is for low duty cycle pulse event only.

Typical Characteristics: ($T_C=25^\circ\text{C}$ unless otherwise noted)

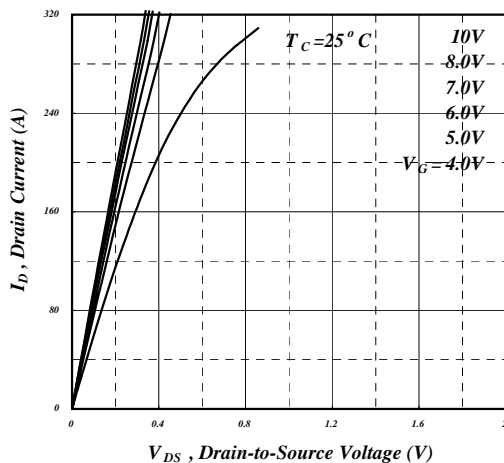


Fig 1. Typical Output Characteristics

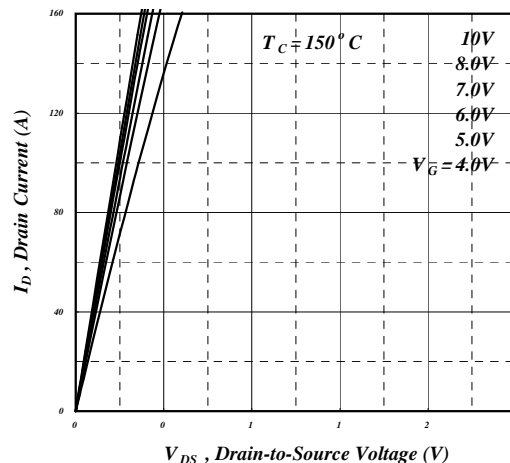


Fig 2. Typical Output Characteristics

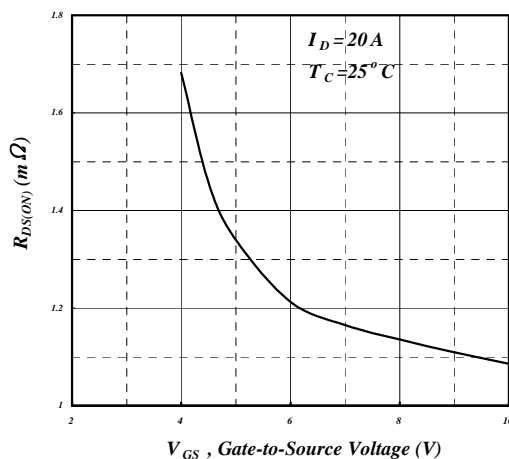


Fig 3. On-Resistance v.s. Gate Voltage

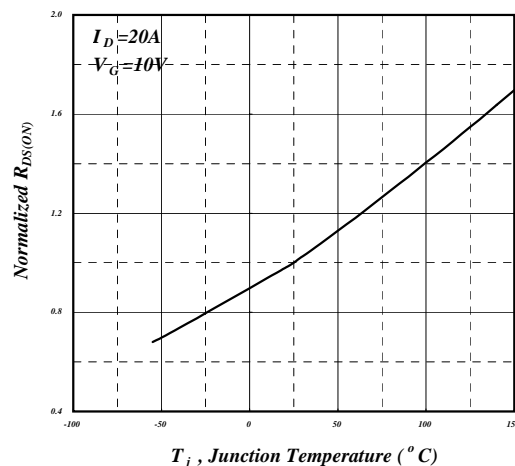


Fig 4. Normalized On-Resistance v.s. Junction Temperature

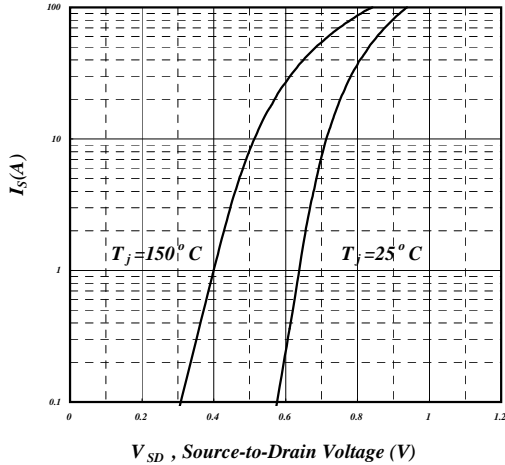


Fig 5. Forward Characteristic of Reverse Diode

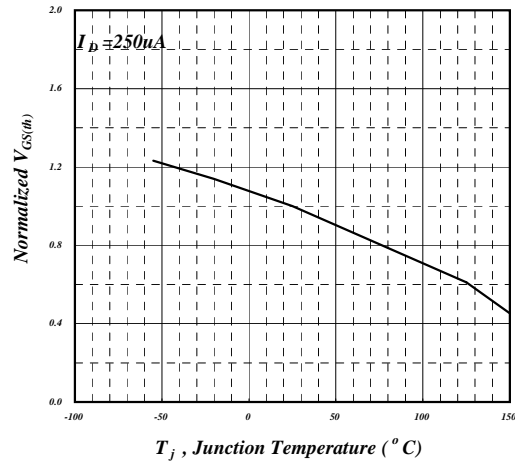


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

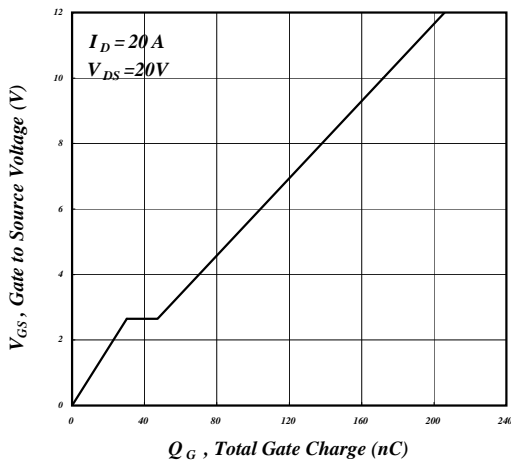


Fig 7. Gate Charge Characteristics

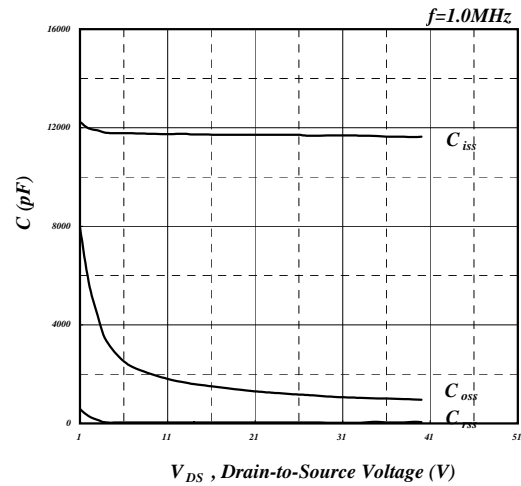


Fig 8. Typical Capacitance Characteristics

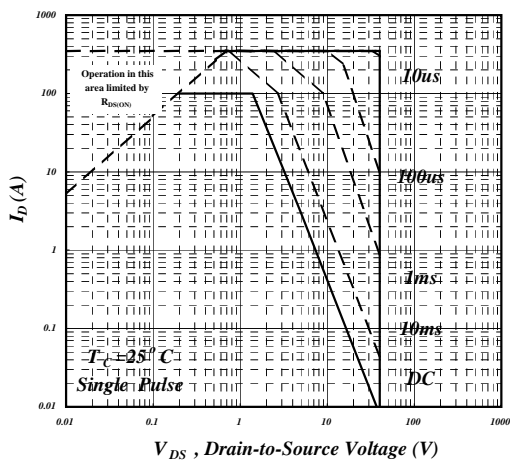


Fig 9. Maximum Safe Operating Area

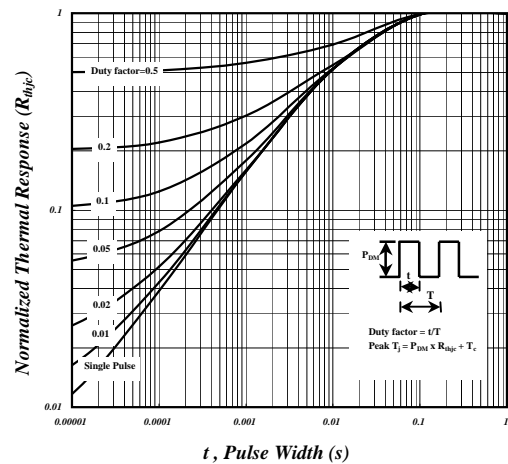


Fig 10. Effective Transient Thermal Impedance

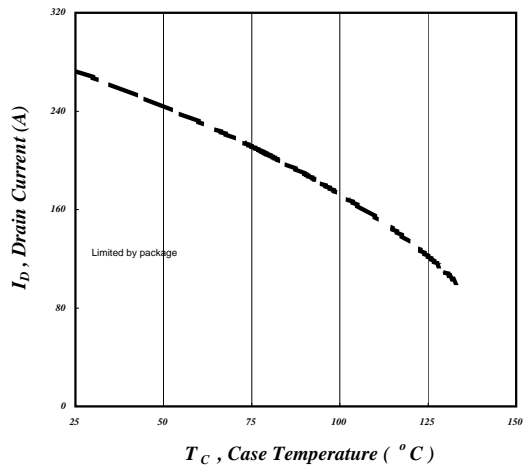


Fig 11. Drain Current v.s. Case Temperature

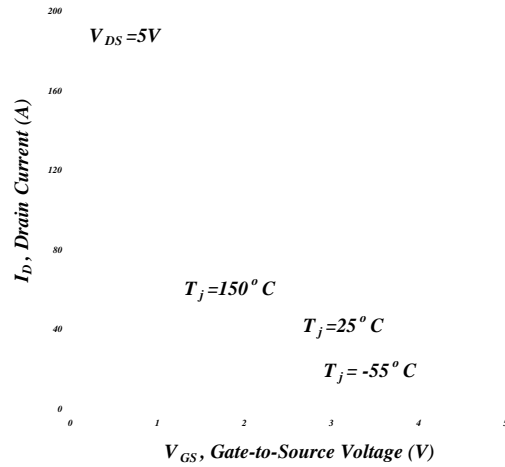


Fig 12. Transfer Characteristics

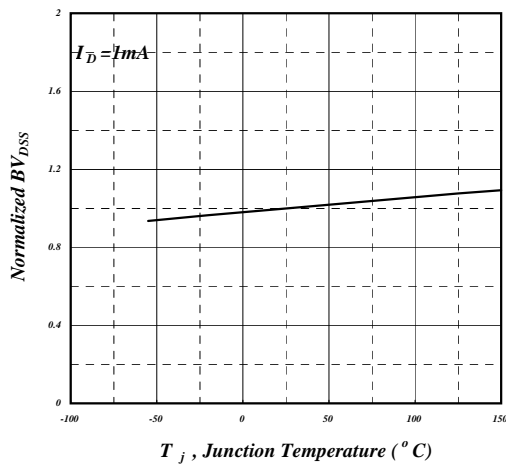


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

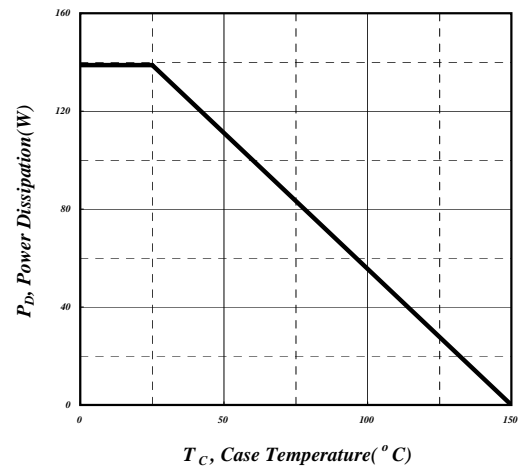
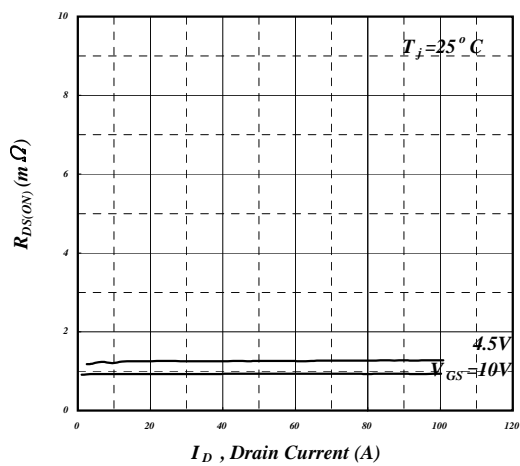


Fig 14. Total Power Dissipation



Resistance