12ns, Single Supply Ground-Sensing Comparator

FEATURES

- Ultra Fast (12ns Typ)
- Operates off **Single** +5V Supply or ±5V
- Input Common Mode Extends to Negative Supply
- No Minimum Input Slew Rate Requirement
- Complementary TTL Output
- Inputs Can Exceed the Positive Supply Up to +15V without Damaging the Comparator
- Low Offset Voltage
- Pin-Compatible with LT1016
- Output Latch Capability

APPLICATIONS

- High Speed A/D Converters
- Zero Crossing Detectors
- Current Sense for Switching Regulators
- Extended Range V to F Converters
- Fast Pulse Height/Width Discriminators
- High Speed Triggers
- Line Receivers
- High Speed Sampling Circuits

DESCRIPTION

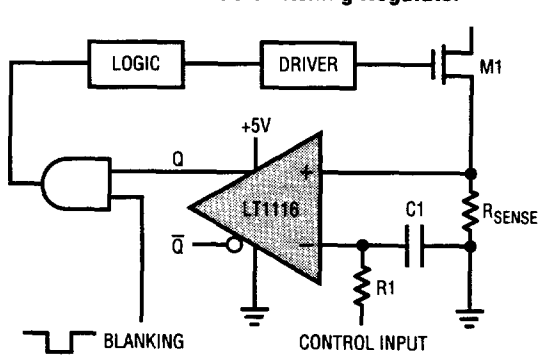
The LT1116 is an ultra fast (12ns) comparator designed for sensing signals near the negative supply. The input common mode range extends from 2.5V below the positive supply down to the negative supply rail. Like the LT1016, this comparator is specifically designed to interface directly to TTL logic with complementary outputs. The comparator may operate from either a single +5V supply or dual ±5V supplies. Tight offset voltage specifications and high gain allow the LT1116 to be used in precision applications.

The LT1116 is designed for improved speed and stability for a wide range of operating conditions. The output stage provides active drive in both directions for maximum speed into TTL logic or passive loads, yet it has minimal cross-conduction current. Unlike other fast comparators, the LT1116 remains stable even for slow transitions through the active region, which eliminates the need to specify a minimum input slew rate.

The LT1116 has an internal, TTL compatible latch for retaining data at the outputs. The latch holds data as long as the latch pin is held high. Device parameters such as gain, offset, and negative power supply current are not significantly affected by variations in negative supply voltage.

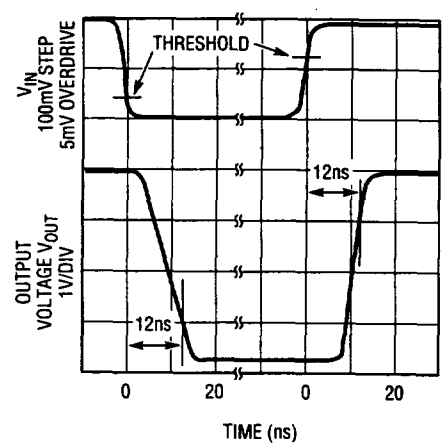
TYPICAL APPLICATION

Fast Current Comparator for Current Mode Switching Regulator



LT1116 • TA01

Comparator Response Time



LT1116 • TA02

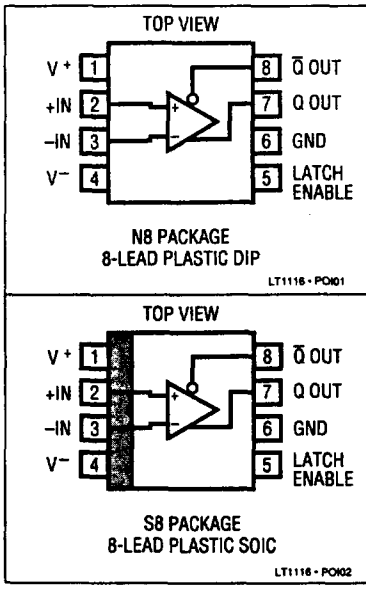
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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND 7V
Negative Supply Voltage (V^-) ..... –7V to GND Voltage
Differential Input Voltage ..... ±15V
Inputs Voltage (Either Input) ..... (V^-) –0.3V to 15V
Latch Pin Voltage ..... Equal to Supplies
Output Current (Continuous) ..... ±20mA
Operating Temperature Range
LT1116C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1116CN8
LT1116CS8
S8 PART MARKINGS
1116

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = -5V$, V_{OUT} (Q) = 1.4V, LATCH = 0V, $T_A = 25°C$.
Specifications for V_{OS}, I_B, CMRR, and Voltage Gain are valid for single supply operation, $V^+ = 5V$, $V^- = 0V$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS		LT1116 MIN	LT1116 TYP	LT1116 MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 2)			1.0	±3.0	mV
			•			3.5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		•		5		$\frac{\mu V}{°C}$
I_{OS}	Input Offset Current	(Note 2)	•		0.5	2	µA
I_B	Input Bias Current, Sourcing	(Note 3)	•		10	20	µA
	Input Voltage Range	Arbitrary Supply Range	•	V^-		(V^+) –2.5	V
		Single +5V Supply	•	0		2.5	V
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 2.5V$, $V_S = \pm 5V$	•	75	90		dB
		$0V \le V_{CM} \le 2.5V$	•	65	90		dB
PSRR	Power Supply Rejection Ratio	Positive Supply $4.6V \le V^+ \le 5.4V$	•	60	75		dB
		Negative Supply $-7V \le V^- \le -2V$	•	80	100		dB
A_V	Small Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1400	3000		V/V
I+	+Supply Current		•		27	38	mA
I–	–Supply Current		•		5	7	mA
V_{OH}	Output High Voltage	$I_{SOURCE} = 1mA$	•	2.7	3.4		V
		$I_{SOURCE} = 10mA$	•	2.4	3.0		V
V_{OL}	Output Low Voltage	$I_{SINK} = 4mA$	•		0.3	0.5	V
		$I_{SINK} = 10mA$			0.4		V

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = -5V$, V_{OUT} (Q) = 1.4V, LATCH = 0V, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS		LT1116 MIN	LT1116 TYP	LT1116 MAX	UNITS
V_{IH}	+Latch Threshold		•	2.0			V
V_{IL}	–Latch Threshold		•			0.8	V
I_{IL}	Latch Input Current	V_{LATCH} = 0V	•		–20	–500	µA
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV (Note 4)			12	16	ns
			•			18	ns
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 20mV (Note 4)			10	14	ns
			•			16	ns
Δt_{PD}	Differential Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV (Note 4)				3	ns
t_{SU}	Latch Set-Up Time	(Note 5)			2		ns
t_H	Latch Hold Time	(Note 5)			2		ns

The • denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impared.

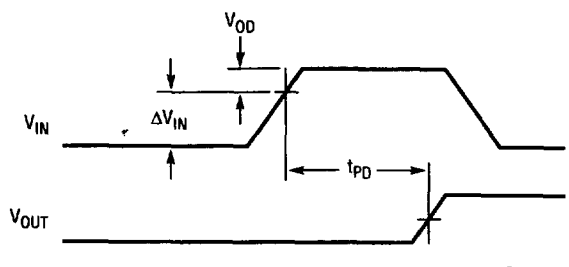
Note 2: Input offset voltage is defined as the average of two offset voltages measured by forcing first the Q output to 1.4V then forcing the $\overline{Q}$ output to 1.4V.

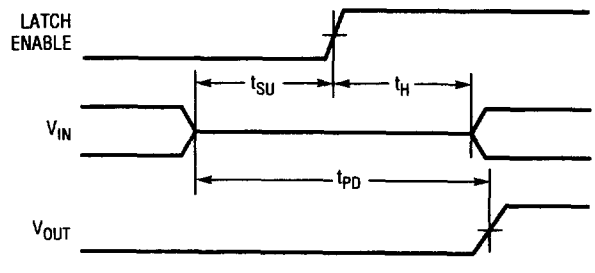
Note 3: Input bias current is defined as the average of the two input currents.

Note 4: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1116 is sample tested with a 1V step and 500mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} can be guaranteed with this test if additional DC tests are performed to verify internal bias conditions are correct. For low overdrive conditions V_{OS} is added to the measured overdrive.

Note 5: Input latch set-up time, t_{SU}, is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time, t_H, is the interval after the latch is asserted in which the input signal must be stable.

TIMING DIAGRAMS

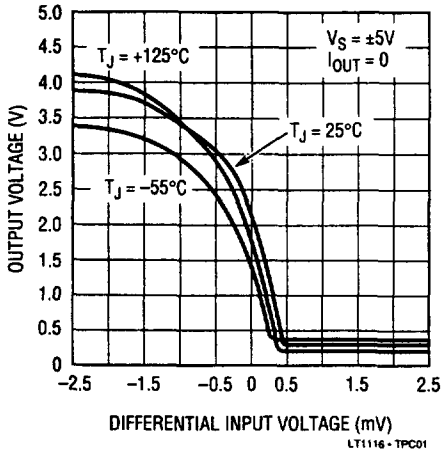




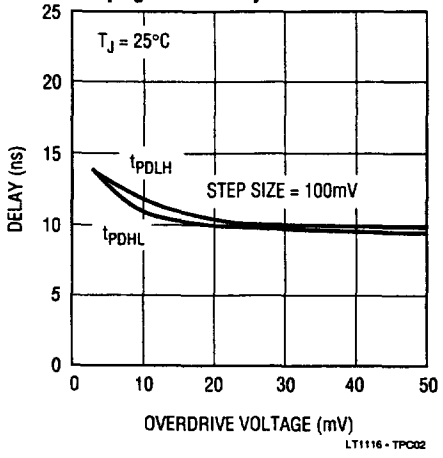
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TYPICAL PERFORMANCE CHARACTERISTICS

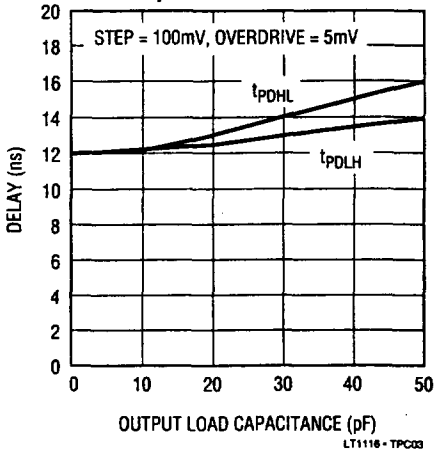
Gain Characteristics



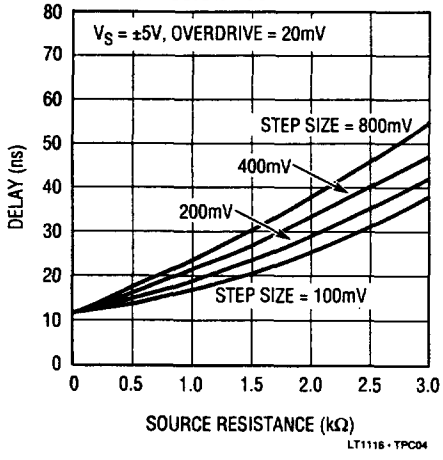
Propagation Delay vs Overdrive



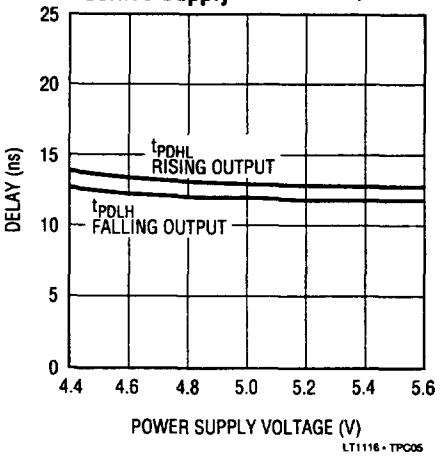
Propagation Delay vs Load Capacitance



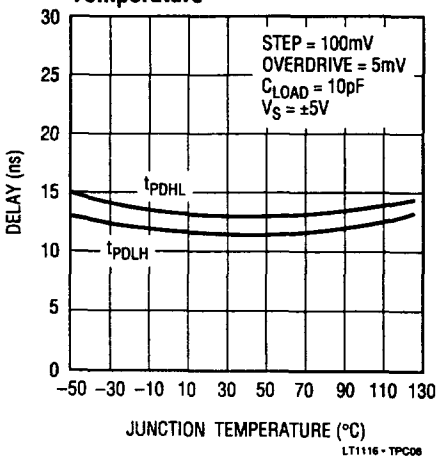
Propagation Delay vs Source Resistance



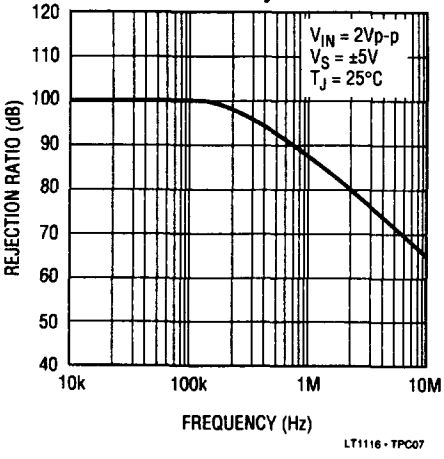
Propagation Delay vs Positive Supply



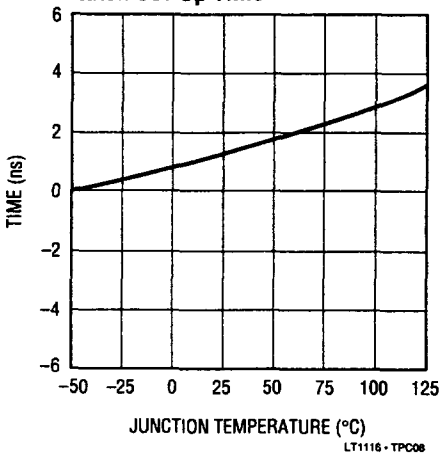
Propagation Delay vs Temperature



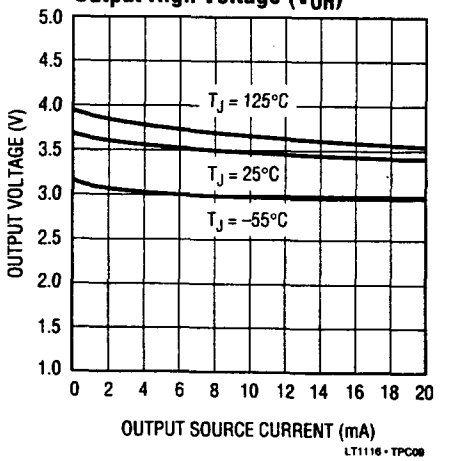
Common Mode Rejection



Latch Set-Up Time

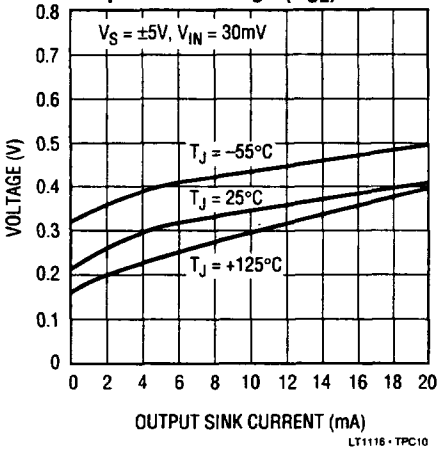


Output High Voltage (V_{OH})

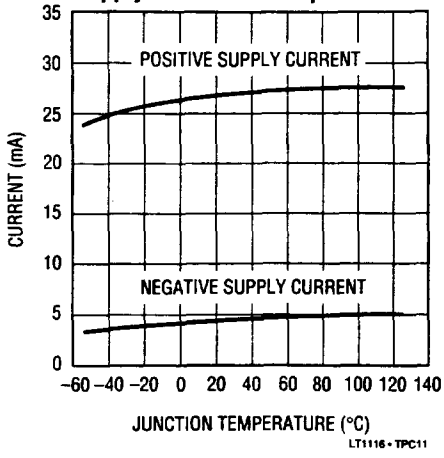


TYPICAL PERFORMANCE CHARACTERISTICS

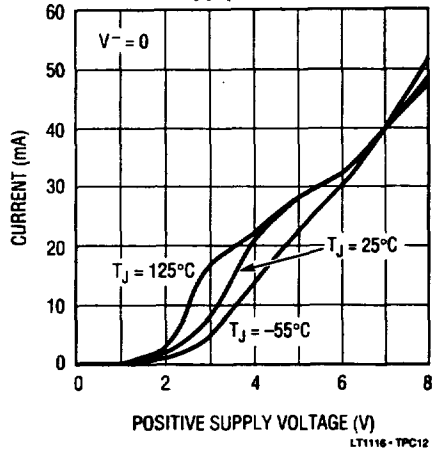
Output Low Voltage (V_{OL})



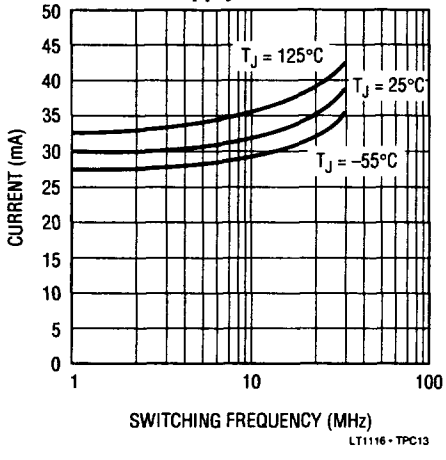
Supply Current vs Temperature



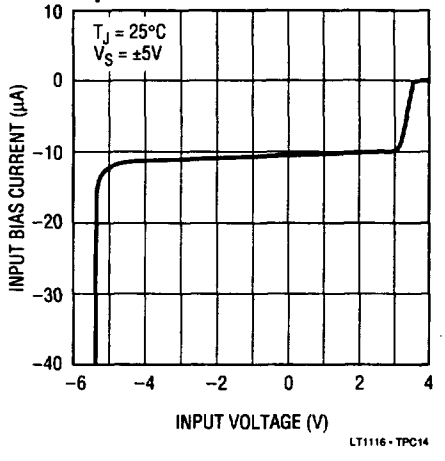
Positive Supply Current



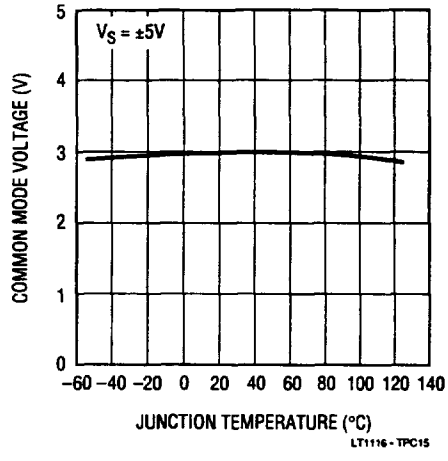
Positive Supply Current



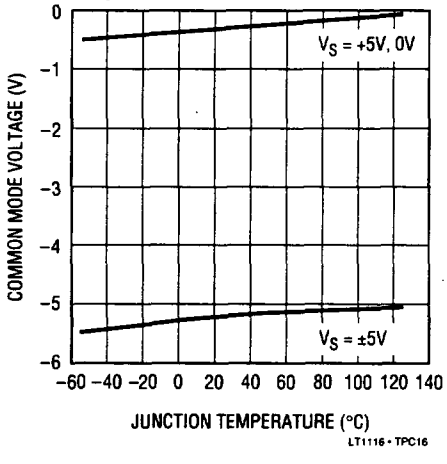
Input Bias Current



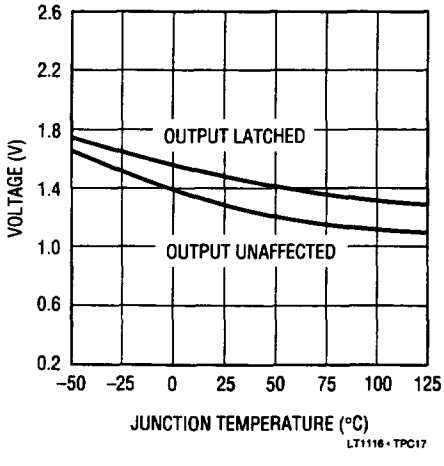
Positive Common Mode Limit



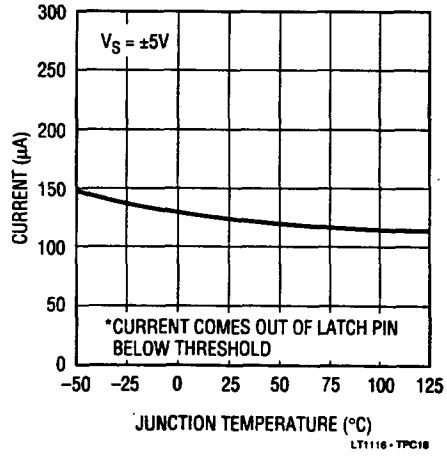
Negative Common Mode Limit



Latch Pin Threshold



Latch Pin Current*



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APPLICATIONS INFORMATION

Common Mode Considerations

The LT1116 is specified for a common mode range of 0V to 2.5V with a single +5V supply, and –5V to 2.5V with ±5V supplies. The common mode range is defined as the DC input for which the output responds correctly to small changes in the input differential. Input signals can exceed the positive common mode limit up to the 15V absolute maximum rating without damaging the comparator. There will, however, be an increase in propagation delay of up to 10ns when the input signal switches back into the common mode range. When input signals fall below the negative common mode limit, the internal PN diode formed with the substrate can turn on resulting in significant charge flow throughout the die. A Schottky clamp diode between the input and the negative rail speeds up recovery from negative overdrive by preventing the substrate diode from turning on. The zero crossing detector in Figure 1 demonstrates the use of a fast clamp diode. Recovery from 500mV overdrive below V^- for this circuit is approximately 18ns.

Input Characteristics

Each input to the LT1116 is buffered with a fast PNP follower — input bias current therefore does not vary significantly throughout the common mode range. When either input exceeds the positive common mode limit, the bias current drops to zero. Inputs that fall more than one diode drop below V^- will forward bias the substrate or clamp diode, and will cause large input current to flow.

Fast Zero Crossing Detector

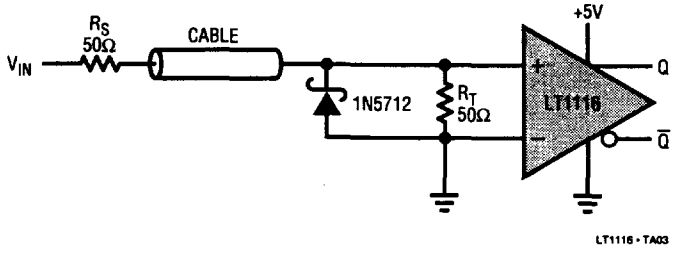


Figure 1. The zero crossing detector terminates the transmission line at its 50Ω characteristic impedance. Negative inputs should not fall below –2V to keep the signal current within the clamp diode's maximum forward rating. Positive inputs should not exceed the devices absolute maximum ratings nor the power rating on the terminating resistor.

Single ended input resistance is about 5MΩ, and remains roughly constant over the input common mode range. The common mode resistance is about 2.5MΩ with zero differential input voltage, and does not change significantly with the absolute value of difierential input.

Effective input capacitance, typically 5pF, is determined by measuring the resulting change in propagation delay for a 1kΩ change in source resistance.

Latch Pin Dynamics

The internal latch uses local regenerative feedback to shorten set-up and hold times. Driving the latch pin high retains the output state. The latch pin floats to a high state when disconnected, so it must be driven low for flow-through operation. The set-up time required to guarantee detecting a given transition of the inputs is 2ns. The inputs must also remain stable for a 2ns hold time after latch is asserted. New data will appear at the output approximately 10ns to 12ns after the latch goes low. The latch pin has no built-in hysteresis, and is designed to be driven from TTL or CMOS logic gates.

Additional Information

Linear Technology's Application Note 13 provides an extensive discussion of design techniques for high speed comparators.

Single Supply Crystal Oscillator 10MHz-15MHz

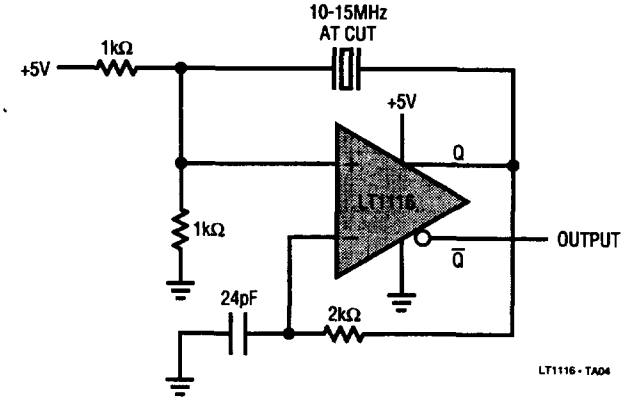


Figure 2. This single supply crystal oscillator utilizes crystals from 10MHz to 15MHz without component changes.

APPLICATIONS INFORMATION

High Speed Adaptive Trigger Circuit

Line receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 3 triggers on 2mV to 200mV signals from 100Hz to 10MHz from a single 5V rail. The trigger level is the average of the input signal's positive and negative peaks stored on 0.005µF capacitors. Pairs of NPN and PNP transistors are used instead of diodes to temperature compensate the peak detector.

To achieve single supply operation, the input signal must be shifted into the pre-amplifier's common mode range. The input amplifier A1, adds a 1V level shift, while A2 provides a gain of 20 for high frequency signals. Capacitors C1 and C2 insure that low frequency signals see unity gain. Bandwidth limiting in A1 and A2 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

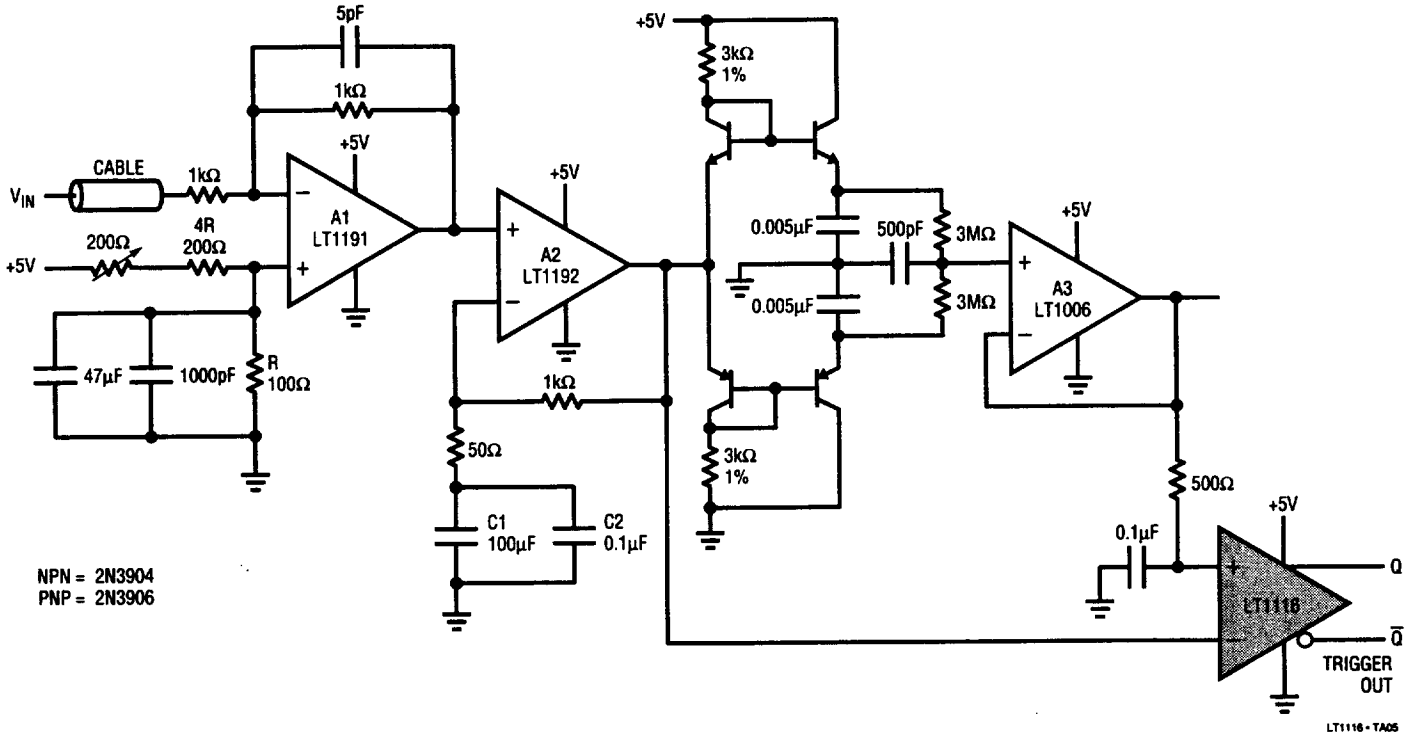


Figure 3. Fast Single Supply Adaptive Trigger