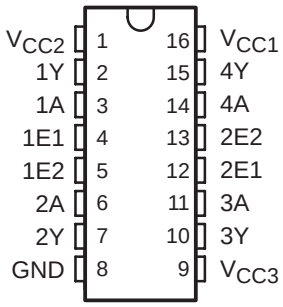
- **Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range From 5 V to 24 V**
- **Low Standby Power Dissipation**
- **V_{CC3} Supply Maximizes Output Source Voltage**

D OR N PACKAGE
(TOP VIEW)



description/ordering information

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

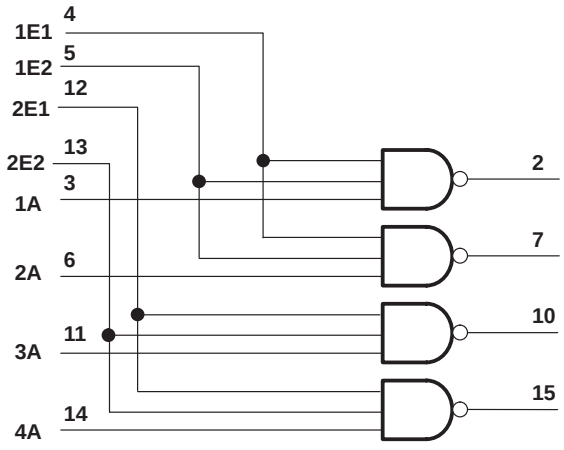
The outputs can be switched very close to the V_{CC2} supply rail when V_{CC3} is about 3 V higher than V_{CC2}. V_{CC3} also can be tied directly to V_{CC2} when the source voltage requirements are lower.

ORDERING INFORMATION

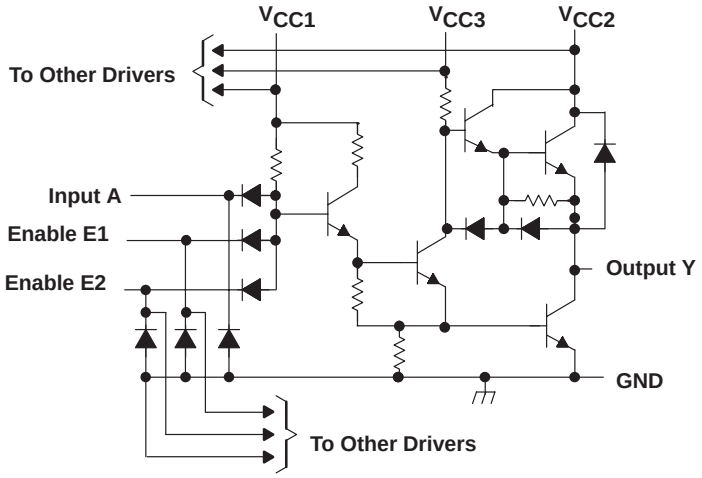
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	SN75374N	SN75374N
	SOIC (D)	Tube of 40	SN75374D	SN75374
		Reel of 2500	SN75374DR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram (positive logic)



schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1): V_{CC1} . . . . . −0.5 V to 7 V
V_{CC2} . . . . . −0.5 V to 25 V
V_{CC3} . . . . . −0.5 V to 30 V
Input voltage, V_I . . . . . 5.5 V
Peak output current, I_I (t_W < 10 ms, duty cycle < 50%) . . . . . 500 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 73°C/W
N package . . . . . 67°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage	4.75	5	5.25	V
V_{CC2}	Supply voltage	4.75	20	24	V
V_{CC3}	Supply voltage	V_{CC2}	24	28	V
$V_{CC3} - V_{CC2}$	Voltage difference between supply voltages	0	4	10	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−10	mA
I_{OL}	Low-level output current			40	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

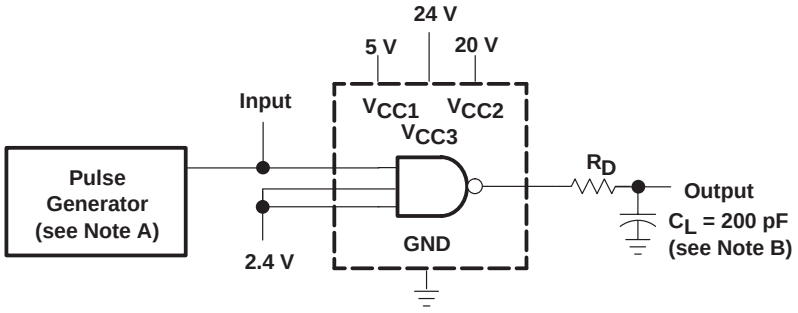
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA					−1.5	V
V_{OH}	High-level output voltage		$V_{CC3} = V_{CC2}$ + 3 V,	V_{IL} = 0.8 V,	I_{OH} = −100 µA	V_{CC2} − 0.3	V_{CC2} − 0.1		V
			$V_{CC3} = V_{CC2}$ + 3 V,	V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2} − 1.3	V_{CC2} − 0.9		
			$V_{CC3} = V_{CC2}$,	V_{IL} = 0.8 V,	I_{OH} = −50 µA	V_{CC2} − 1	V_{CC2} − 0.7		
			$V_{CC3} = V_{CC2}$,	V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2} − 2.5	V_{CC2} − 1.8		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 10 mA			0.15	0.3	V
			V_{CC2} = 15 V to 28 V,	V_{IH} = 2 V,	I_{OL} = 40 mA		0.25	0.5	
V_F	Output clamp-diode forward voltage		V_I = 0,	I_F = 20 mA				1.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V					1	mA
I_{IH}	High-level input current	Any A	V_I = 2.4 V					40	µA
		Any E						80	
I_{IL}	Low-level input current	Any A	V_I = 0.4 V				−1	−1.6	mA
		Any E					−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load	V_{CC3} = 28 V,		4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high						−2.2	0.25	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high						2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low		V_{CC1} = 5.25 V, All inputs at 5 V,	V_{CC2} = 24 V, No load	V_{CC3} = 28 V,		31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low							2	
$I_{CC3(L)}$	Supply current from V_{CC1}, all outputs low						16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load	V_{CC3} = 24 V,			0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high							0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		V_{CC1} = 0, All inputs at 0 V,	V_{CC2} = 24 V, No load	V_{CC3} = 24 V,			0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition							0.5	

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, and T_A = 25°C, except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

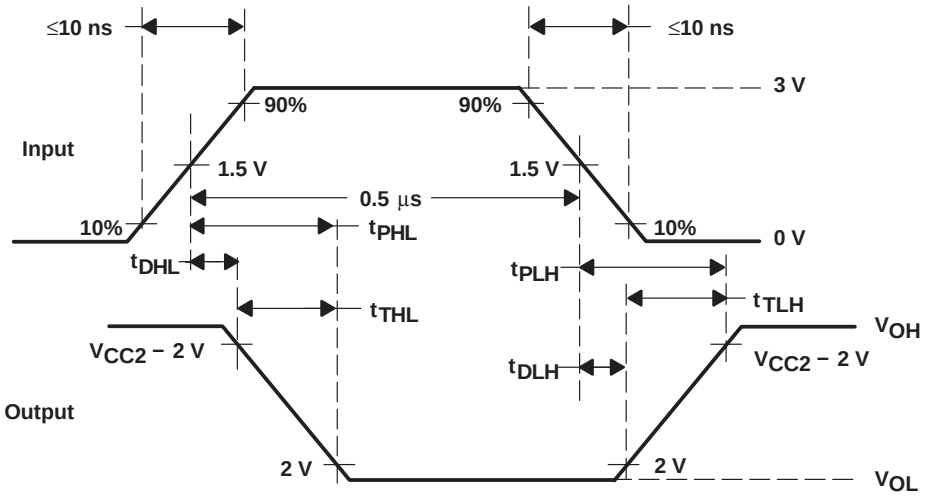
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low- to high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		20	30	ns
t_{DHL}	Delay time, high- to low-level output			10	20	ns
t_{PLH}	Propagation delay time, low- to high-level output		10	40	60	ns
t_{PHL}	Propagation delay time, high- to low-level output		10	30	50	ns
t_{TLH}	Transition time, low- to high-level output			20	30	ns
t_{THL}	Transition time, high- to low-level output			20	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O \approx 50\,\Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

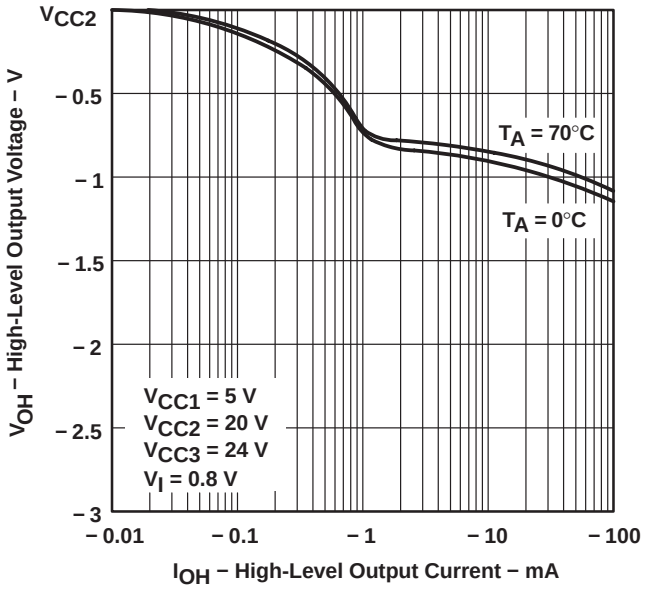


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

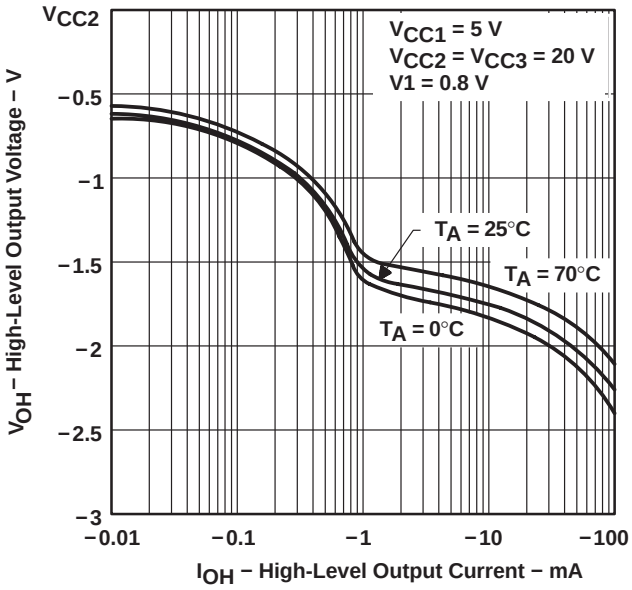


Figure 3

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

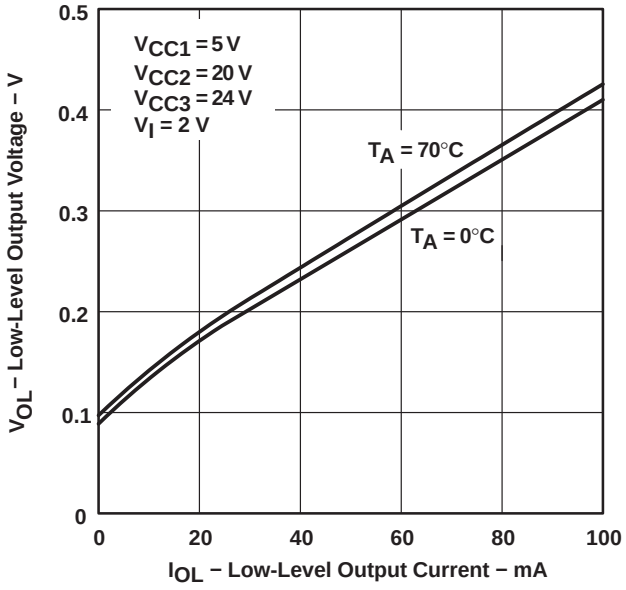


Figure 4

VOLTAGE TRANSFER CHARACTERISTICS

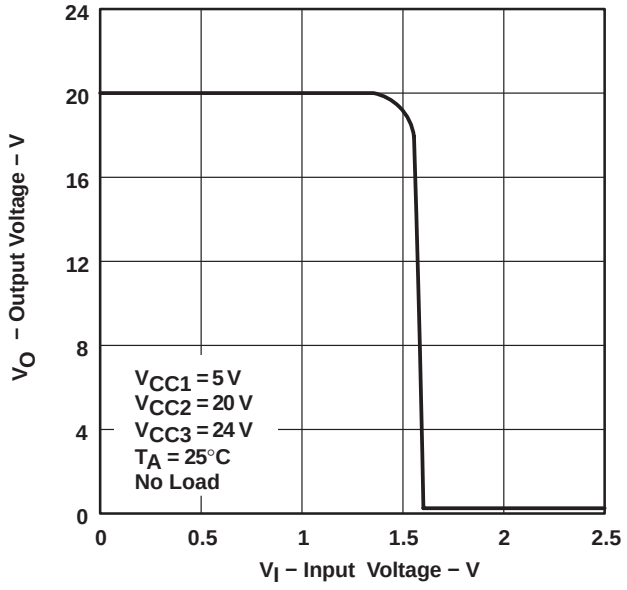


Figure 5

TYPICAL CHARACTERISTICS

**PROPAGATION DELAY TIME
LOW- TO HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE**

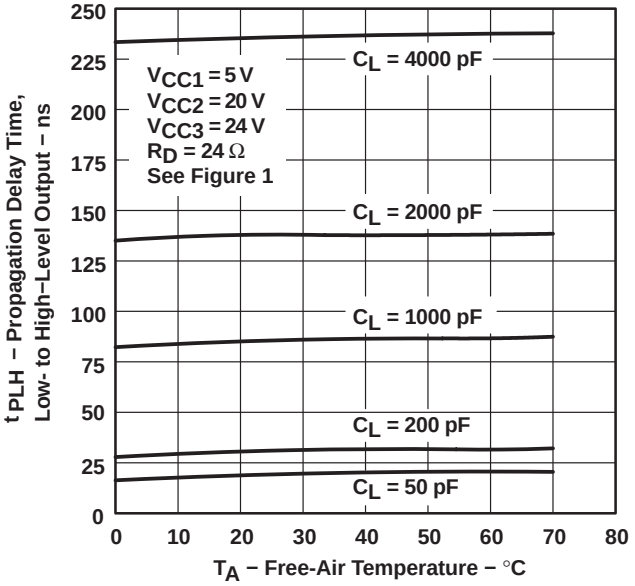


Figure 6

**PROPAGATION DELAY TIME
HIGH- TO LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE**

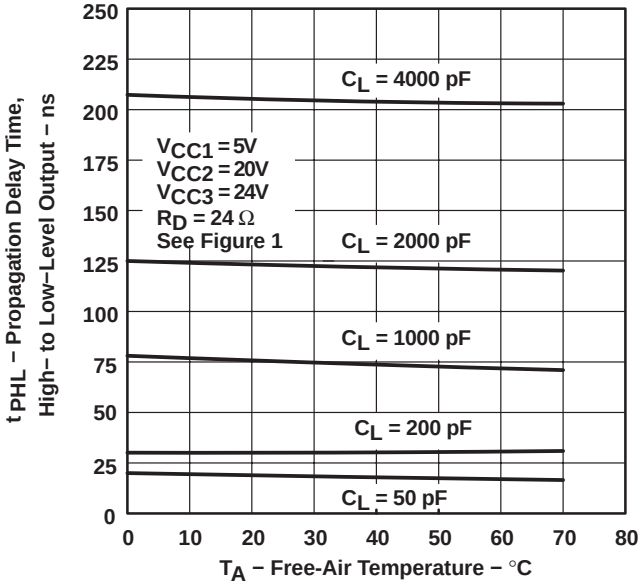


Figure 7

**PROPAGATION DELAY TIME
LOW-TO HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE**

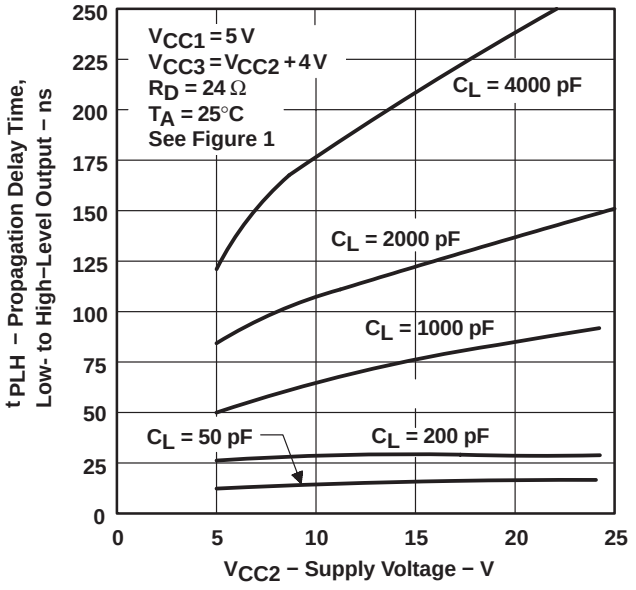


Figure 8

**PROPAGATION DELAY TIME
HIGH- TO LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE**

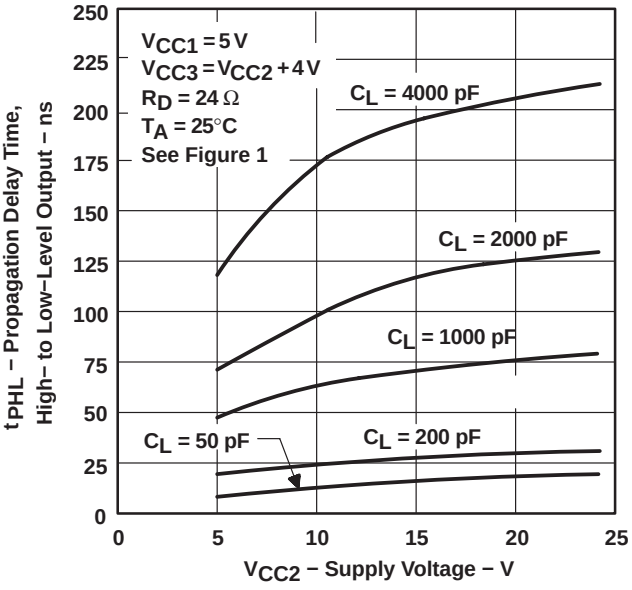


Figure 9

TYPICAL CHARACTERISTICS

**PROPAGATION DELAY TIME
LOW- TO HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE**

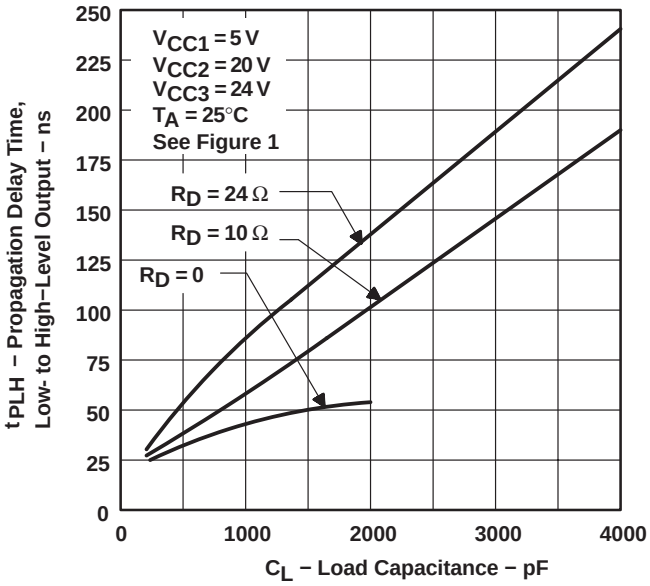


Figure 10

**PROPAGATION DELAY TIME
HIGH- TO LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE**

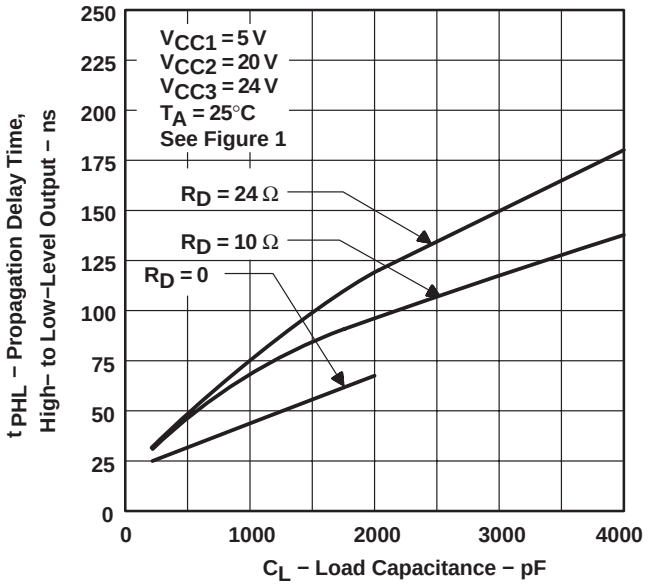


Figure 11

**POWER DISSIPATION (ALL DRIVERS)
vs
FREQUENCY**

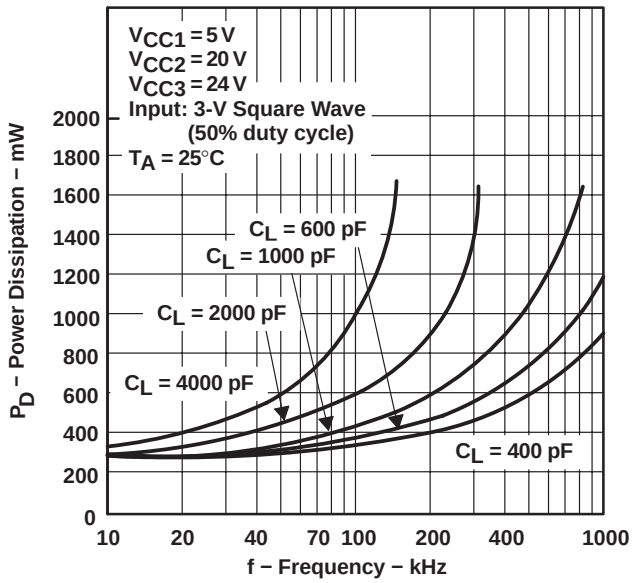


Figure 12

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

THERMAL INFORMATION

power-dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load, and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{(P_H t_H + P_L t_L)}{T}$$

$$P_{C(AV)} \approx CV_c^2 f$$

$$P_{S(AV)} = \frac{(P_{LH} t_{LH} + P_{HL} t_{HL})}{T}$$

where the times are as defined in Figure 15.

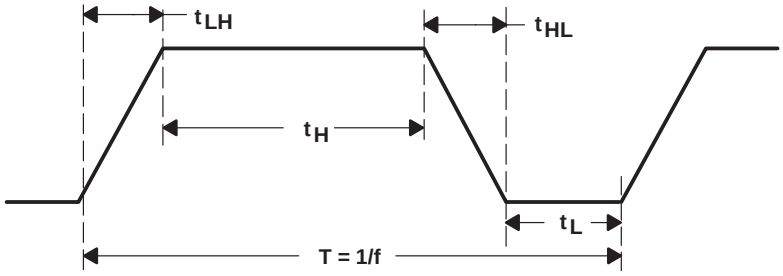


Figure 13. Output-Voltage Waveform

THERMAL INFORMATION

power-dissipation precautions (continued)

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, and C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation:

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz, V_{OH} = 19.9 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_C = 19.75 V, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for C_L < 2000 pF, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is low, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data-sheet values,

$$P_{DC(AV)} = \left[5\ V\left(\frac{4\ mA}{4}\right) + 20\ V\left(\frac{-2.2\ mA}{4}\right) + 24\ V\left(\frac{2.2\ mA}{4}\right)\right] 0.6 +$$

$$\left[5\ V\left(\frac{31\ mA}{4}\right) + 20\ V\left(\frac{0\ mA}{4}\right) + 24\ V\left(\frac{16\ mA}{4}\right)\right] 0.4$$

$P_{DC(AV)}$ = 58.2 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)} = (1000\ pF)(19.75\ V)^2(0.2\ MHz) = 78$ mW per channel

Total power for each driver is:

$P_{T(AV)}$ = 58.2 mW + 78 mW = 136.2 mW

The total package power is:

$P_{T(AV)} = (136.2)(4) = 544.8$ mW

APPLICATION INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of an FET consists of a reverse-biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 14a, an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pullup resistor. The input capacitance (C_{ISS}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time, due to the product of input capacitance and the pullup resistor, is shown in Figure 14b.

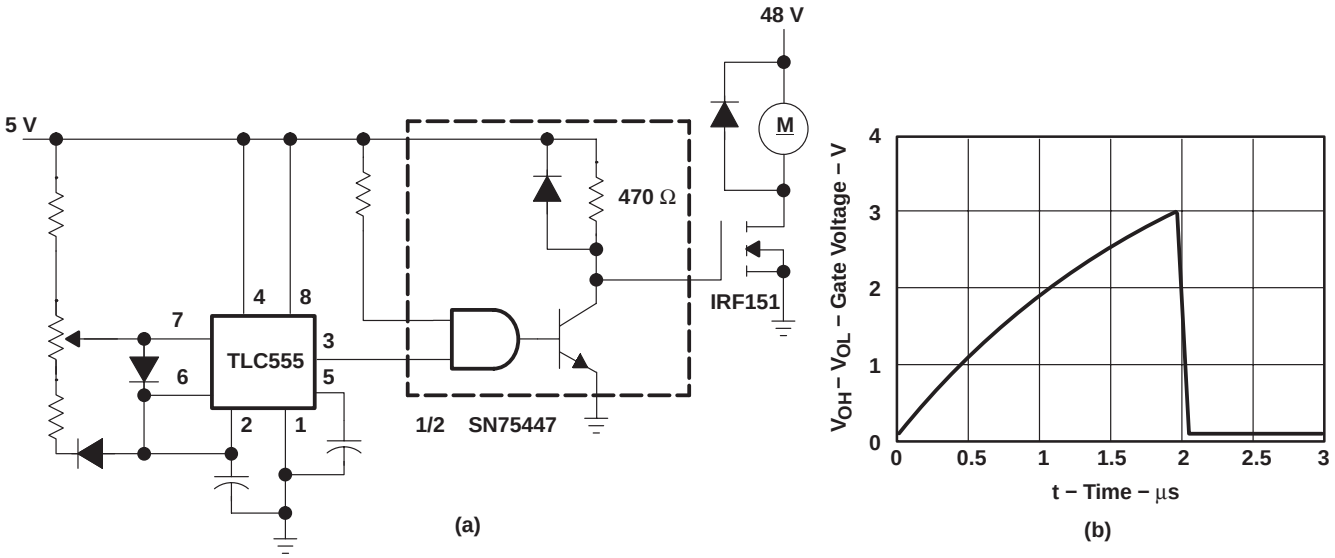


Figure 14. Power MOSFET Drive Using SN75447

A faster, more efficient drive circuit uses an active pullup, as well as an active pulldown output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type (see Figure 15a). The resulting faster switching speeds are shown in Figure 15b.

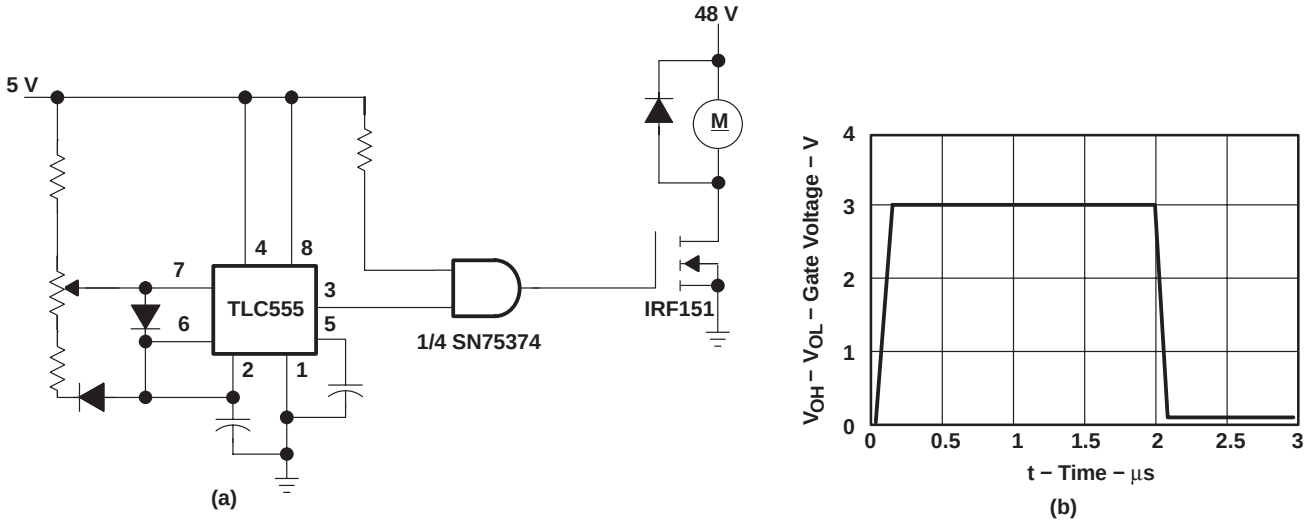


Figure 15. Power MOSFET Drive Using SN75374

APPLICATION INFORMATION

driving power MOSFETs (continued)

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation:

$$I_{PK} = \frac{VC}{t_r}$$

where C is the capacitive load and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14a, V is found by the equation:

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14a is:

$$I_{PK} = \frac{(3 - 0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, V_{CC3} should be at least 3 V higher than V_{CC2}.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75374D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374	Samples
SN75374DE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374	Samples
SN75374DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374	Samples
SN75374DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75374	Samples
SN75374N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75374N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

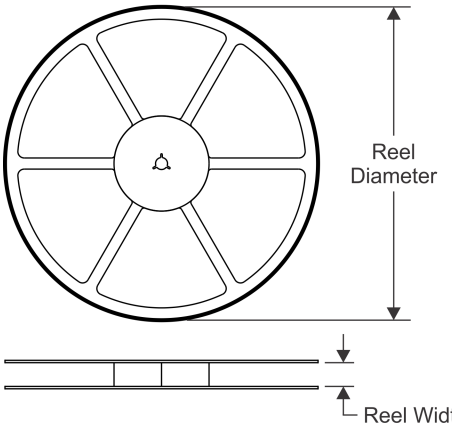
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

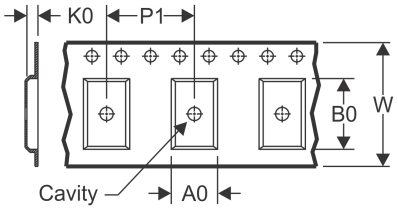
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

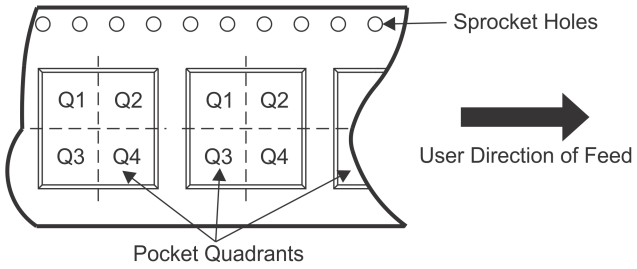


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

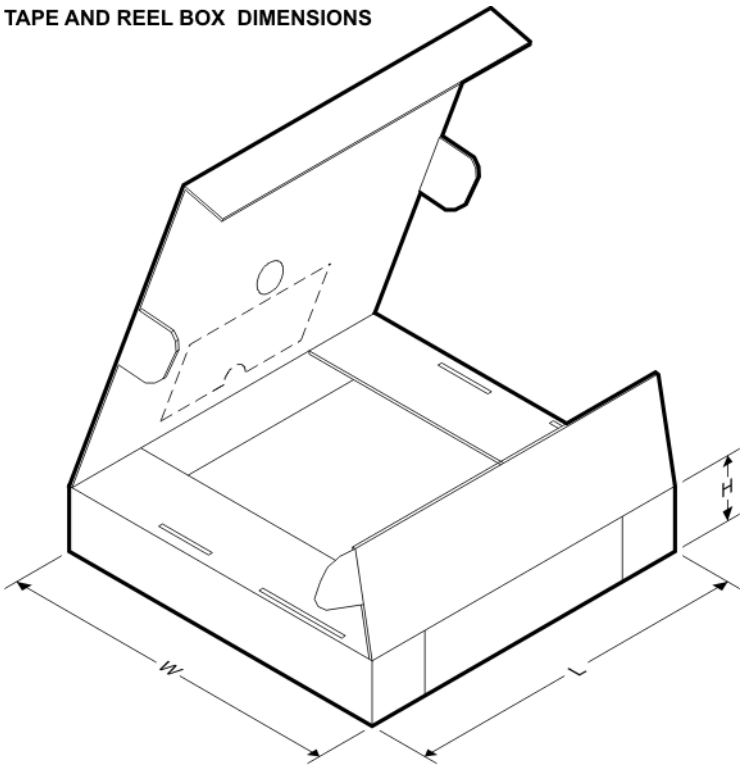
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75374DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

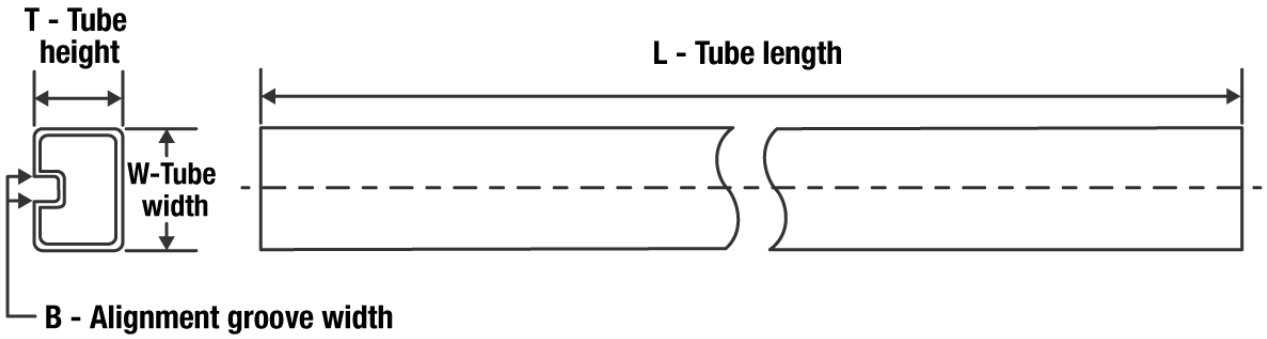
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75374DR	SOIC	D	16	2500	340.5	336.1	32.0

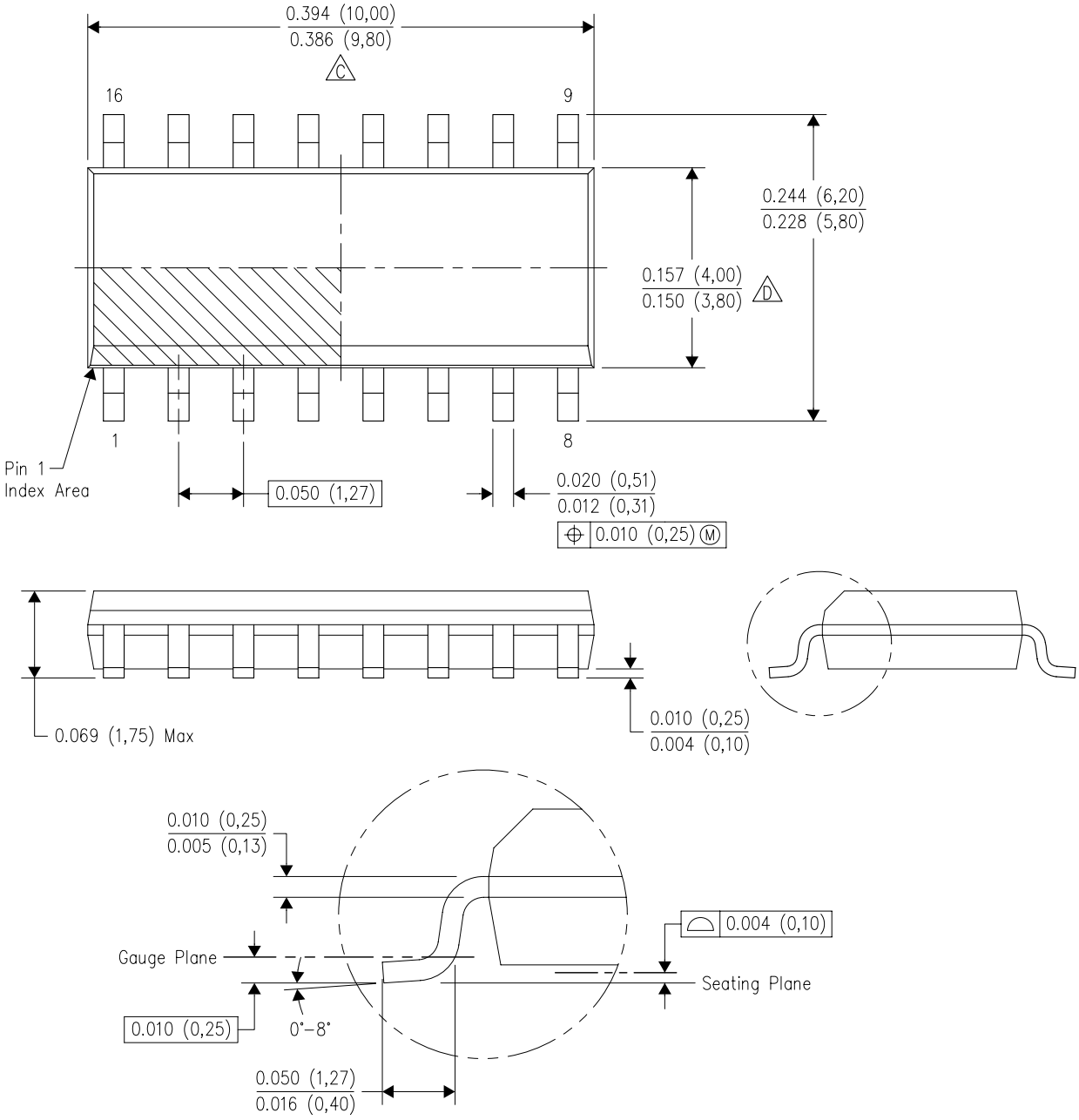
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75374D	D	SOIC	16	40	507	8	3940	4.32
SN75374DE4	D	SOIC	16	40	507	8	3940	4.32
SN75374N	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

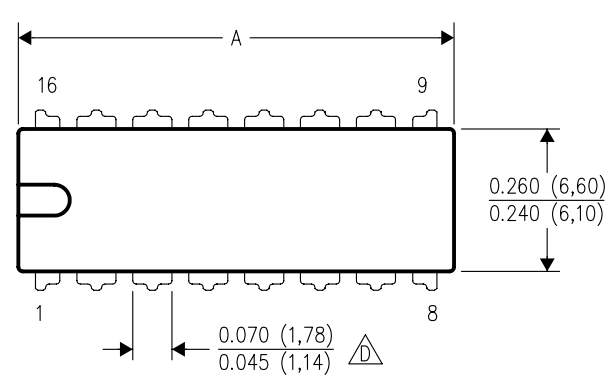


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

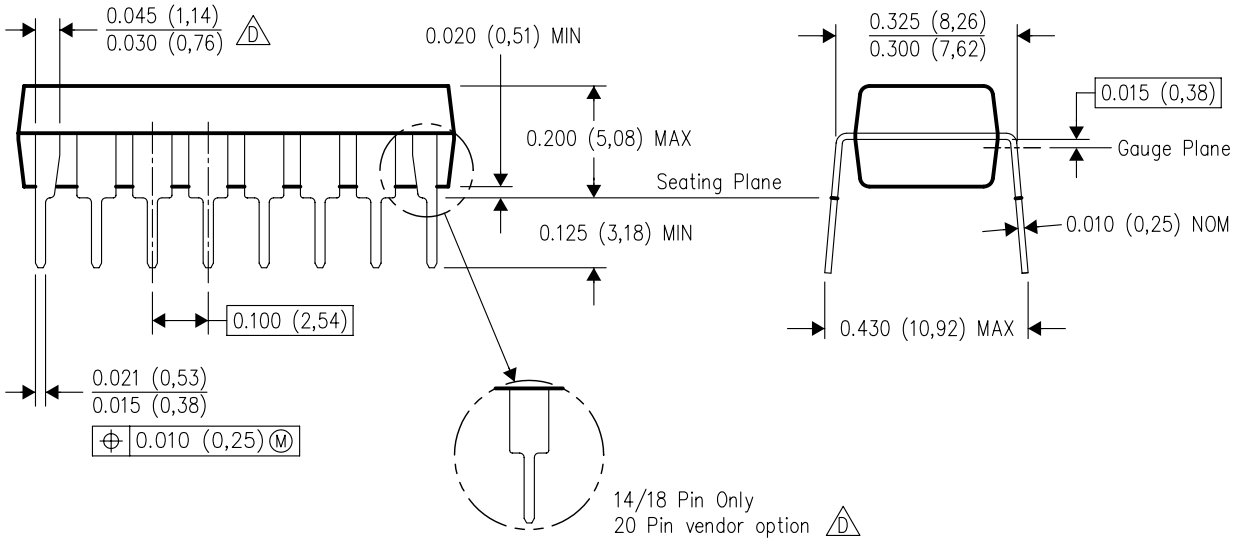
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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