

Document Title

64K x 32 Pipelined Sync. SRAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	September 13,2001	

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64K x 32 SYNCHRONOUS PIPELINE STATIC RAM

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Power-down control by ZZ input
- JEDEC 100-Pin LQFP and PQFP package
- Single +3.3V power supply
- Two Clock enables and one Clock disable to eliminate multiple bank bus contention
- Control pins mode upon power-up:
 - MODE in interleave burst mode
 - ZZ in normal operation mode
 These control pins can be connected to GNDQ or VCCQ to alter their power-up state
- Industrial temperature available

DESCRIPTION

The *ICSI* IC61S6432 is a high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, secondary cache for the Pentium™, 680X0™, and PowerPC™ microprocessors. It is organized as 65,536 words by 32 bits, fabricated with *ICSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. BW1 controls DQ1-DQ8, BW2 controls DQ9-DQ16, BW3 controls DQ17-DQ24, BW4 controls DQ25-DQ32, conditioned by BWE being LOW. A LOW on GW input would cause all bytes to be written.

Bursts can be initiated with either $\overline{\text{ADSP}}$ (Address Status Processor) or $\overline{\text{ADSC}}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally by the IC61S6432 and controlled by the ADV (burst address advance) input pin.

Asynchronous signals include output enable ($\overline{\text{OE}}$), sleep mode input (ZZ), clock (CLK) and burst mode input (MODE). A HIGH input on the ZZ pin puts the SRAM in the power-down state. When ZZ is pulled LOW (or no connect), the SRAM normally operates after three cycles of the wake-up period. A LOW input, i.e., GNDQ, on MODE pin selects LINEAR Burst. A VCCQ (or no connect) on MODE pin selects INTERLEAVED Burst.

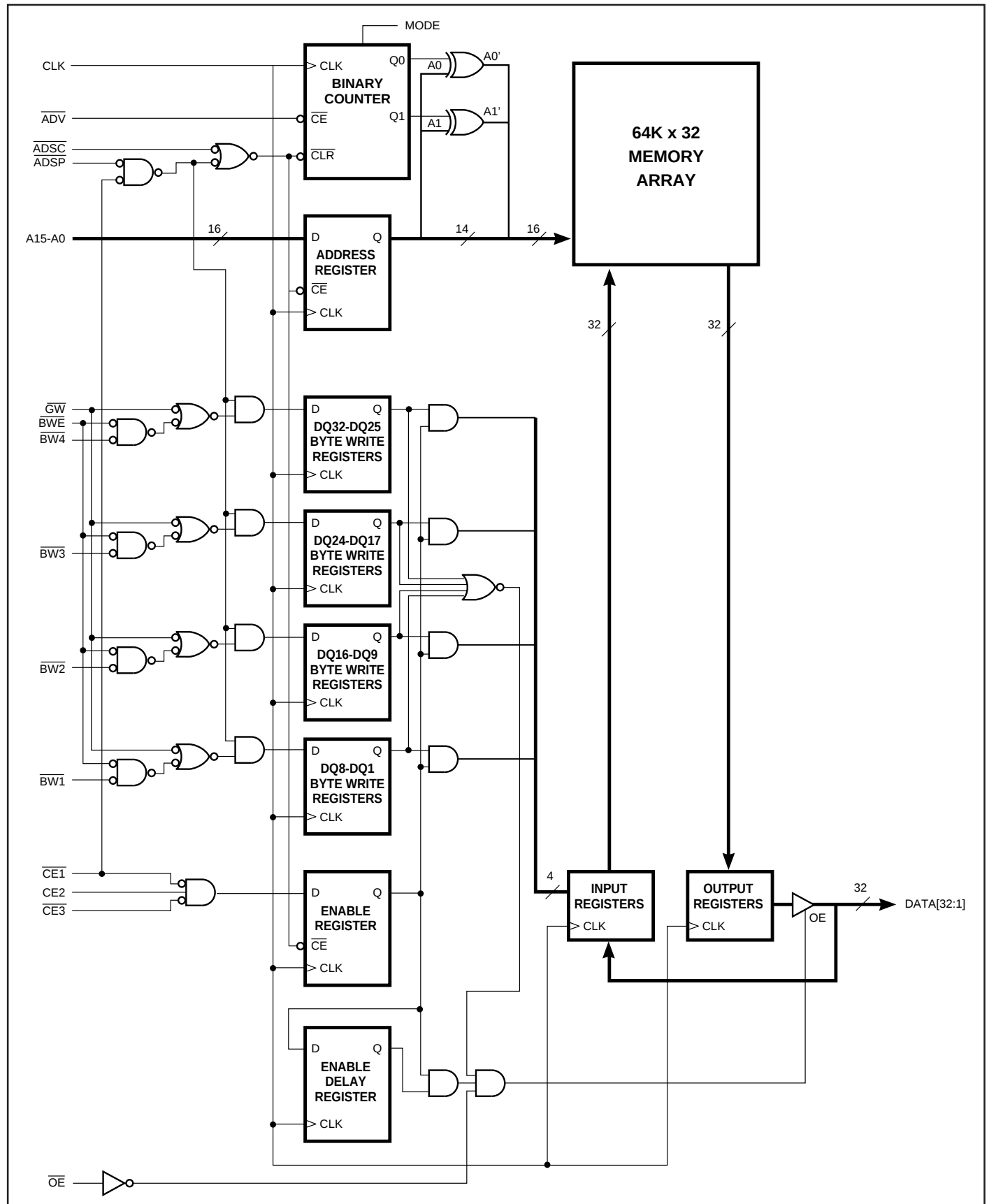
FAST ACCESS TIME

Symbol	Parameter	-200 ⁽¹⁾	-166	-133	-117	-5	-6	-7	-8	Unit
t _{KQ}	CLK Access Time	4	5	5	5	5	6	7	8	ns
t _{KC}	Cycle Time	5	6	7.5	8.5	10	12	13	15	ns
—	Frequency	200	166	133	117	100	83	75	66	MHz

Note:

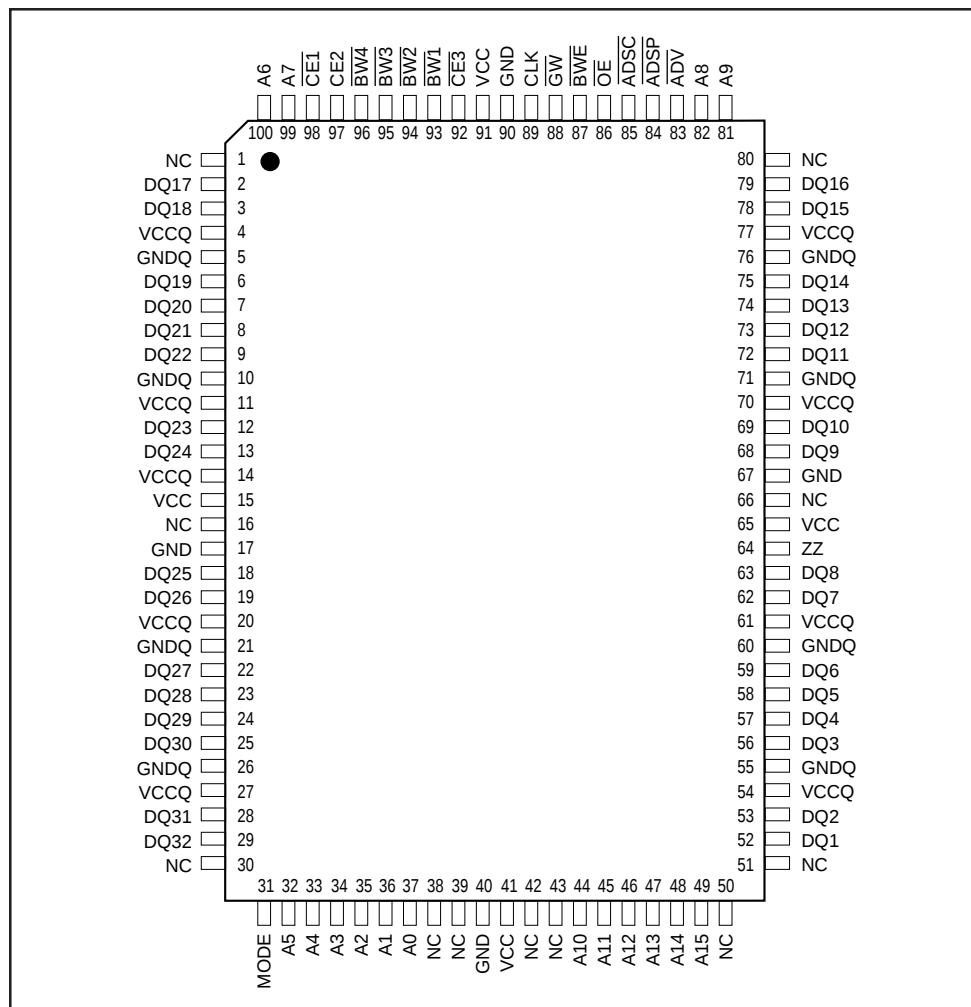
1. ADVANCE INFORMATION ONLY.

BLOCK DIAGRAM



PIN CONFIGURATION

100-Pin LQFP and PQFP (Top View)



PIN DESCRIPTIONS

A0-A15	Address Inputs
CLK	Clock
$\overline{\text{ADSP}}$	Processor Address Status
$\overline{\text{ADSC}}$	Controller Address Status
$\overline{\text{ADV}}$	Burst Address Advance
$\overline{\text{BW1-BW4}}$	Synchronous Byte Write Enable
$\overline{\text{BWE}}$	Byte Write Enable
$\overline{\text{GW}}$	Global Write Enable
$\overline{\text{CE1}}, \overline{\text{CE2}}, \overline{\text{CE3}}$	Synchronous Chip Enable

$\overline{\text{OE}}$	Output Enable
DQ1-DQ32	Data Input/Output
ZZ	Sleep Mode
MODE	Burst Sequence Mode
V _{CC}	+3.3V Power Supply
GND	Ground
V _{CCQ}	Isolated Output Buffer Supply: +3.3V
GND _Q	Isolated Output Buffer Ground
NC	No Connect

TRUTH TABLE

Operation	Address Used	$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	WRITE	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	H	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	L	Q
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	H	High-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	D
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	D

Notes:

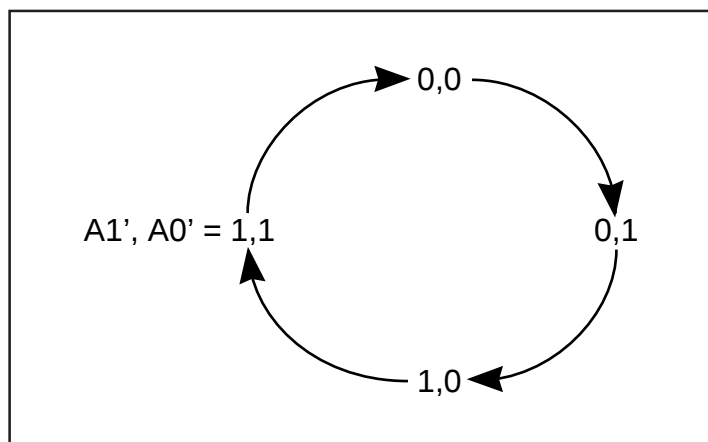
1. All inputs except $\overline{OE}$ must meet setup and hold times for the Low-to-High transition of clock (CLK).
2. Wait states are inserted by suspending burst.
3. "X" means don't care. WRITE=L means any one or more byte write enable signals ($\overline{BW1}$ - $\overline{BW4}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. WRITE=H means all byte write enable signals are HIGH.
4. For a Write operation following a Read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
5. $\overline{ADSP}$ LOW always initiates an internal READ at the Low-to-High edge of clock. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of clock.

PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	X	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE All Bytes	X	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CCQ} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)

ABSOLUTE MAXIMUM RATINGS^(1,2,3)

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	−10 to +85	°C
T _{STG}	Storage Temperature	−55 to +150	°C
P _D	Power Dissipation	1.8	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	−0.5 to V _{CCQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	−0.5 to 5.5	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V +10%, −5%
Industrial	−40°C to +85°C	3.3V +10%, −5%

DC ELECTRICAL CHARACTERISTICS^(1,2) (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -5.0 mA		2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 5.0 mA		—	0.4	V
V _{IH}	Input HIGH Voltage			2.0	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage			-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CCQ} ⁽²⁾	Com. Ind.	-5 -10	5 10	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CCQ} , $\overline{OE} = V_{IH}$	Com. Ind.	-5 -10	5 10	μA

Notes:

1. MODE pin have an internal pull-up. ZZ pin has an internal pull-down. These pins may be a No Connect, tied to GND, or tied to V_{CCQ}.
2. MODE pin should be tied to V_{CC} or GND. They exhibit ±30 μA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{CC} - 0.2V.

POWER SUPPLY CHARACTERISTICS (Operating Range)

Symbol	Parameter	Test Conditions		-200 ⁽¹⁾		-166		-133		-117		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs = V _{IL} or V _{IH} OE = V _{IH} , Cycle Time ≥ t _{CC} min.	Com. Ind.	— —	400 —	— —	215 —	— —	205 —	— —	195 205	mA
I _{SB}	Standby Current	Device Deselected, V _{CC} = Max., CLK Cycle Time ≥ t _{CC} min.	Com. Ind.	— —	100 —	— —	70 —	— —	60 —	— —	50 60	mA
I _{ZZ}	Power-Down Mode Current	ZZ = V _{CCQ} , CLK Running All Inputs ≤ GND + 0.2V or ≥ V _{CC} - 0.2V	Com. Ind.	— —	5 —	— —	5 —	— —	5 —	— —	5 10	mA

Note:

1. ADVANCE INFORMATION ONLY.

Symbol	Parameter	Test Conditions		-5		-6		-7		-8		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs = V _{IL} or V _{IH} OE = V _{IH} , Cycle Time ≥ t _{CC} min.	Com. Ind.	— —	175 185	— —	165 175	— —	150 160	— —	140 150	mA
I _{SB}	Standby Current	Device Deselected, V _{CC} = Max., CLK Cycle Time ≥ t _{CC} min.	Com. Ind.	— —	25 35	— —	25 35	— —	25 35	— —	25 35	mA
I _{ZZ}	Power-Down Mode Current	ZZ = V _{CCQ} , CLK Running All Inputs ≤ GND + 0.2V or ≥ V _{CC} - 0.2V	Com. Ind.	— —	5 10	— —	5 10	— —	5 10	— —	5 10	mA

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

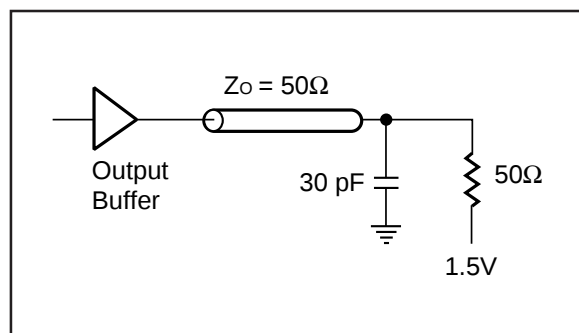


Figure 1

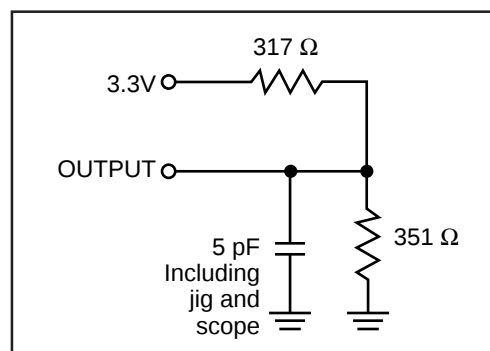


Figure 2

READ CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-200 ⁽¹⁾		-166		-133		-117		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CC}	Cycle Time	5	—	6	—	7.5	—	8.5	—	ns
t _{KH}	Clock High Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{KL}	Clock Low Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{KQ}	Clock Access Time	—	4	—	5	—	5	—	5	ns
t _{KQX} ⁽²⁾	Clock High to Output Invalid	1	—	1.5	—	1.5	—	1.5	—	ns
t _{KQLZ} ^(2,3)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{KQHZ} ^(2,3)	Clock High to Output High-Z	1	3.5	1.5	5	1.5	5	1.5	6	ns
t _{OEQ}	Output Enable to Output Valid	—	3.5	—	5	—	5	—	5	ns
t _{OEQX} ⁽²⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
t _{OELZ} ^(2,3)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{OEHZ} ^(2,3)	Output Disable to Output High-Z	—	3	—	3	—	3	—	4	ns
t _{AS}	Address Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{WS}	Write Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{AVS}	Address Advance Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CFG} ⁽⁴⁾	Configuration Setup	25	—	25	—	30	—	35	—	ns

Notes:

1. **ADVANCE INFORMATION ONLY.**

2. Guaranteed but not 100% tested. This parameter is periodically sampled.

3. Tested with load in Figure 2.

4. Configuration signal MODE is static and must not change during normal operation.

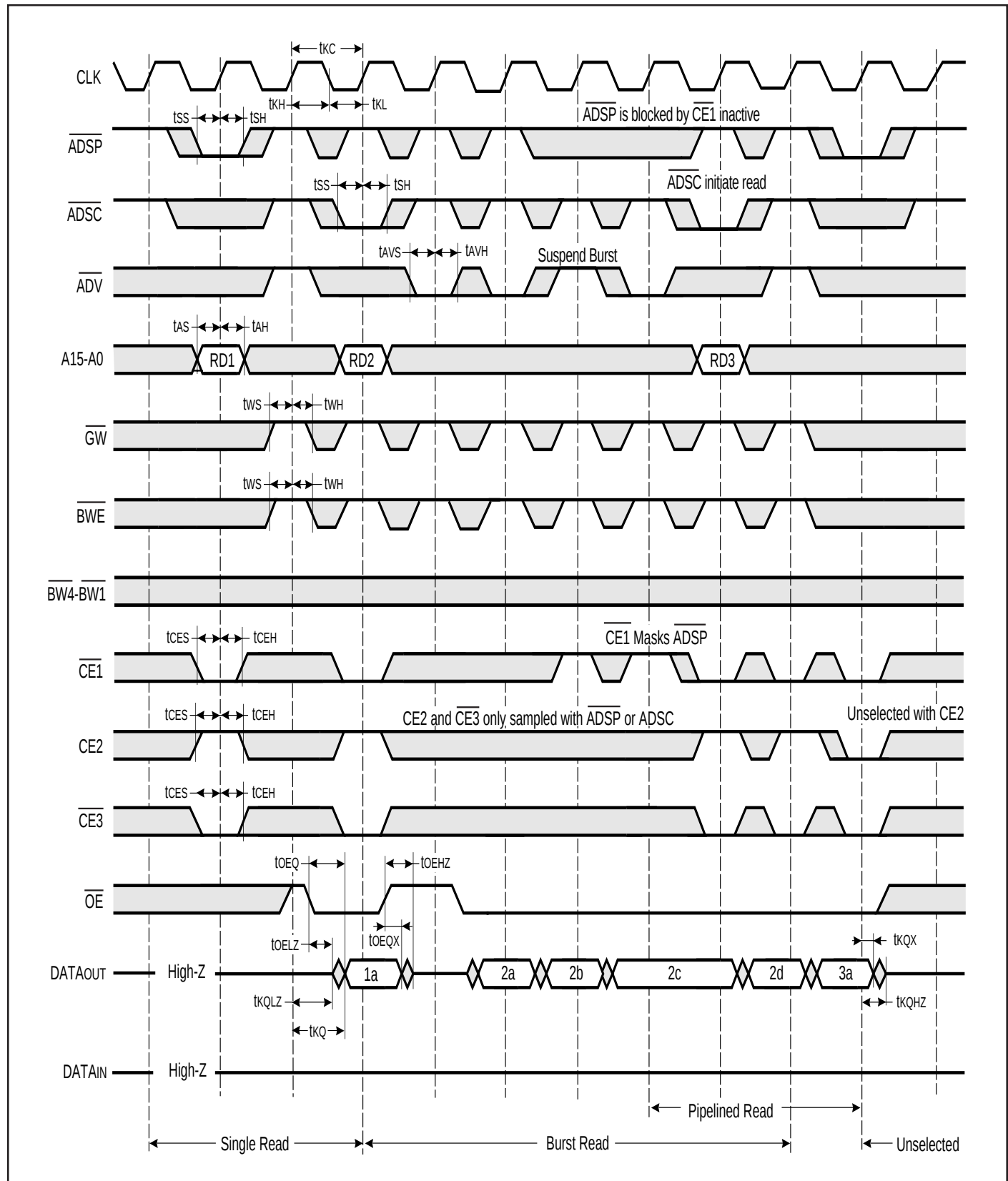
READ CYCLE SWITCHING CHARACTERISTICS (Over Operating Range) *(Continued)*

Symbol	Parameter	-5		-6		-7		-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{KC}	Cycle Time	10	—	12	—	13	—	15	—	ns
t _{KH}	Clock High Time	3.5	—	4	—	6	—	6	—	ns
t _{KL}	Clock Low Time	3.5	—	4	—	6	—	6	—	ns
t _{KQ}	Clock Access Time	—	5	—	6	—	7	—	8	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	1.5	—	1.5	—	2	—	2	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	1.5	6	1.5	6	2	6	2	6	ns
t _{OEQ}	Output Enable to Output Valid	—	5	—	6	—	6	—	6	ns
t _{OEQX} ⁽¹⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{OEHZ} ^(1,2)	Output Disable to Output High-Z	—	4	—	5	—	6	—	6	ns
t _{AS}	Address Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{WS}	Write Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{AVS}	Address Advance Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CFG} ⁽³⁾	Configuration Setup	35	—	45	—	66.7	—	80	—	ns

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Configuration signal MODE is static and must not change during normal operation.

READ CYCLE TIMING: PIPELINE



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-200 ⁽¹⁾		-166		-133		-117		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CC}	Cycle Time	5	—	6	—	7.5	—	8.5	—	ns
t _{KH}	Clock High Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{KL}	Clock Low Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{AS}	Address Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{WS}	Write Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{DS}	Data In Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{AVS}	Address Advance Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{DH}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CFG} ⁽²⁾	Configuration Setup	25	—	25	—	30	—	35	—	ns

Symbol	Parameter	-5		-6		-7		-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CC}	Cycle Time	10	—	12	—	13	—	15	—	ns
t _{KH}	Clock High Time	3.5	—	4	—	6	—	6	—	ns
t _{KL}	Clock Low Time	3.5	—	4	—	6	—	6	—	ns
t _{AS}	Address Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{WS}	Write Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{DS}	Data In Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{AVS}	Address Advance Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{DH}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CFG} ⁽²⁾	Configuration Setup	35	—	45	—	52	—	60	—	ns

Note:

1. ADVANCE INFORMATION ONLY.

2. Configuration signal MODE is static and must not change during normal operation.

The diagram illustrates the timing relationships for the ADSP and ADSC signals. Key timing parameters and signal states are shown:

- CLK**: Clock signal with period t_{KC} .
- ADSP**: Address Strobe for Program memory. Timing parameters include t_{SS} , t_{SH} , t_{KH} , and t_{KL} . A note indicates "ADSP is blocked by $\overline{CE1}$ inactive".
- ADSC**: Address Strobe for Data memory. A note indicates "ADSC initiate Write".
- ADV**: Address Valid signal. Timing parameters include t_{AVS} and t_{AVH} . A note indicates "ADV must be inactive for ADSP Write".
- A15-A0**: Address bus. Shows write cycles $WR1$, $WR2$, and $WR3$. Timing parameters include t_{AS} and t_{AH} .
- GW**: Global Write Enable signal. Timing parameters include t_{WS} and t_{WH} .
- BWE**: Bank Write Enable signal. Timing parameters include t_{WS} and t_{WH} .
- BW4-BW1**: Bank Write Enable signals. Timing parameters include t_{WS} and t_{WH} .
- CE1**: Chip Enable 1. Timing parameters include t_{CES} and t_{CEH} . A note indicates "CE1 Masks ADSP".
- CE2**: Chip Enable 2. Timing parameters include t_{CES} and t_{CEH} . A note indicates "CE2 and CE3 only sampled with ADSP or ADSC".
- CE3**: Chip Enable 3. Timing parameters include t_{CES} and t_{CEH} . A note indicates "Unselected with CE2".
- OE**: Output Enable signal.
- DATAOUT**: Data output bus. Shows High-Z state.
- DATAIN**: Data input bus. Shows High-Z state and data cycles 1a, 2a, 2b, 2c, 2d, 3a. Timing parameters include t_{DS} and t_{DH} . A note indicates "BW4-BW1 only are applied to first cycle of WR2".

The diagram is divided into four main sections: Single Write, Burst Write, Write, and Unselected.

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-200 ⁽¹⁾		-166		-133		-117		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{kc}	Cycle Time	5	—	6	—	7.5	—	8.5	—	ns
t _{kH}	Clock High Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{kL}	Clock Low Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{kQ}	Clock Access Time	—	4	—	5	—	5	—	5	ns
t _{kQX} ⁽²⁾	Clock High to Output Invalid	1	—	1.5	—	1.5	—	1.5	—	ns
t _{kQLZ} ^(2,3)	Clock High to Output Low-Z	—	—	0	—	0	—	0	—	ns
t _{kQHZ} ^(2,3)	Clock High to Output High-Z	1	3.5	1.5	5	1.5	5	1.5	6	ns
t _{oEQ}	Output Enable to Output Valid	—	3.5	—	5	—	5	—	5	ns
t _{oEQX} ⁽²⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
t _{oELZ} ^(2,3)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{oEHZ} ^(2,3)	Output Disable to Output High-Z	—	3	—	3	—	3	—	4	ns
t _{AS}	Address Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{WS}	Write Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CFG} ⁽⁴⁾	Configuration Setup	25	—	25	—	30	—	35	—	ns

Notes:1. **ADVANCE INFORMATION ONLY.**

2. Guaranteed but not 100% tested. This parameter is periodically sampled.

3. Tested with load in Figure 2.

4. Configuration signal MODE is static and must not change during normal operation.

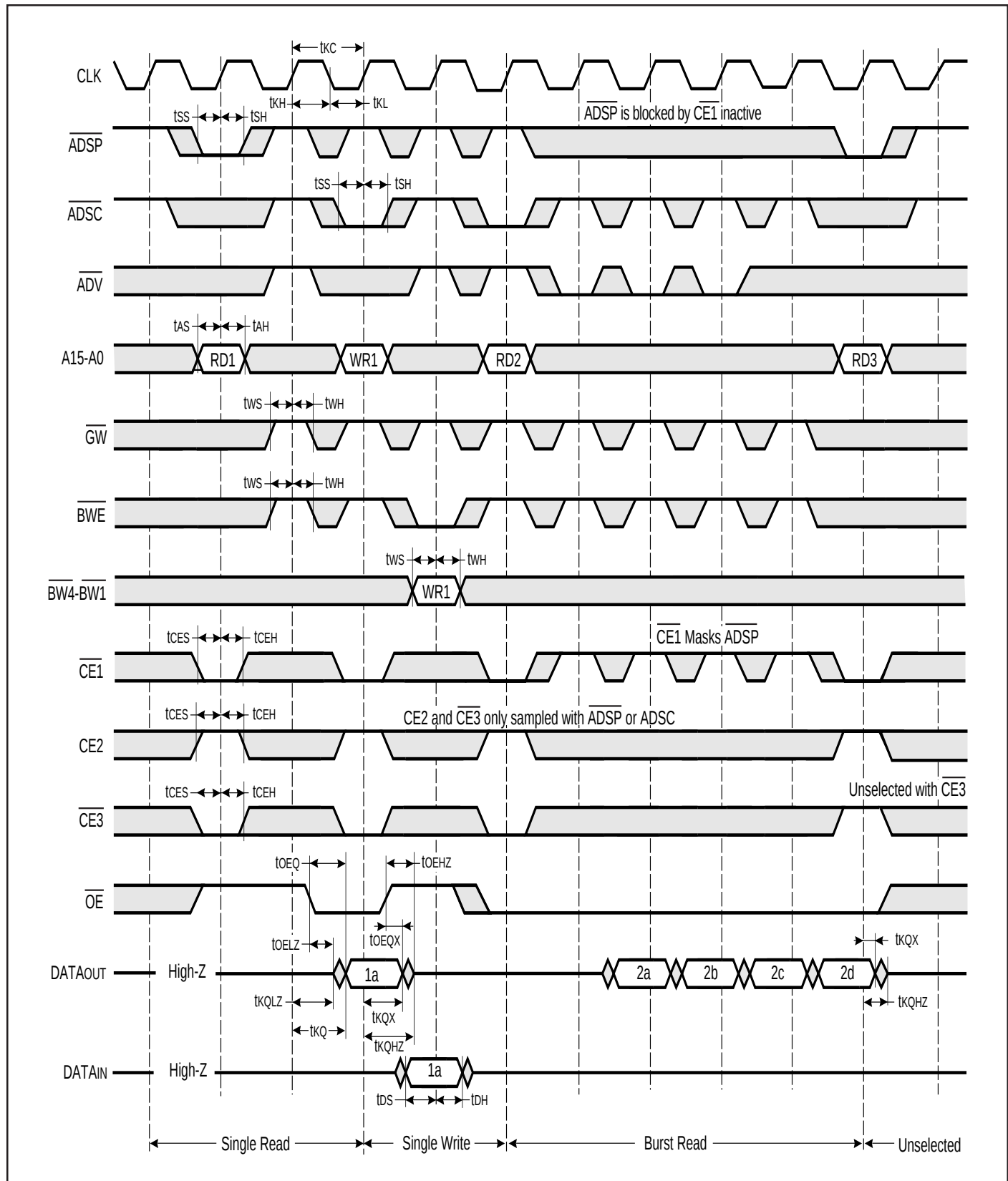
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range) (Continued)

Symbol	Parameter	-5		-6		-7		-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{KC}	Cycle Time	10	—	12	—	13	—	15	—	ns
t _{KH}	Clock High Time	3.5	—	4	—	6	—	6	—	ns
t _{KL}	Clock Low Time	3.5	—	4	—	6	—	6	—	ns
t _{KQ}	Clock Access Time	—	5	—	6	—	7	—	8	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	1.5	—	1.5	—	2	—	2	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	1.5	6	1.5	6	2	6	2	6	ns
t _{OEQ}	Output Enable to Output Valid	—	5	—	6	—	6	—	6	ns
t _{OEQX} ⁽¹⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{OEHZ} ^(1,2)	Output Disable to Output High-Z	—	4	—	5	—	6	—	6	ns
t _{AS}	Address Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{WS}	Write Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{CFG} ⁽³⁾	Configuration Setup	35	—	45	—	52	—	60	—	ns

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Configuration signal MODE is static and must not change during normal operation.

READ/WRITE CYCLE TIMING: PIPELINE



SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-200 ⁽²⁾		-166		-133		-117		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{KC}	Cycle Time	5	—	6	—	7.5	—	8.5	—	ns
t _{KH}	Clock High Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{KL}	Clock Low Time	1.6	—	2.4	—	2.8	—	3	—	ns
t _{KQ}	Clock Access Time	—	4	—	5	—	5	—	5	ns
t _{KQX} ⁽³⁾	Clock High to Output Invalid	1	—	1.5	—	1.5	—	1.5	—	ns
t _{KQLZ} ^(3,4)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{KQHZ} ^(3,4)	Clock High to Output High-Z	1	3.5	1.5	5	1.5	5	1.5	6	ns
t _{OEQ}	Output Enable to Output Valid	—	3.5	—	5	—	5	—	5	ns
t _{OEQX} ⁽³⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
t _{OELZ} ^(3,4)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{OEHZ} ^(3,4)	Output Disable to Output High-Z	—	3	—	3	—	3	—	4	ns
t _{AS}	Address Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{SH}	Address Status Hold Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{CEH}	Chip Enable Hold Time	2	—	2.5	—	2.5	—	2.5	—	ns
t _{ZZS} ⁽⁵⁾	ZZ Standby	—	8	2	—	2	—	2	—	cyc
t _{ZZREC} ⁽⁶⁾	ZZ Recovery	8	—	2	—	2	—	2	—	cyc

Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. **ADVANCE INFORMATION ONLY.**
3. Guaranteed but not 100% tested. This parameter is periodically sampled.
4. Tested with load in Figure 2.
5. The assertion of ZZ allows the SRAM to enter a lower power state than when deselected within the time specified. Data retention is guaranteed when ZZ is asserted and clock remains active.
6. ADSC and ADSP must not be asserted for at least two cycles after leaving ZZ state.

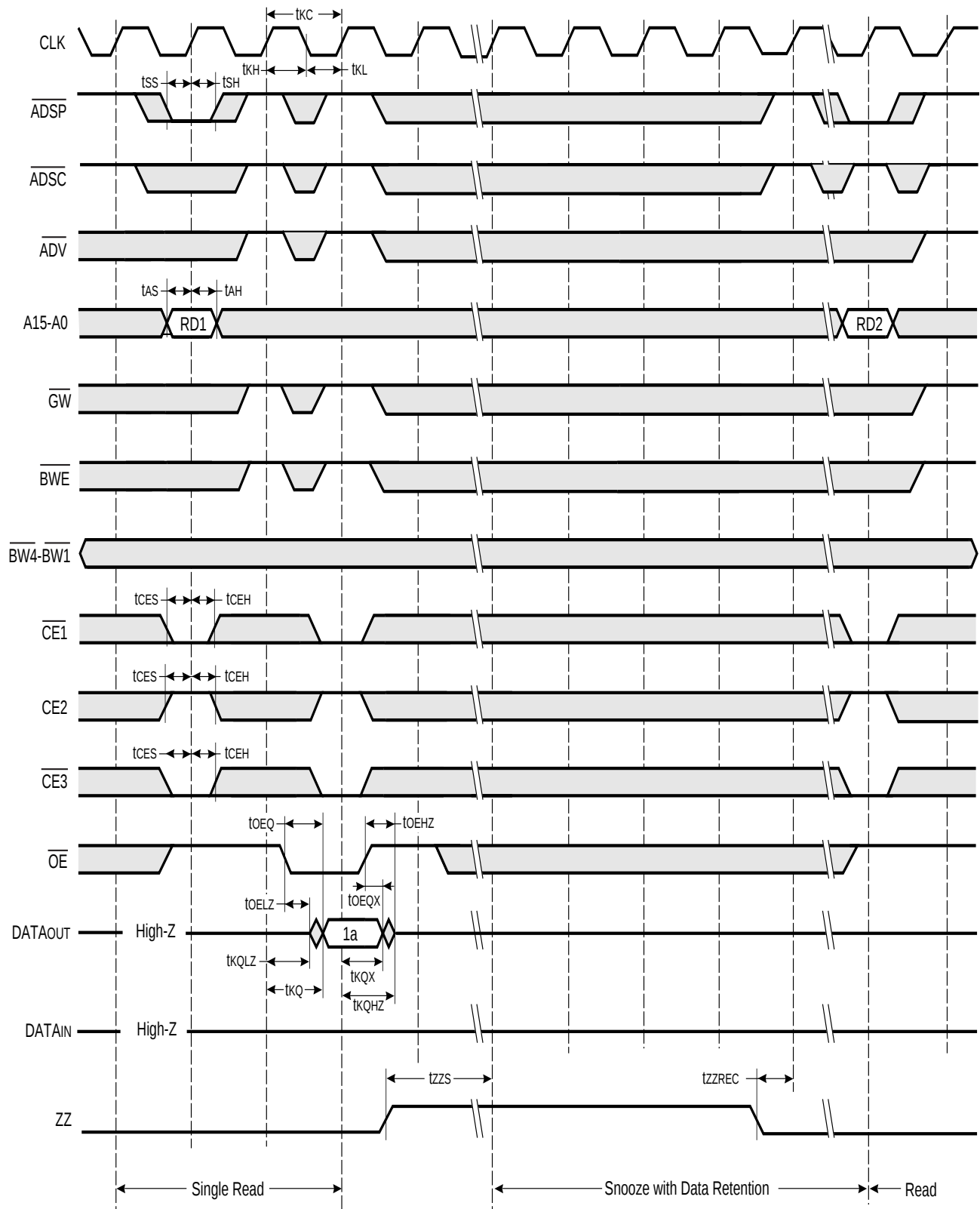
SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range) *(Continued)*

Symbol	Parameter	-5		-6		-7		-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{KC}	Cycle Time	10	—	12	—	13	—	15	—	ns
t _{KH}	Clock High Time	3.5	—	4	—	6	—	6	—	ns
t _{KL}	Clock Low Time	3.5	—	4	—	6	—	6	—	ns
t _{KQ}	Clock Access Time	—	5	—	6	—	7	—	8	ns
t _{KQX} ⁽²⁾	Clock High to Output Invalid	1.5	—	1.5	—	2	—	2	—	ns
t _{KQLZ} ^(2,3)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{KQHZ} ^(2,3)	Clock High to Output High-Z	1.5	6	1.5	6	2	6	2	6	ns
t _{OEQ}	Output Enable to Output Valid	—	5	—	6	—	6	—	6	ns
t _{OEQX} ⁽²⁾	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	ns
t _{OELZ} ^(2,3)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t _{OEHZ} ^(2,3)	Output Disable to Output High-Z	—	4	—	5	—	6	—	6	ns
t _{AS}	Address Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{SS}	Address Status Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{CES}	Chip Enable Setup Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{AH}	Address Hold Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{SH}	Address Status Hold Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{CEH}	Chip Enable Hold Time	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _{ZZS} ⁽⁴⁾	ZZ Standby	2	—	2	—	2	—	2	—	cyc
t _{ZZREC} ⁽⁵⁾	ZZ Recovery	2	—	2	—	2	—	2	—	cyc

Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.
4. The assertion of ZZ allows the SRAM to enter a lower power state than when deselected within the time specified. Data retention is guaranteed when ZZ is asserted and clock remains active.
5. ADSC and ADSP must not be asserted for at least two cycles after leaving ZZ state.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

Frequency (MHz)	Order Part Number	Package
200	IC61S6432-200TQ	14*20*1.4mm LQFP
	IC61S6432-200PQ	14*20*2.7mm PQFP
166	IC61S6432-166TQ	14*20*1.4mm LQFP
	IC61S6432-166PQ	14*20*2.7mm PQFP
133	IC61S6432-133TQ	14*20*1.4mm LQFP
	IC61S6432-133PQ	14*20*2.7mm PQFP
117	IC61S6432-117TQ	14*20*1.4mm LQFP
	IC61S6432-117PQ	14*20*2.7mm PQFP
100	IC61S6432-5TQ	14*20*1.4mm LQFP
	IC61S6432-5PQ	14*20*2.7mm PQFP
83	IC61S6432-6TQ	14*20*1.4mm LQFP
	IC61S6432-6PQ	14*20*2.7mm PQFP
75	IC61S6432-7TQ	14*20*1.4mm LQFP
	IC61S6432-7PQ	14*20*2.7mm PQFP
66	IC61S6432-8TQ	14*20*1.4mm LQFP
	IC61S6432-8PQ	14*20*2.7mm PQFP

ORDERING INFORMATION**Industrial Range: -40°C to +85°C**

Frequency (MHz)	Order Part Number	Package
117	IC61S6432-117TQI	14*20*1.4mm LQFP
	IC61S6432-117PQI	14*20*2.7mm PQFP
100	IC61S6432-5TQI	14*20*1.4mm LQFP
	IC61S6432-5PQI	14*20*2.7mm PQFP
83	IC61S6432-6TQI	14*20*1.4mm LQFP
	IC61S6432-6PQI	14*20*2.7mm PQFP
75	IC61S6432-7TQI	14*20*1.4mm LQFP
	IC61S6432-7PQI	14*20*2.7mm PQFP
66	IC61S6432-8TQI	14*20*1.4mm LQFP
	IC61S6432-8PQI	14*20*2.7mm PQFP



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