SN8P021X/8P011X 8-bit microcontroller

1. GENERAL DESCRIPTION

The SN8P021X/8P011X is an 8-bit micro-controller utilized with CMOS technology fabrication and featured with low power consumption and high performance by its unique electronic structure. This chip is designed with the excellent IC structure, including the program memory up to 2K/1K-word OTP ROM, 64 bytes of the data memory, one 8-bit T0 basic timer, one 8-bit timer/event counter, a watch dog timer, three interrupt sources (T0, TC0, INT0), 13 I/O pins and 8 levels stack buffer. Besides, the user can choose desired oscillator configurations for the controller. There are three oscillator configurations to select for generating system clock, including high-performing crystal, ceramic resonator or cost-saving RC.

2. FEATURES

- ***Memory configuration***
  OTP ROM size : 2048 * 16 bits for SN8P021X series
  OTP ROM size : 1024 * 16 bits for SN8P011X series
  RAM size : 64 * 8 bits.

- ***I/O pin configuration*** *(Total 13 pins)*
  One input port : 1 pin with wakeup function.
  Two Input/output ports : 12 pins.

- ***56 powerful instructions***
  All of instructions are 1 word with 1 or 2 cycles' execution.
  Execution time : 1 cycle uses 4 clocks of oscillator.
  All ROM area **JMP** instruction.
  All ROM area Subroutine **CALL** instruction.
  All ROM area lookup table function. (**MOVC** instruction)

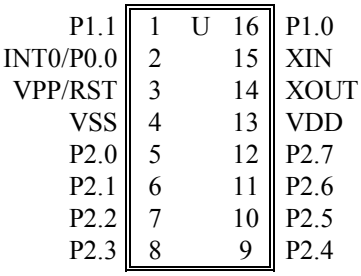
- ***Three interrupt sources :***
  Two internal interrupts : T0, TC0
  One external interrupt : INT0

- ***Eight levels stack buffer***
- An 8-bit basic timer.
- An 8-bit timer/event counter.
- A watchdog timer.

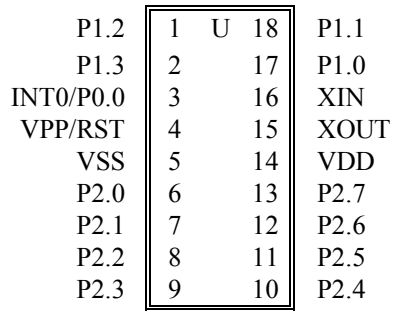
- Acceptable oscillator type :
  Crystal or ceramic resonator up to 8MHz
  RC oscillator up to 2 MHz

- ***Package :***
  PDIP : 16, 18, 20
  SOP : 16, 18, 20

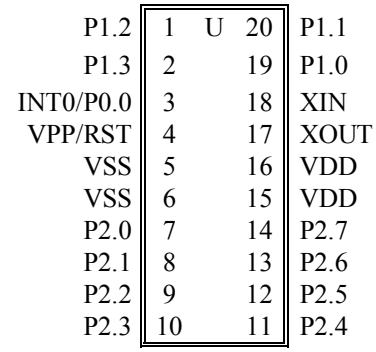
3. PIN ASSIGNMENT



SN8P0211P
SN8P0211S
SN8P0111P
SN8P0111S

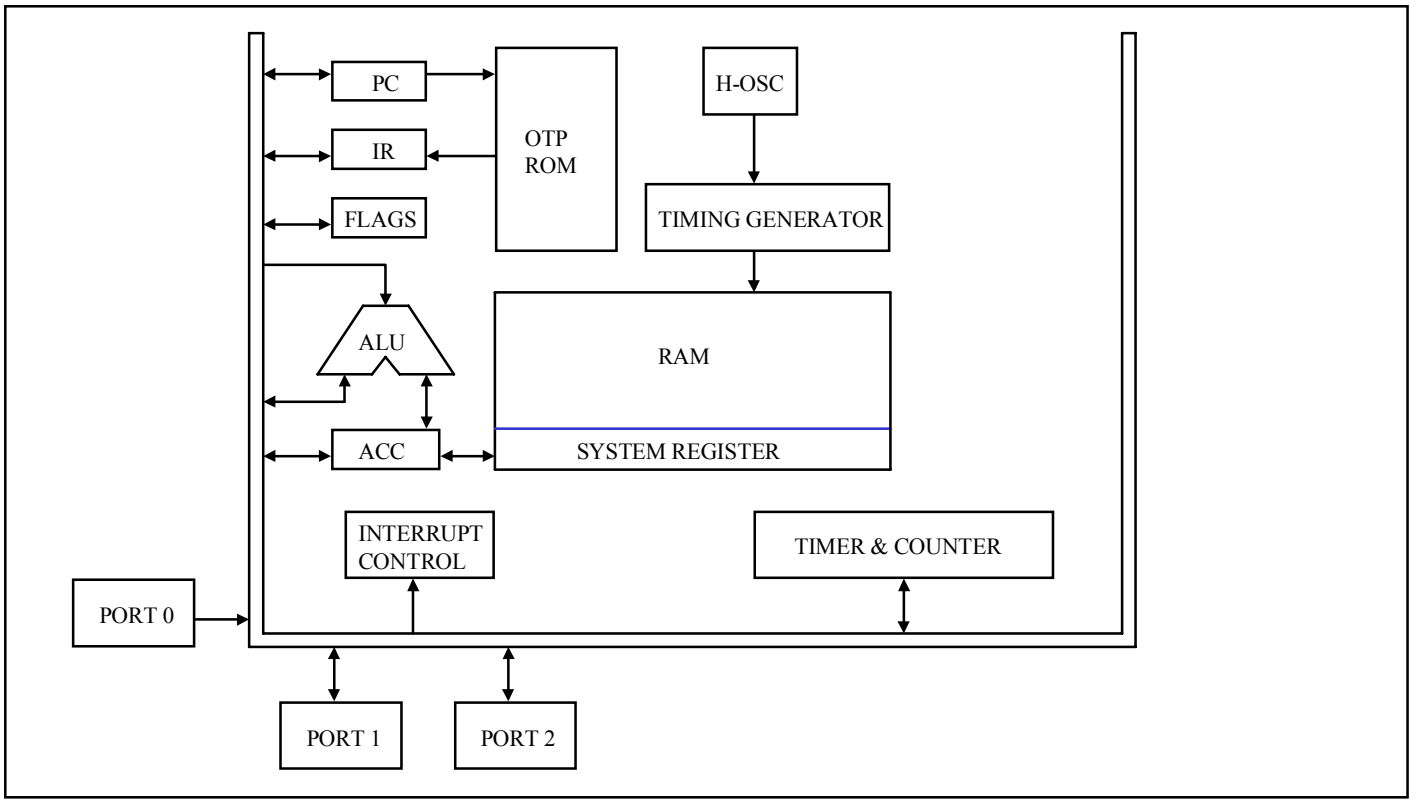


SN8P0212P
SN8P0212S
SN8P0112P
SN8P0112S



SN8P0213P
SN8P0213S
SN8P0113P
SN8P0113S

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

PIN NAME	TYPE	DESCRIPTION
P1.0 ~ P1.3	I/O	Port 1.0 ~ Port 1.3 bi-direction pins.
RST/VPP	I	System reset inputs pin. Schmitt trigger structure, active "low", normal stay to "high". During program op-code, this pin be pull to 12.5Vdc to reset internal address counter and to write data into OTP-ROM.
VDD, VSS	P	Power supply input pins.
P2.0 ~ P2.7	I/O	Port 2.0 ~ Port 2.7 bi-direction pins.
XIN	I	Oscillator input pin.
XOUT	O	Oscillator output pin.
P0.0 / INT0	I	Port 0.0 and INT0 trigger pin with schmitt trigger structure.

Note : In order to reduce power consumption, the following procedure must be setup.
a). In the SN8P0211/8P0111 version, P1.2 ~ P1.3 must be programmed to input mode with pull up resistor.

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