TQFP, BGA
Commercial Temp
Industrial Temp

256K x 18 Sync Cache Tag

180 MHz–100 MHz
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- 3.3 V +10%/–5% core power supply, 2.5 V or 3.3 V I/O supply
- Dual Cycle Deselect (DCD)
- Intergrated data comparator for Tag RAM application
- $\overline{FT}$ mode pin for flow through or pipeline operation
- $\overline{LBO}$ pin for Linear or Interleave (Pentium™ and X86) Burst mode
- Synchronous address, data I/O, and control inputs
- Synchronous Data Enable ($\overline{DE}$)
- Asynchronous Output Enable ($\overline{OE}$)
- Asynchronous Match Output Enable ($\overline{MOE}$)
- Byte Write ($\overline{BWE}$) and Global Write ($\overline{GW}$) operation
- Three chip enable signals for easy depth expansion
- Internal self-timed write cycle
- JTAG Test mode conforms to IEEE standard 1149.1
- JEDEC-standard 100-lead TQFP package and 119-BGA
- Pb-Free 100-lead TQFP package available

Functional Description

The GS841E18A is a 256K x 18 high performance synchronous DCD SRAM with integrated Tag RAM comparator. A 2-bit burst counter is included to provide burst interface with Pentium™ and other high performance CPUs. It is designed to be used as a Cache Tag SRAM, as well as data SRAM. Addresses, data IOs, match output, chip enables ($\overline{CE1}$, CE2, $\overline{CE3}$), address control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BWE}$, $\overline{GW}$, $\overline{DE}$) are synchronous and are controlled by a positive-edge-triggered clock (CLK).

Output Enable ($\overline{OE}$), Match Output Enable, and power down control (ZZ) are asynchronous. Burst can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. Subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst sequence is either interleave order (Pentium™ or x86) or linear order, and is controlled by $\overline{LBO}$.

Output registers and the Match output register are provided and controlled by the $\overline{FT}$ mode pin (Pin 14). Through use of the $\overline{FT}$ mode pin, I/O registers can be programmed to perform pipeline or flow through operation. Flow Through mode reduces latency.

Byte write operation is performed by using Byte Write Enable ($\overline{BWE}$) input combined with two individual byte write signals $\overline{BW}$1-2. In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time.

Compare cycles begin as a read cycle with output disabled so that compare data can be loaded into the data input register. The comparator compares the read data with the registered input data and a match signal is generated. The match output can be either in Pipeline or Flow Through modes controlled by the $\overline{FT}$ signal.

Low power (Standby mode) is attained through the assertion of the ZZ signal, or by stopping the clock (CLK). Memory data is retained during Standby mode.

JTAG boundary scan interface is provided using IEEE standard 1149.1 protocol. Four pins—Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS)—are used to perform JTAG function.

The GS841E18A operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- or 2.5 V-LVTTL-compatible. Separate output (V_{DDQ}) pins are used to allow both 3.3 V or 2.5 V IO interface.

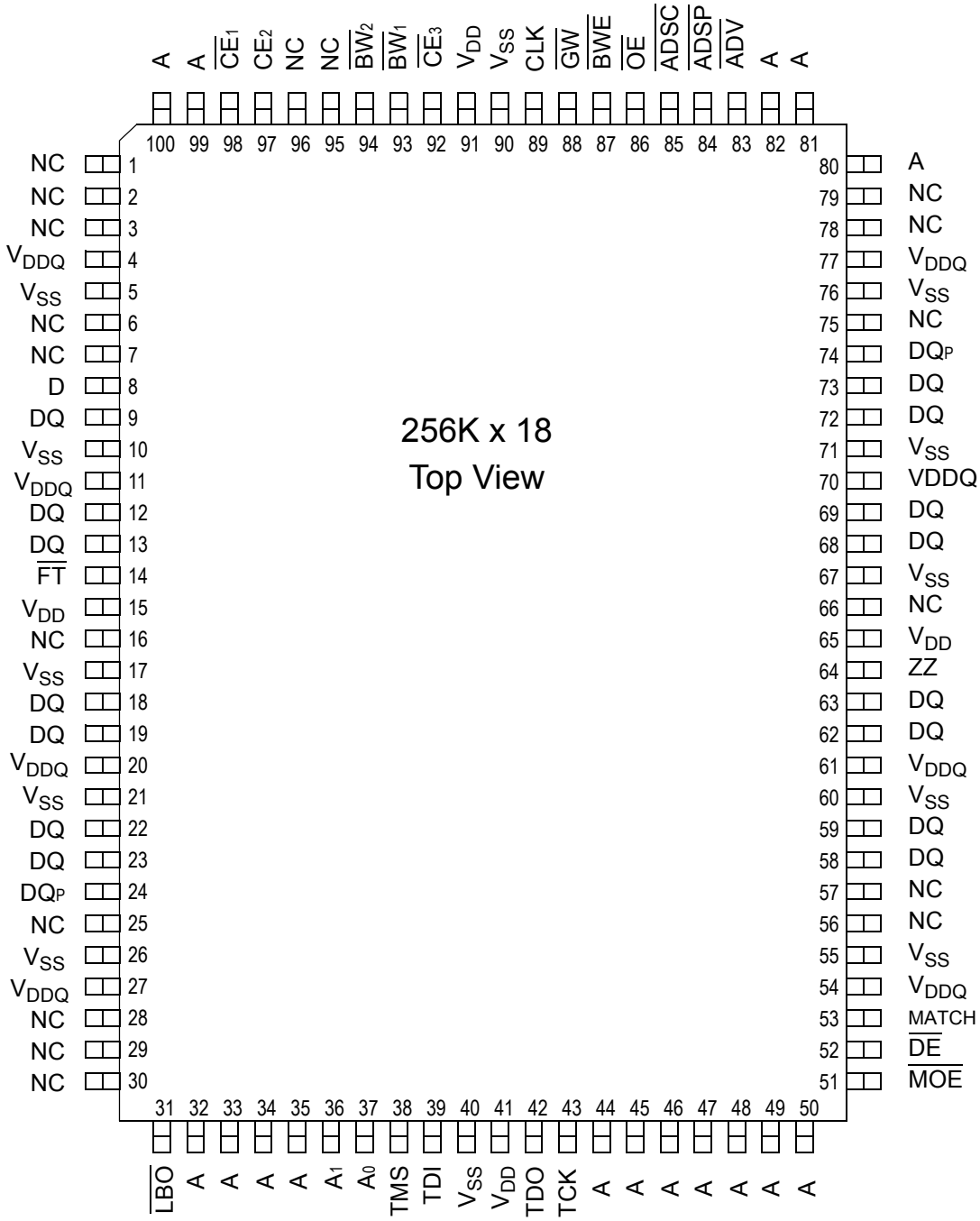
Dual Cycle Deselect (DCD)

The GS841E18A is a DCD pipelines synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. DCD SRAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of the clock.

Parameter Synopsis

		–180	-166	-150	-133	-100
Pipeline 3-1-1-1	t_{cycle}	5.5 ns	6.0 ns	6.6 ns	7.5 ns	10 ns
	t_{KQ}	3.2 ns	3.5 ns	3.8 ns	4.0 ns	4.5 ns
	I_{DD}	335 mA	310 mA	275 mA	250 mA	190 mA
Flow Through 2-1-1-1	t_{KQ}	8 ns	8.5 ns	10 ns	11 ns	12 ns
	t_{cycle}	9.1 ns	10 ns	10 ns	15 ns	15 ns
	I_{DD}	210 mA	190 mA	190 mA	140 mA	140 mA

Pin Configuration (Package T)



GS841E18A PadOut—119-Bump BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	E_2	A	$\overline{ADSC}$	A	$\overline{E}_3$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQ_P	NC
E	NC	DQ_B	V_{SS}	$\overline{E}_1$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{B}_B$	$\overline{ADV}$	NC	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CK	V_{SS}	NC	DQ_A
L	DQ_B	NC	NC	NC	$\overline{B}_A$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BW}$	V_{SS}	MATCH	V_{DDQ}
N	DQ_B	NC	V_{SS}	A_1	V_{SS}	DQ_A	$\overline{DE}$
P	NC	DQ_P	V_{SS}	A_0	V_{SS}	$\overline{MOE}$	DQ_A
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

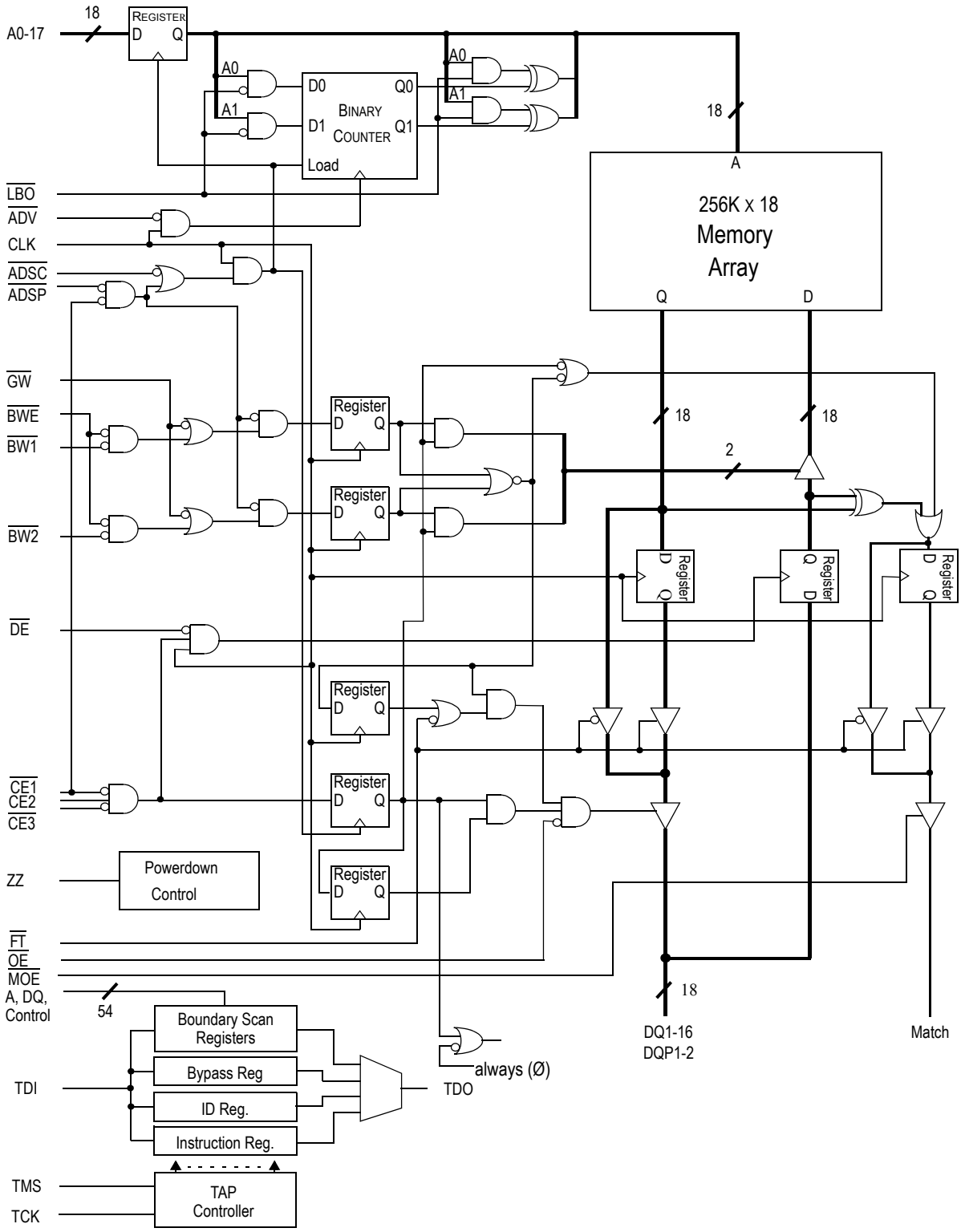
TQFP Pin Description

Symbol	Description
An	Address Input Signals—Inputs are registered and must meet setup and hold times, as specified on **page 11**.
CLK	Clock Input Signal
$\overline{BWE}$	Byte Write Enable Signal—The byte write enable signal needs to be combined with one of the four byte write signals for a write operation to occur.
$\overline{BW1}$	Byte Write signal for data outputs 1 thru 8
$\overline{BW2}$	Byte Write signal for data outputs 9 thru 16
$\overline{GW}$	Global Write Enable
$\overline{CE1}$,CE2, $\overline{CE3}$	Chip Enables
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst address advance
$\overline{ADSP}$, $\overline{ADSC}$	Address status signals
DQ	Data Input and Output pins
DQP	Parity Input and Output pins
MATCH	Match Output
$\overline{MOE}$	Match Output Enable
$\overline{DE}$	Data Enable—Data input registers are updated only when $\overline{DE}$ is active.
ZZ	Power down control—Application of ZZ will result in a low standby power consumption.
$\overline{FT}$	Flow Through or Pipeline mode
$\overline{LBO}$	Linear Order Burst mode
TMS	Test Mode Select
TDI	Test Data In
TDO	Test Data Out
TCK	Test Clock
V_{DD}	3.3 V power supply
V_{SS}	Ground
V_{DDQ}	2.5 V/3.3 V output power supply
NC	No Connect

PBGA Pin Description

Symbol	Description
An	Address Input Signals—Inputs are registered and must meet setup and hold times, as specified on **page 11**.
CLK	Clock Input Signal
$\overline{BWE}$	Byte Write Enable Signal—The byte write enable signal needs to be combined with one of the four byte write signals for a write operation to occur.
$\overline{BW1}$	Byte Write signal for data outputs 1 thru 8
$\overline{BW2}$	Byte Write signal for data outputs 9 thru 16
$\overline{GW}$	Global Write Enable
$\overline{CE1}$,CE2, $\overline{CE3}$	Chip Enables
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst address advance
$\overline{ADSP}$, $\overline{ADSC}$	Address status signals
DQ	Data Input and Output pins
DQP	Parity Input and Output pins
MATCH	Match Output
$\overline{MOE}$	Match Output Enable
$\overline{DE}$	Data Enable—Data input registers are updated only when $\overline{DE}$ is active.
ZZ	Power down control—Application of ZZ will result in a low standby power consumption.
$\overline{FT}$	Flow Through or Pipeline mode
$\overline{LBO}$	Linear Order Burst mode
TMS	Test Mode Select
TDI	Test Data In
TDO	Test Data Out
TCK	Test Clock
V_{DD}	3.3 V power supply
V_{SS}	Ground
V_{DDQ}	2.5 V/3.3 V output power supply
NC	No Connect

Functional Block Diagram



Mode Pin Function

$\overline{LBO}$	Function
L	Linear Burst
H or NC	Interleaved Burst

$\overline{FT}$	Function
L	Flow Through
H or NC	Pipeline

Power Down Control

ZZ	Function
L or NC	Active
H	Standby, IDD = ISB

Note:
There are pull up devices on $\overline{LBO}$ and $\overline{FT}$ pins and pull down device on ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Byte Write Function

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$
Read	H	H	X	X
Read	H	L	H	H
Write all bytes	L	X	X	X
Write all bytes	H	L	L	L
Write byte 1	H	L	L	H
Write byte 2	H	L	H	L

Note: H = logic high, L = logic low, NC = no connect

Synchronous Truth Table

Operation	Address Used	$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{Write}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	none	H	X	X	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power Down	none	L	L	X	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power Down	none	L	X	H	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power Down	none	L	L	X	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power Down	none	L	X	H	H	L	X	X	X	L-H	High-Z
Read Cycle, Begin Burst	external	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	external	L	H	L	L	X	X	X	H	L-H	High-Z
Read Cycle, Begin Burst	external	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	external	L	H	L	H	L	X	H	H	L-H	High-Z
$\overline{Write}$ Cycle, Begin Burst	external	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Continue Burst	next	X	X	X	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	next	X	X	X	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	next	H	X	X	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	next	H	X	X	X	H	L	H	H	L-H	High-Z
$\overline{Write}$ Cycle, Continue Burst	next	X	X	X	H	H	L	L	X	L-H	D
$\overline{Write}$ Cycle, Continue Burst	next	H	X	X	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	current	X	X	X	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	current	X	X	X	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	current	H	X	X	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	current	H	X	X	X	H	H	H	H	L-H	High-Z
$\overline{Write}$ Cycle, Suspend Burst	current	X	X	X	H	H	H	L	X	L-H	D
$\overline{Write}$ Cycle, Suspend Burst	current	H	X	X	X	H	H	L	X	L-H	D

Notes:

1. X means “don’t care,” H means “logic high,” L means “logic low.”
2. $\overline{Write}$ is the logic function of $\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$. See Byte Write Function table for detail.
3. All inputs, except $\overline{OE}$, must meet setup and hold on rising edge of CLK.
4. Suspending busrt generates a wait cycle.
5. $\overline{ADSP}$ LOW along with SRAM being selected always initiates a Read cycle at the L-H edge of the clock (CLK).
6. A Write cycle can only be performed by setting Write low for the clock L-H edge of the subsequent wait cycle. Refer to **page 12** for the Write timing diagram.

Truth Table For Read/Write/Compare/Fill Write Operation

	$\overline{CE}$	$\overline{Write}$	$\overline{DE}$	$\overline{MOE}$	$\overline{OE}$	Match	DQ
Read	L	H	X	X	L	—	Q
Write	L	L	L	X	H	—	D
Compare	L	H	L	L	H	Data Out	D
Fill Write	L	L	H	X	X	—	X
Match Deselect	H	X	X	L	X	High	High Z
Deselect	H	X	X	H	X	High Z	High Z

Notes:
1. X means "don't care," H means "logic high," L means "logic low."
2. $\overline{Write}$ is the logic function of $\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$. See Byte Write Function table for detail.
3. $\overline{CE}$ is defined as $\overline{CE1}$=L, CE2=H and $\overline{CE3}$=L
4. All signals are synchronous and are sampled by CLK except $\overline{OE}$ and $\overline{MOE}$. $\overline{OE}$ and $\overline{MOE}$ are asynchronous and drive the bus immediately.

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Absolute Maximum Ratings (Voltage reference to V_{SS} = 0 V)

Symbol	Description	Commerical	Unit
V_{DD}	Supply Voltage	–0.5 to 4.6	V
V_{DDQ}	Output Supply Voltage	–0.5 to V_{DD}	V
V_{CLK}	CLK Input Voltage	–0.5 to 6	V
V_{in}	Input Voltage	–0.5 to V_{DD} + 0.5 (≤ 4.6 V max.)	V
V_{out}	Output Voltage	–0.5 to V_{DD} + 0.5 (≤ 4.6 V max.)	V
I_{out}	Output Current per I/O	+/–20	mA
P_D	Power Dissipation	1.5	W
T_{OPR}	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximun Ratings are exceeded. Functional operation should be restricted to the recommended operation conditions. Exposure to higher than recommended voltages, for an extended period of time, could effect the performance and reliability of this component.

Package Thermal Characteristics

Rating	Layer Board	Symbol	TQFP max	PBGA max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	32	28	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	20	18	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	7	4	°C/W	3

Notes:

1. Junction temperature is a function of SRAM power dissapation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87.
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1.

AC Test Conditions
(VDD = 3.135 V–3.6 V, Ta = 0–70°C)

Parameter	Conditions
Input high level	V_{IH} = 2.3 V
Input low level	V_{IL} = 0.2 V
Input slew rate	TR = 1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.
4. Device is deselected as defined by the Truth Table.

Output load 1

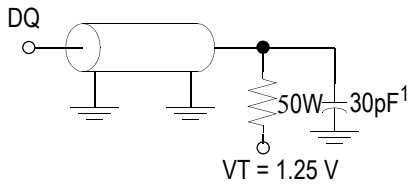


FIG. 1

Output load 2

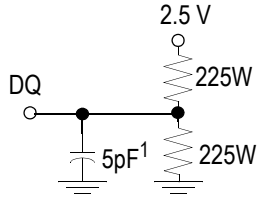


FIG. 2

DC Characteristics and Supply Currents (Voltage reference to V_{SS} = 0 V)

(VDD = 3.135 V–3.6 V, Ta = 0–70°C for Commercial Temperature Offering)

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except ZZ, FT, LBO pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	Iin_{ZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V ≤ V_{IN} ≤ V_{IH}	–1 uA –1 uA	1 uA 300 uA
Mode Input Current ($\overline{FT}$ & $\overline{LBO}$ pins)	Iin_{M}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V ≤ V_{IN} ≤ V_{IL}	–30 0uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{ol}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 2.375 V	1.7 V	
Output High Voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135 V	2.4 V	
Output Low Voltage	V_{OL}	I_{OL} = +4 mA		0.4 V

Operating Currents

Parameter	Test Conditions	Symbol	-180		-166		-150		-133		-100		Unit
			0 to 70°C	–40 to 85°C	0 to 70°C	–40 to +85°C	0 to 70°C	–40 to +85°C	0 to 70°C	–40 to +85°C	0 to 70°C	–40 to +85°C	
Operating Current	Device Selected; All other inputs ≥ V_{IH} or ≤ V_{IL} Output open	I_{DD} Pipeline	335	345	310	320	275	285	250	260	190	200	mA
		I_{DD} Flow Through	210	220	190	200	190	200	140	150	140	150	mA
Standby Current	ZZ ≥ V_{DD} – 0.2 V	I_{SB} Pipeline	20	30	30	40	30	40	30	40	30	40	mA
		I_{SB} Flow Through	20	30	30	40	30	40	30	40	30	40	mA
Deselect Supply Current	Device Deselected; All other inputs ≥ V_{IH} OR ≤ V_{IL}	I_{DD} Pipeline	55	65	110	120	105	115	100	110	80	90	mA
		I_{DD} Flow Through	40	50	80	90	80	90	65	75	65	75	mA

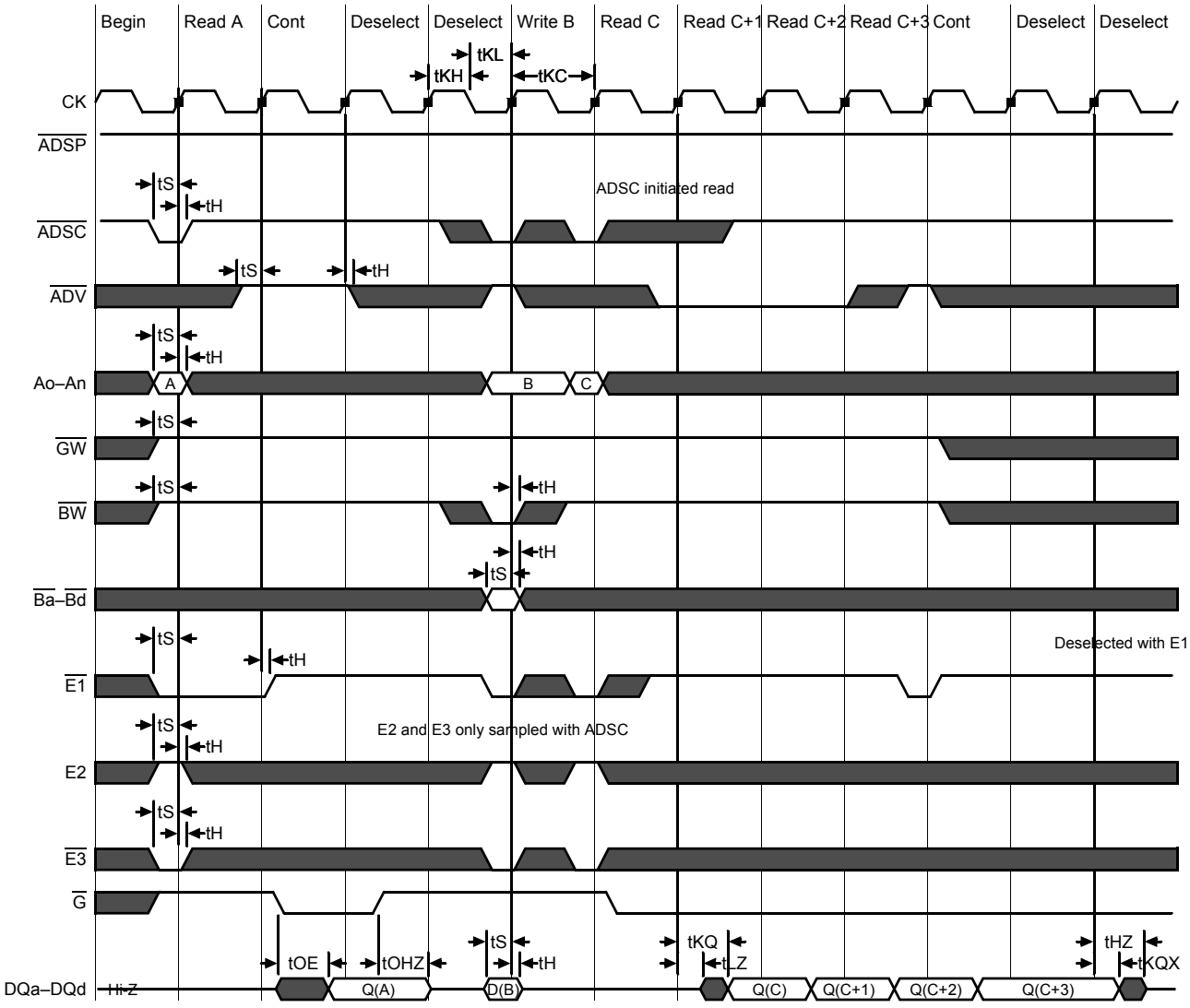
AC Electrical Characteristics

	Parameter	Symbol	-180		-166		-150		-133		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	5.5	—	6.0	—	6.7	—	7.5	—	10	—	ns
	Clock to Output Valid	tKQ	—	3.2	—	3.5	—	3.8	—	4	—	4.5	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Match Valid	tKM	—	3.2	—	3.5	—	3.8	—	4	—	4.5	ns
	Clock to Match Invalid	tKMX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Match in Low-Z	tMLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow Through	Clock Cycle Time	tKC	9.1	—	10.0	—	10.0	—	15.0	—	15.0	—	ns
	Clock to Output Valid	tKQ	—	8.0	—	8.5	—	10.0	—	11.0	—	12.0	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Match Valid	tKM	—	8.5	—	8.5	—	10.0	—	11.0	—	12.0	ns
	Clock to Match Invalid	tKMX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Match in Low-Z	tMLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.5	—	1.7	—	2	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.7	—	1.9	—	2.2	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	3.2	1.5	3.5	1.5	3.8	1.5	4	1.5	5	ns
	$\overline{OE}$ to Output Valid	tOE	—	3.2	—	3.5	—	3.8	—	4	—	5	ns
	$\overline{OE}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{OE}$ to output in High-Z	tOHZ[1]	—	3.2	—	3.5	—	3.8	—	4	—	5	ns
	$\overline{MOE}$ to Match Valid	tMOE	—	3.2	—	3.5	—	3.8	—	4	—	5	ns
	$\overline{MOE}$ to Match in Low-Z	tMOLZ[1]	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{MOE}$ to Match in High-Z	tMOHZ[1]	—	3.2	—	3.5	—	3.8	—	4	—	5	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	2.0	—	2.0	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	ns

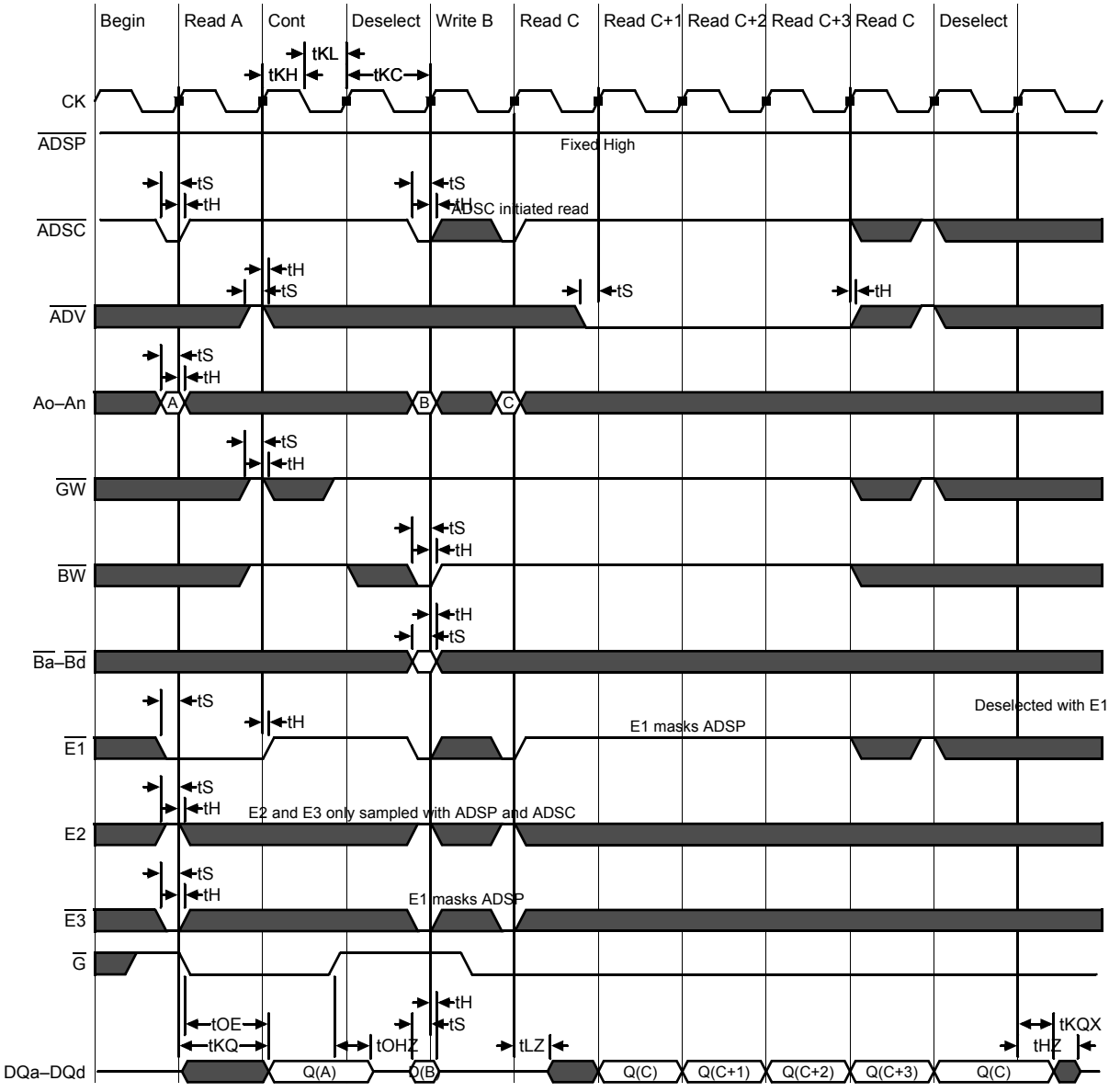
Notes:

1. These parameters are sampled and are not 100% tested
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

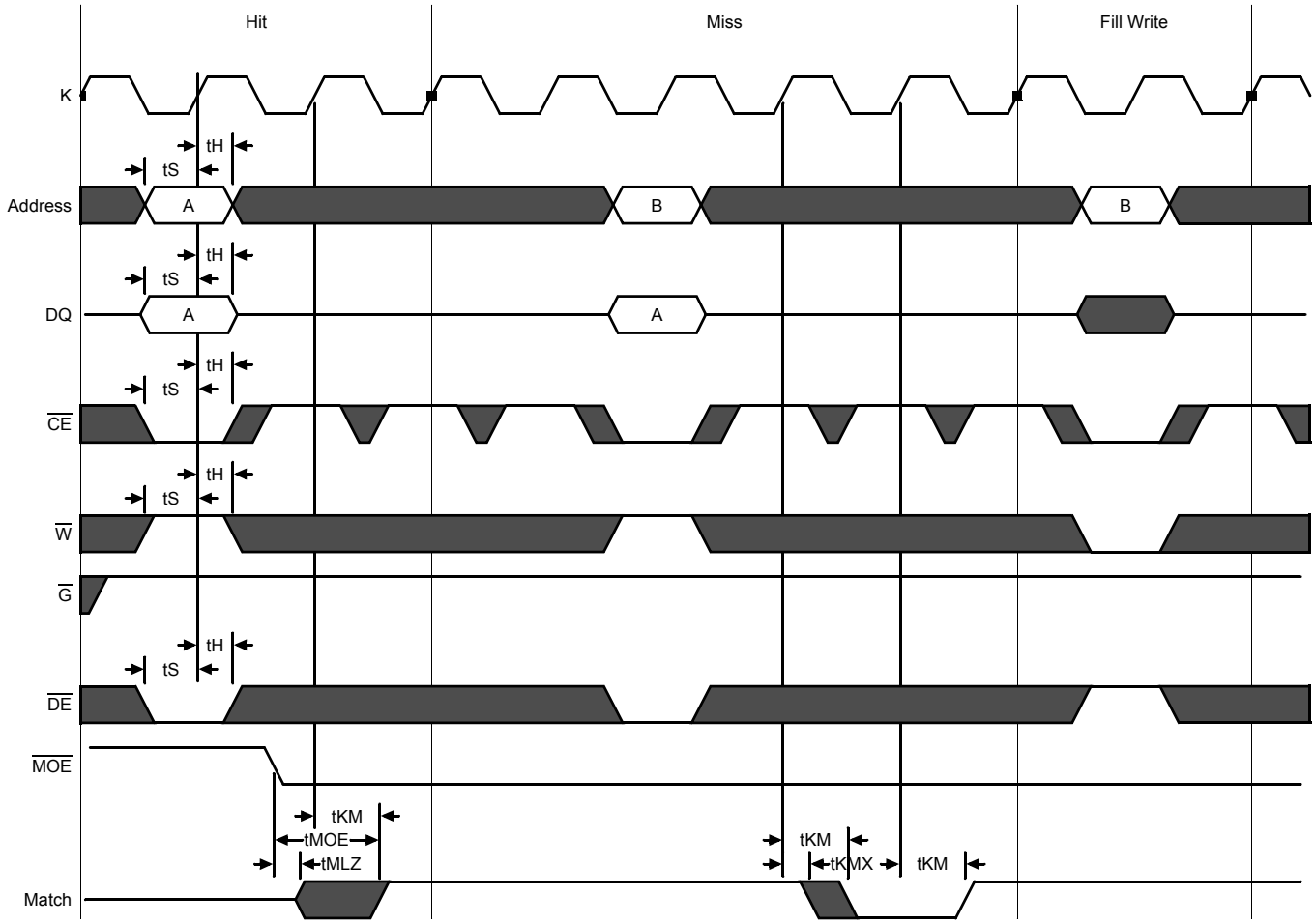
Pipeline Mode Timing



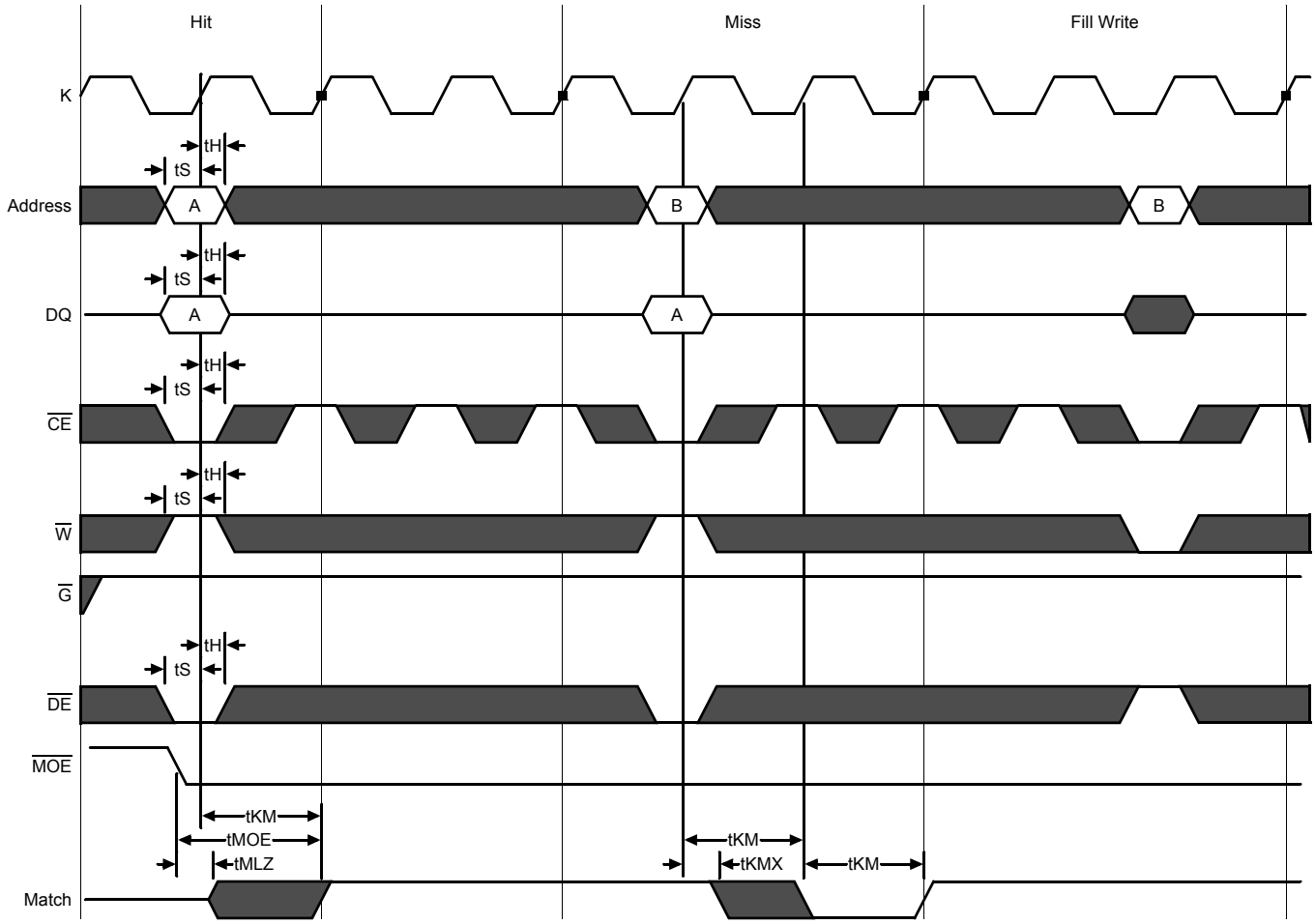
Flow Through Mode Timing



Pipeline Compare Fill Write Cycle

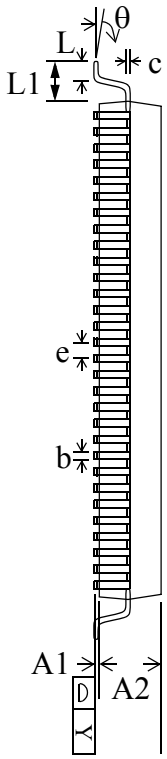


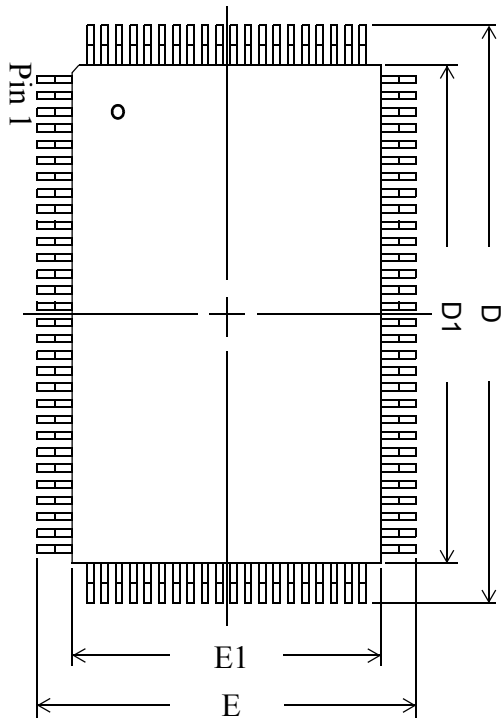
Flow Through Compare Fill Write Cycle



TQFP Package Drawing (Package T)

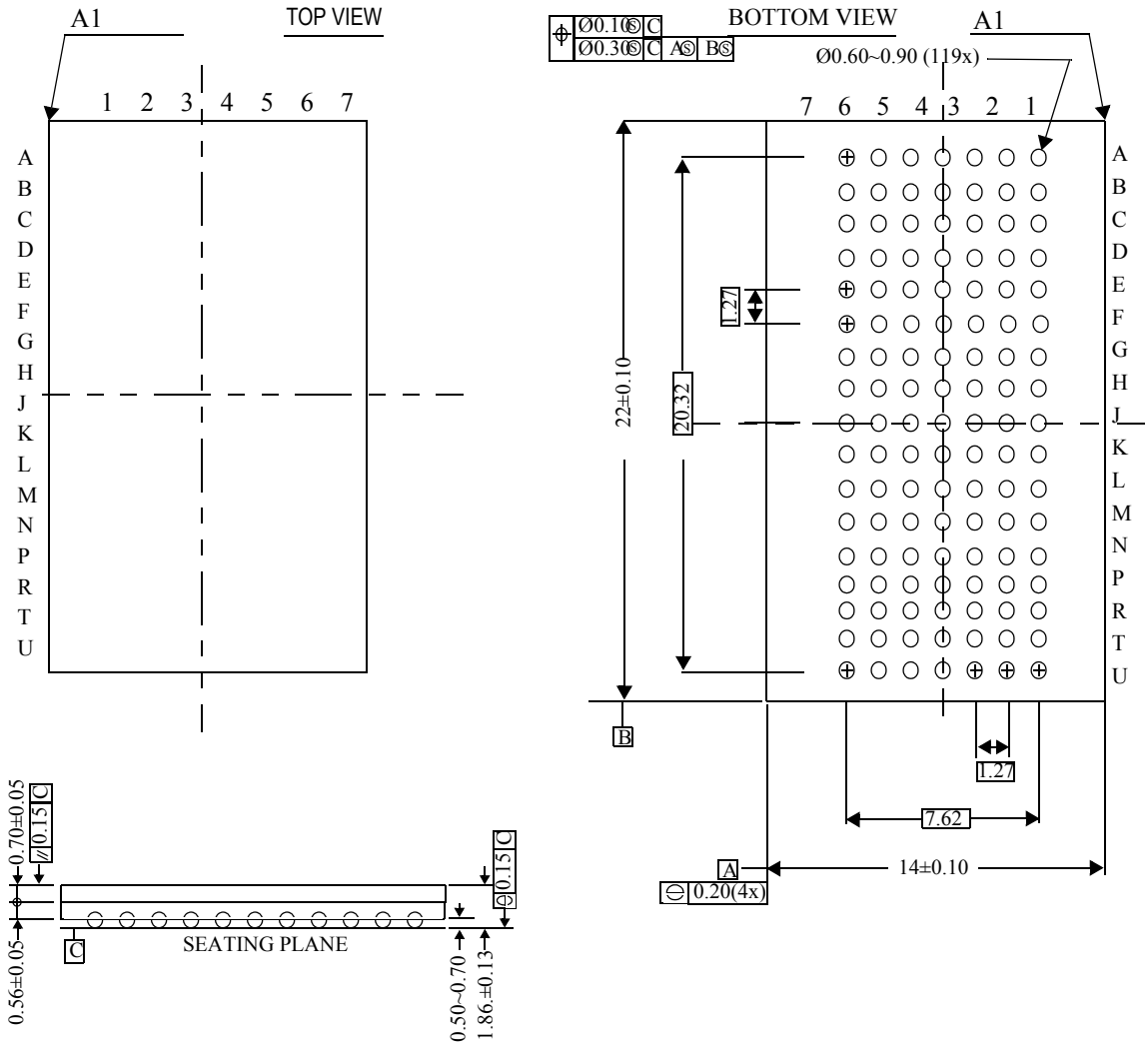
Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°





Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Package Dimensions—119-Bump FPBGA (Package B, Variation 2)



Ordering Information

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A [3]	Status
256K x 18	GS841E18AT-180	DCD Pipeline/Flow Through	TQFP	180/8	C	
256K x 18	GS841E18AT-166	DCD Pipeline/Flow Through	TQFP	166/8.5	C	
256K x 18	GS841E18AT-150	DCD Pipeline/Flow Through	TQFP	150/10	C	
256K x 18	GS841E18AT-133	DCD Pipeline/Flow Through	TQFP	133/11	C	
256K x 18	GS841E18AT-100	DCD Pipeline/Flow Through	TQFP	100/12	C	
256K x 18	GS841E18AT-180I	DCD Pipeline/Flow Through	TQFP	180/8	I	
256K x 18	GS841E18AT-166I	DCD Pipeline/Flow Through	TQFP	166/8.5	I	
256K x 18	GS841E18AT-150I	DCD Pipeline/Flow Through	TQFP	150/10	I	
256K x 18	GS841E18AT-133I	DCD Pipeline/Flow Through	TQFP	133/11	I	
256K x 18	GS841E18AT-100I	DCD Pipeline/Flow Through	TQFP	100/12	I	
256K x 18	GS841E18AGT-180	DCD Pipeline/Flow Through	Pb-Free TQFP	180/8	C	
256K x 18	GS841E18AGT-166	DCD Pipeline/Flow Through	Pb-Free TQFP	166/8.5	C	
256K x 18	GS841E18AGT-150	DCD Pipeline/Flow Through	Pb-Free TQFP	150/10	C	
256K x 18	GS841E18AGT-133	DCD Pipeline/Flow Through	Pb-Free TQFP	133/11	C	
256K x 18	GS841E18AGT-100	DCD Pipeline/Flow Through	Pb-Free TQFP	100/12	C	
256K x 18	GS841E18AGT-180I	DCD Pipeline/Flow Through	Pb-Free TQFP	180/8	I	
256K x 18	GS841E18AGT-166I	DCD Pipeline/Flow Through	Pb-Free TQFP	166/8.5	I	
256K x 18	GS841E18AGT-150I	DCD Pipeline/Flow Through	Pb-Free TQFP	150/10	I	
256K x 18	GS841E18AGT-133I	DCD Pipeline/Flow Through	Pb-Free TQFP	133/11	I	
256K x 18	GS841E18AGT-100I	DCD Pipeline/Flow Through	Pb-Free TQFP	100/12	I	
256K x 18	GS841E18AB-180	DCD Pipeline/Flow Through	119 BGA (var. 2)	180/8	C	
256K x 18	GS841E18AB-166	DCD Pipeline/Flow Through	119 BGA (var. 2)	166/8.5	C	
256K x 18	GS841E18AB-150	DCD Pipeline/Flow Through	119 BGA (var. 2)	150/10	C	
256K x 18	GS841E18AB-133	DCD Pipeline/Flow Through	119 BGA (var. 2)	133/11	C	
256K x 18	GS841E18AB-100	DCD Pipeline/Flow Through	119 BGA (var. 2)	100/12	C	
256K x 18	GS841E18AB-180I	DCD Pipeline/Flow Through	119 BGA (var. 2)	180/8	I	
256K x 18	GS841E18AB-166I	DCD Pipeline/Flow Through	119 BGA (var. 2)	166/8.5	I	
256K x 18	GS841E18AB-150I	DCD Pipeline/Flow Through	119 BGA (var. 2)	150/10	I	
256K x 18	GS841E18AI-133I	DCD Pipeline/Flow Through	119 BGA (var. 2)	133/11	I	
256K x 18	GS841E18AB-100I	DCD Pipeline/Flow Through	119 BGA (var. 2)	100/12	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS841E18AT-166T.
2. The speed column indicates the cycle frequency (Mhz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline / Flow through mode selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site for a complete listing of current offerings.

4Mb Synchronous Tag RAM Datasheet Revision History

Rev. Code: Old;New	Types of Changes Format or Content	Page /Revisions;Reason
GS841E18A_r1		• Creation of new datasheet
GS841E18A_r1; GS841E18A_r1_01	Content	• Moved TCK from U6 (incorrect placement) to U4 (correct placement) on BGA • Changed U6 to NC
GS841E18A_r1_01; GS841E18A_r1_02	Format/Content	• Updated format • Added 180 MHz speed bin • Updated timing diagrams • Updated mechanical drawings • Added Pb-Free info for TQFP
GS841E18A_r1_02; GS841E18A_r1_03	Content	• Added Pipeline Compare Fill Write Cycle and Flow Through Compare Fill Write Cycle timing diagrams

