

# DATA SHEET

## **BSP205**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

P-channel enhancement mode vertical  
D-MOS transistor

BSP205

| DESCRIPTION                                                                                                                                                 | QUICK REFERENCE DATA                                                        |               |      |             |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|---------------|------|-------------|
| P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers. | Drain-source voltage                                                        | $-V_{DS}$     | max. | 60 V        |
|                                                                                                                                                             | Drain current (DC)                                                          | $-I_D$        | max. | 275 mA      |
|                                                                                                                                                             | Drain-source ON-resistance<br>$-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$ | $R_{DS(on)}$  | max. | 10 $\Omega$ |
|                                                                                                                                                             | Gate threshold voltage                                                      | $-V_{GS(th)}$ | max. | 3.5 V       |

FEATURES

- Very low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

- 1 = gate
- 2 = drain
- 3 = source
- 4 = drain

PIN CONFIGURATION

Marking code

BSP205

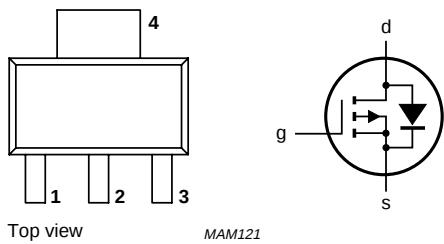


Fig.1 Simplified outline and symbol.

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D-MOS transistor**

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**BSP205**

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

|                                                                               |               |                               |                        |
|-------------------------------------------------------------------------------|---------------|-------------------------------|------------------------|
| Drain-source voltage                                                          | $-V_{DS}$     | max.                          | 60 V                   |
| Gate-source voltage (open drain)                                              | $\pm V_{GSO}$ | max.                          | 20 V                   |
| Drain current (DC)                                                            | $-I_D$        | max.                          | 275 mA                 |
| Drain current (peak)                                                          | $-I_{DM}$     | max.                          | 550 mA                 |
| Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ (note 1) | $P_{tot}$     | max.                          | 1.5 W                  |
| Storage temperature range                                                     | $T_{stg}$     | -65 to 150 $^{\circ}\text{C}$ |                        |
| Junction temperature                                                          | $T_j$         | max.                          | 150 $^{\circ}\text{C}$ |

**THERMAL RESISTANCE**

|                                   |               |   |          |
|-----------------------------------|---------------|---|----------|
| From junction to ambient (note 1) | $R_{th\ j-a}$ | = | 83.3 K/W |
|-----------------------------------|---------------|---|----------|

**Note**

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm<sup>2</sup>.

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BSP205

## CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$-I_D = 10\text{ }\mu\text{A}$ ;  $V_{GS} = 0$

$-V_{(BR)DSS}$  min. 60 V

Drain-source leakage current

$-V_{DS} = 48\text{ V}$ ;  $V_{GS} = 0$

$-I_{DSS}$  max. 1.0  $\mu\text{A}$

Gate-source leakage current

$\pm V_{GS} = 20\text{ V}$ ;  $V_{DS} = 0$

$\pm I_{GSS}$  max. 100 nA

Gate threshold voltage

$-I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

$-V_{GS(th)}$  min. 1.5 V  
max. 3.5 V

Drain-source ON-resistance

$-I_D = 200\text{ mA}$ ;  $-V_{GS} = 10\text{ V}$

$R_{DS(on)}$  typ. 7.5  $\Omega$   
max. 10  $\Omega$

Transfer admittance

$-I_D = 200\text{ mA}$ ;  $-V_{DS} = 15\text{ V}$

$|Y_{fs}|$  min. 60 mS  
typ. 125 mS

Input capacitance at  $f = 1\text{ MHz}$ ;

$-V_{DS} = 10\text{ V}$ ;  $V_{GS} = 0$

$C_{iss}$  typ. 30 pF  
max. 45 pF

Output capacitance at  $f = 1\text{ MHz}$ ;

$-V_{DS} = 10\text{ V}$ ;  $V_{GS} = 0$

$C_{oss}$  typ. 20 pF  
max. 30 pF

Feedback capacitance at  $f = 1\text{ MHz}$ ;

$-V_{DS} = 10\text{ V}$ ;  $V_{GS} = 0$

$C_{rss}$  typ. 5 pF  
max. 10 pF

Switching times (see Figs 2 and 3)

$-I_D = 200\text{ mA}$ ;  $-V_{DD} = 50\text{ V}$ ;

$-V_{GS} = 0$  to  $10\text{ V}$

$t_{on}$  typ. 3 ns  
max. 6 ns

$t_{off}$  typ. 10 ns  
max. 15 ns

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BSP205

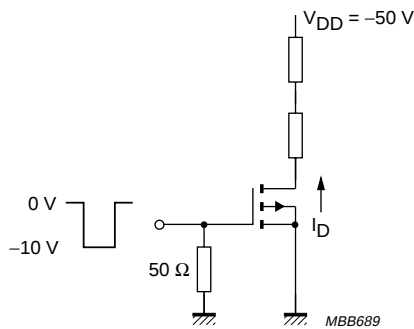


Fig.2 Switching time test circuit.

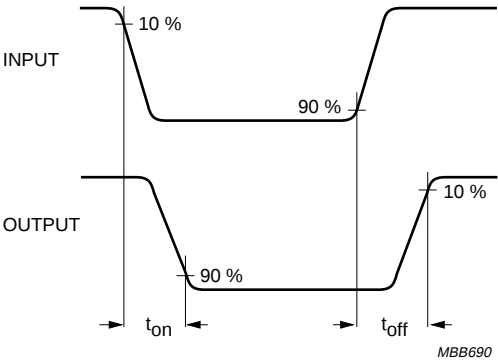


Fig.3 Input and output waveforms.

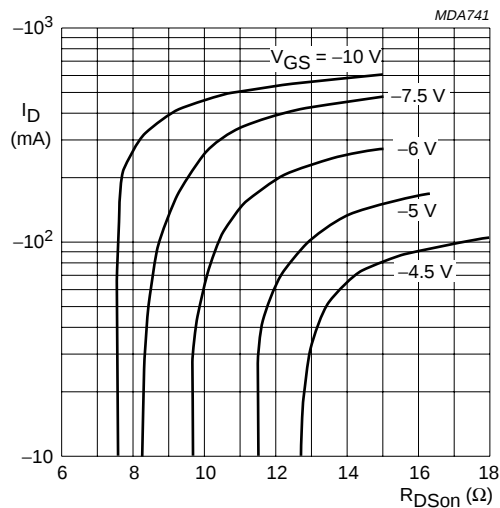


Fig.4 ON-resistance as a function of drain current;  $T_j = 25^\circ\text{C}$ ; typical values.

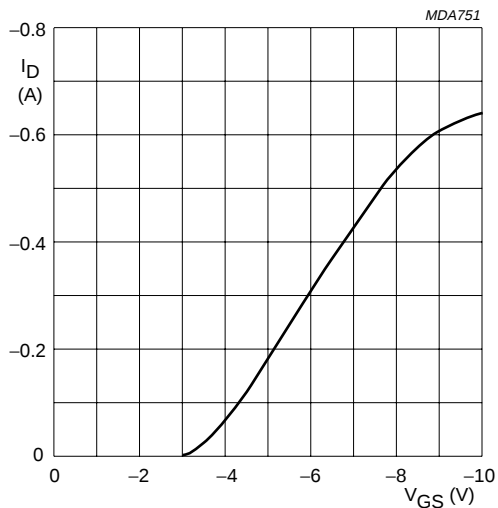


Fig.5 Transfer characteristics;  $-V_{DS} = 10$  V;  $T_j = 25^\circ\text{C}$ ; typical values.

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BSP205

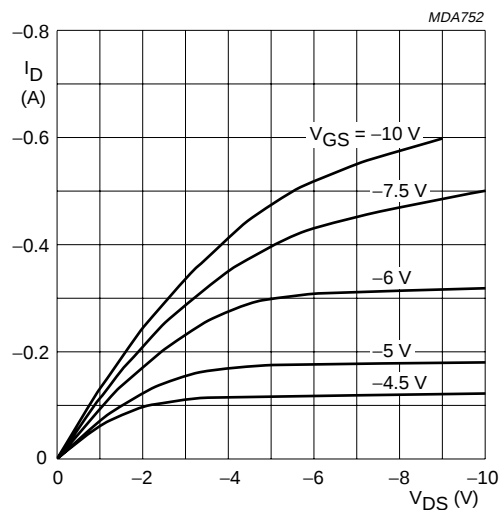


Fig.6 Output characteristics;  $T_j = 25\text{ }^{\circ}\text{C}$ ; typical values.

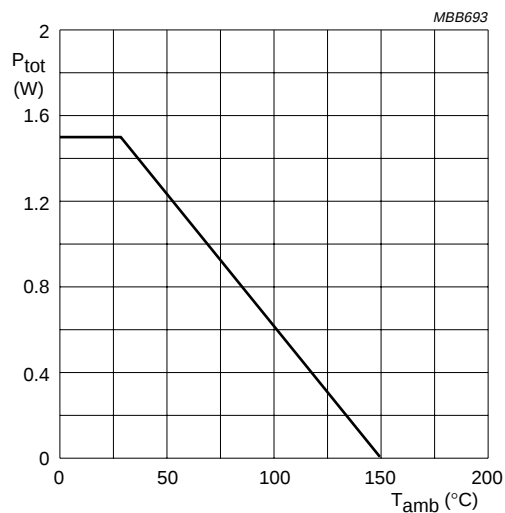


Fig.7 Power derating curve.

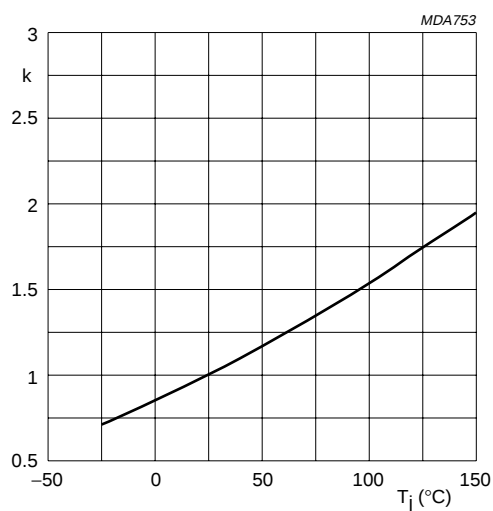


Fig.8

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\text{ }^{\circ}\text{C}};$$

at  $-200\text{ mA}/-10\text{ V}$ ; typical values.

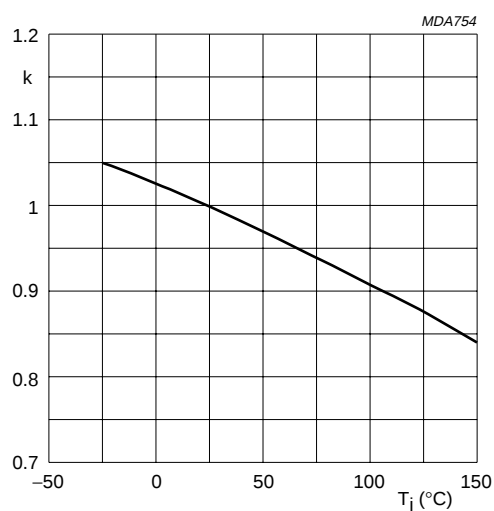


Fig.9

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\text{ }^{\circ}\text{C}};$$

$-V_{GS(th)}$  at  $-1\text{ mA}$ ; typical values.

P-channel enhancement mode vertical  
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BSP205

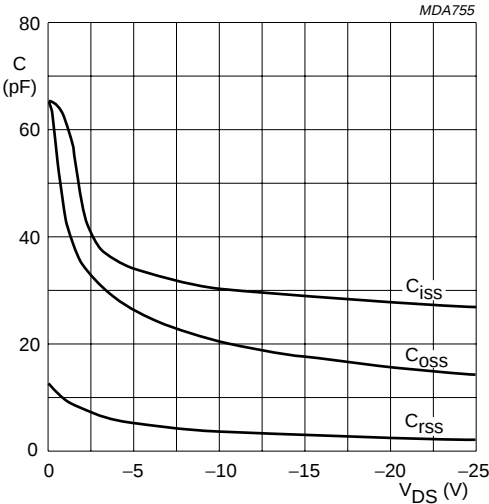


Fig.10  $T_j = 25\text{ }^{\circ}\text{C}$ ;  $V_{GS} = 0$ ;  $f = 1\text{ MHz}$ ; typical values.

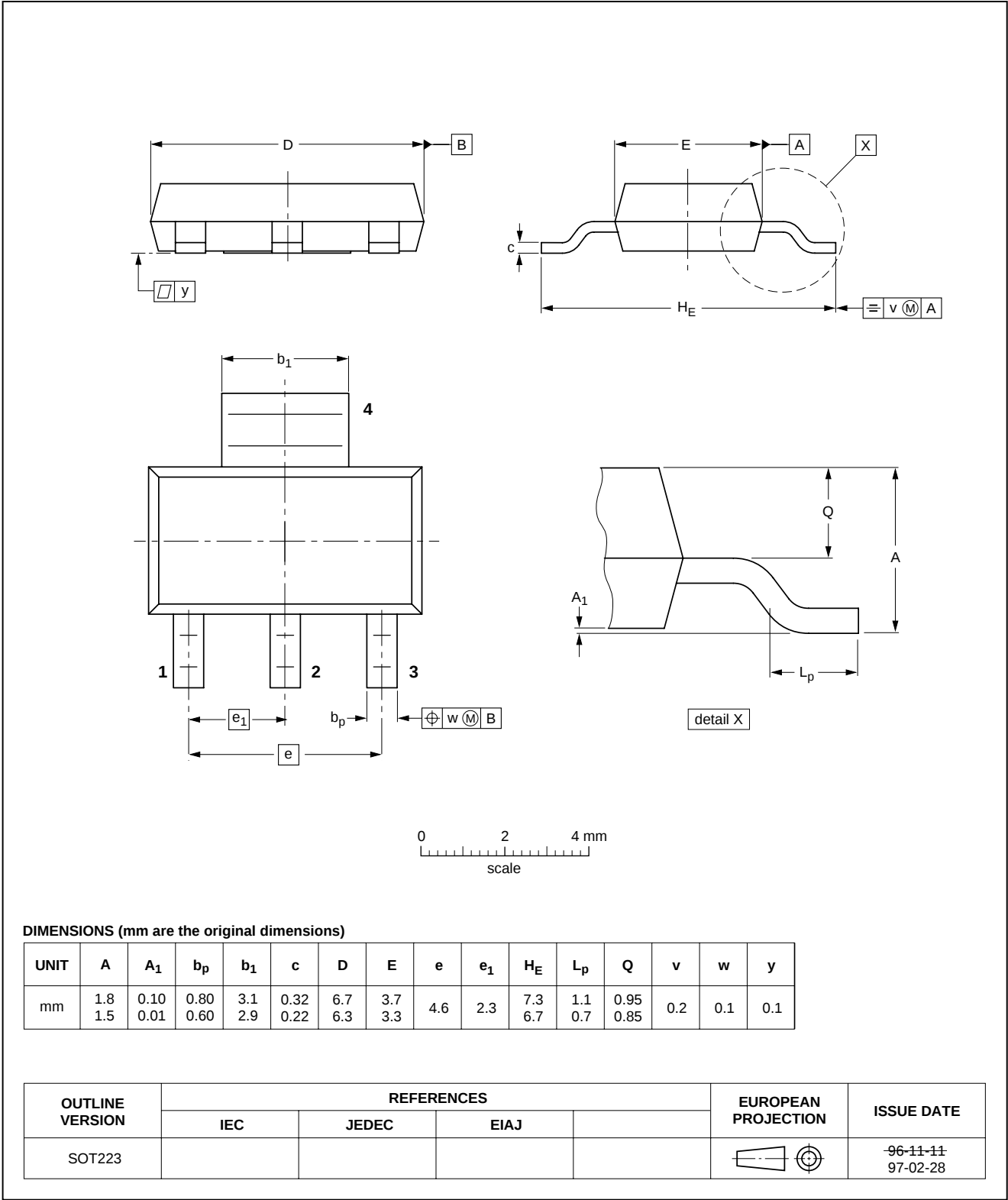
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BSP205

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



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**BSP205****DEFINITIONS**

| <b>Data sheet status</b>                                                                            |                                                                                       |
|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                             | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                           | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                               | This data sheet contains final product specifications.                                |
| <b>Application information</b>                                                                      |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification. |                                                                                       |

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**NOTES**

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**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
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**Belgium:** see The Netherlands

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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
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**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
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**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
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**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
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**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

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**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
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**Portugal:** see Spain

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Tel. +7 095 755 6918, Fax. +7 095 755 6919

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
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**Spain:** Balmes 22, 08007 BARCELONA,  
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**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
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Printed in The Netherlands

137107/1200/01/pp12

Date of release: April 1995

Document order number: 9397 750 02479

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