M2S56D20/ 30/ 40ATP
M2S56D20/ 30/ 40AKT
256M Double Data Rate Synchronous DRAM

DESCRIPTION

M2S56D20ATP / AKT is a 4-bank x 16777216-word x 4-bit,
M2S56D30ATP / AKT is a 4-bank x 8388608-word x 8-bit,
M2S56D40ATP/ AKT is a 4-bank x 4194304-word x 16-bit,
double data rate synchronous DRAM, with SSTL_2 interface. All control and address signals are referenced to the rising edge of CLK.Input data is registered on both edges of data strobes, and output data and data strobe are referenced on both edges of CLK. The M2S56D20/30/40A achieve very high speed data rate up to 166MHz(-60), 133MHz(-75A/-75) and are suitable for main memory in computer systems.

FEATURES

- VDD=VDDQ=2.5V±0.2V
- Double data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data
- Differential clock inputs (CLK and /CLK)
- DLL aligns DQ and DQS transitions
- Commands are entered on each positive CLK edge
- Data and data mask are referenced to both edges of DQS
- 4-bank operations are controlled by BA0, BA1 (Bank Address)
- /CAS latency- 2.0/2.5 (programmable)
- Burst length- 2/4/8 (programmable)
- Burst type- sequential / interleave (programmable)
- Auto precharge / All bank precharge is controlled by A10
- 8192 refresh cycles /64ms (4 banks concurrent refresh)
- Auto refresh and Self refresh
- Row address A0-12 / Column address A0-9,11(x4) / A0-9(x8) / A0-8(x16)
- SSTL_2 Interface
- Both 66-pin TSOP Package and 64-pin Small TSOP Package
  M2S56D*0ATP: 0.65mm lead pitch 66-pin TSOP Package
  M2S56D*0AKT: 0.4mm lead pitch 64-pin Small TSOP Package
- JEDEC standard
- Low Power for the Self Refresh Current
  Ultra Low Power Version : ICC6 ≤ 1mA (-60UL , -75AU , -75UL)
  Low Power Version : ICC6 ≤ 2mA (-60L , -75AL , -75L)

Operating Frequencies

	Max. Frequency @CL=2.0 *	Max. Frequency @CL=2.5 *	Standard
M2S56D20/30/40ATP - 60UL / - 60L / - 60 M2S56D20/30/40AKT - 60UL / - 60L / - 60	133MHz	166MHz	DDR333B
M2S56D20/30/40ATP - 75AU / - 75AL / - 75A M2S56D20/30/40AKT - 75AU / - 75AL / - 75A	133MHz	133MHz	DDR266A
M2S56D20/30/40ATP - 75UL / - 75L / - 75 M2S56D20/30/40AKT - 75UL / - 75L / - 75	100MHz	133MHz	DDR266B

* CL = CAS(Read) Latency

This Product became EOL in July, 2004.

EOL product

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PIN CONFIGURATION 1 (TOP VIEW)

x4
x8
x16

VDD	VDD	VDD	1	66	VSS	VSS	VSS
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	NC	NC	NC
VDD	VDD	VDD	18	49	VREF	VREF	VREF
NC	NC	NC	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
/WE	/WE	/WE	21	46	/CLK	/CLK	/CLK
/CAS	/CAS	/CAS	22	45	CLK	CLK	CLK
/RAS	/RAS	/RAS	23	44	CKE	CKE	CKE
/CS	/CS	/CS	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

66pin TSOP(II)

400mil width
x
875mil length

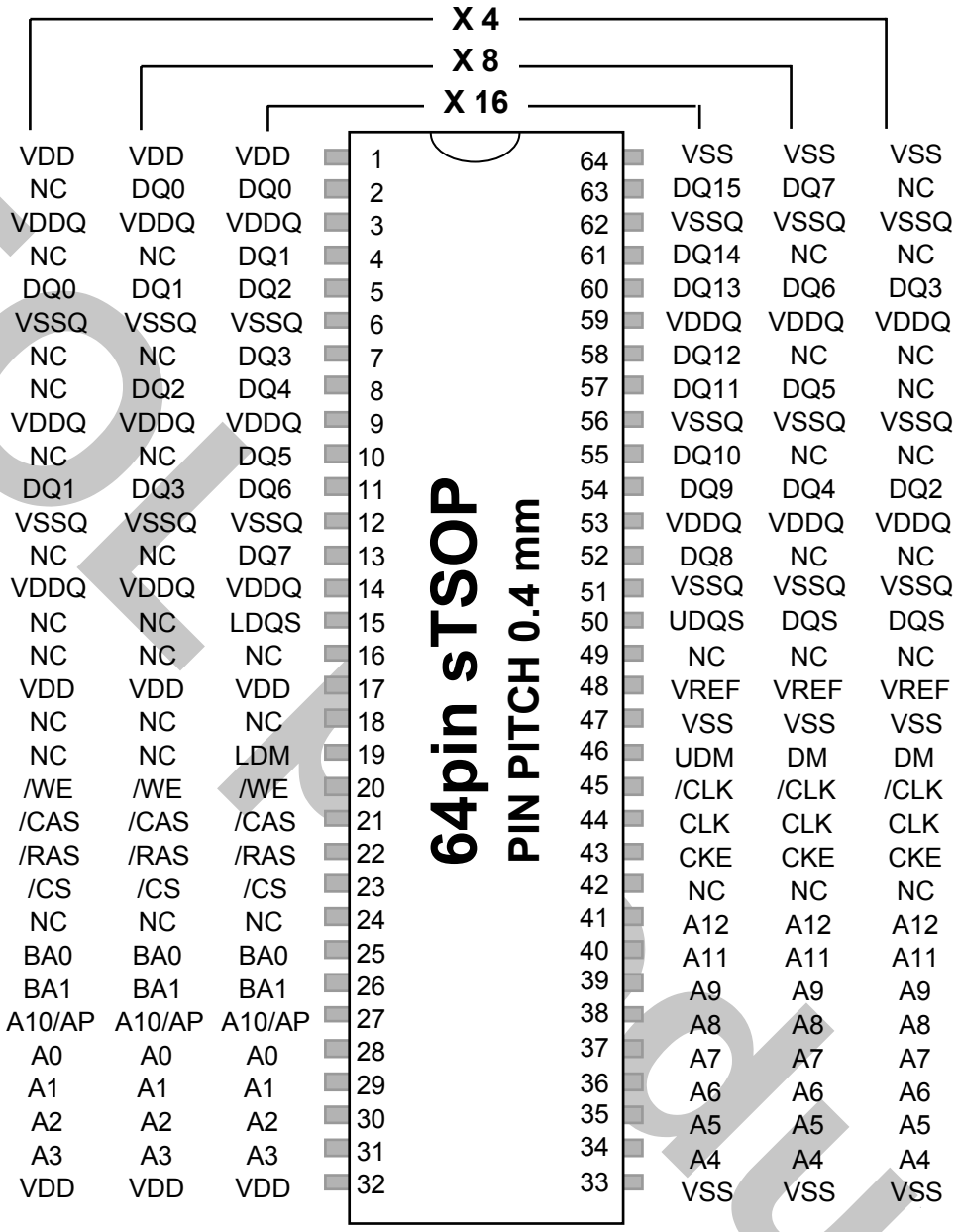
0.65mm
Lead Pitch

ROW
A0-12
Column
A0-9,11(x4)
A0-9 (x8)
A0-8 (x16)

CLK,/CLK	**: Master Clock**
CKE	**: Clock Enable**
/CS	**: Chip Select**
/RAS	**: Row Address Strobe**
/CAS	**: Column Address Strobe**
/WE	**: Write Enable**
DQ0-15	**: Data I/O**
DQS LDQS,UDQS	**: Data Strobe**
DM LDM,UDM	**: Write Mask**
VREF	**: Reference Voltage**
A0-12	**: Address Input**
BA0,1	**: Bank Address Input**
VDD	**: Power Supply**
VDDQ	**: Power Supply for Output**
VSS	**: Ground**
VSSQ	**: Ground for Output**

EOL product

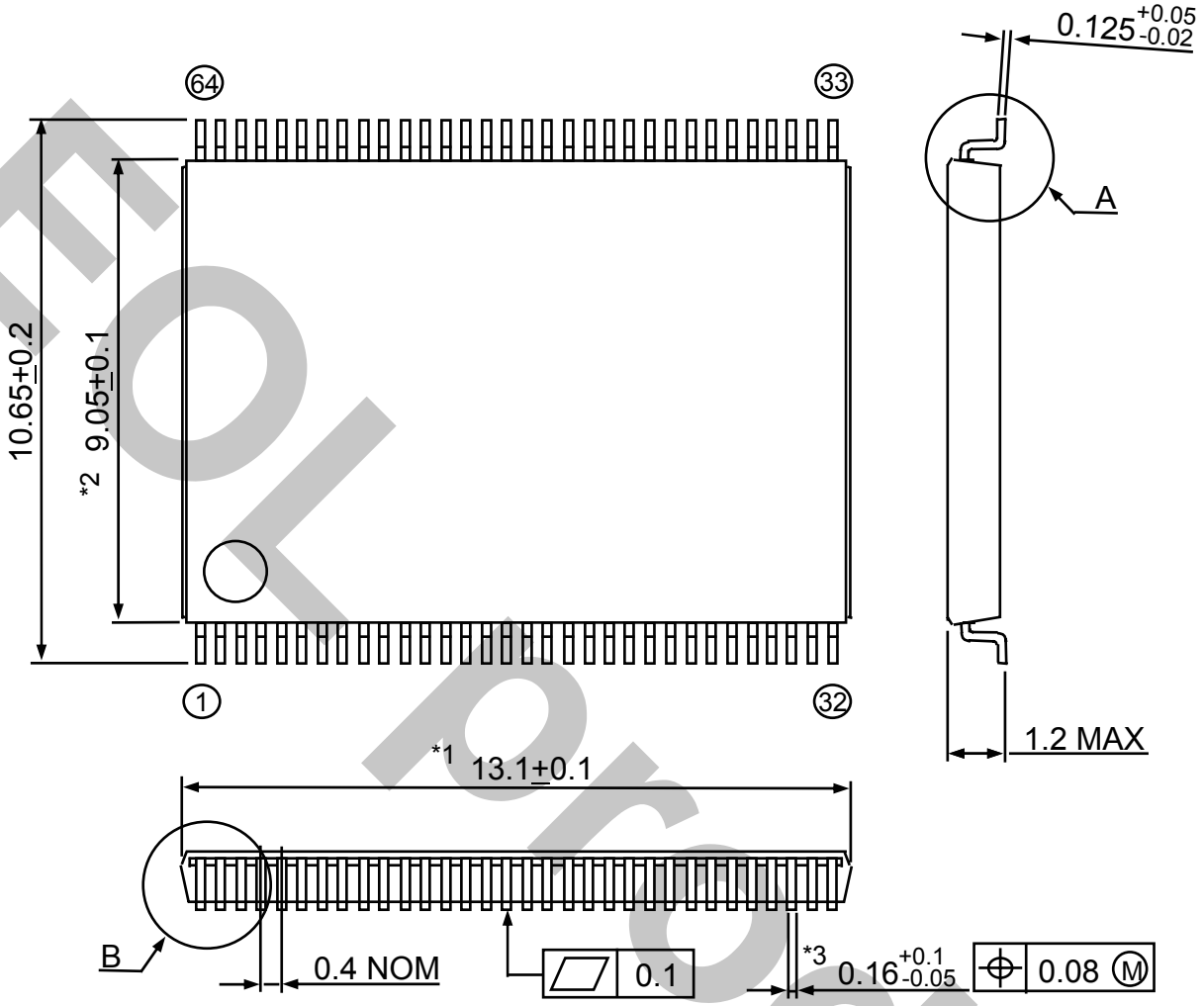
PIN CONFIGURATION 2 (TOP VIEW)

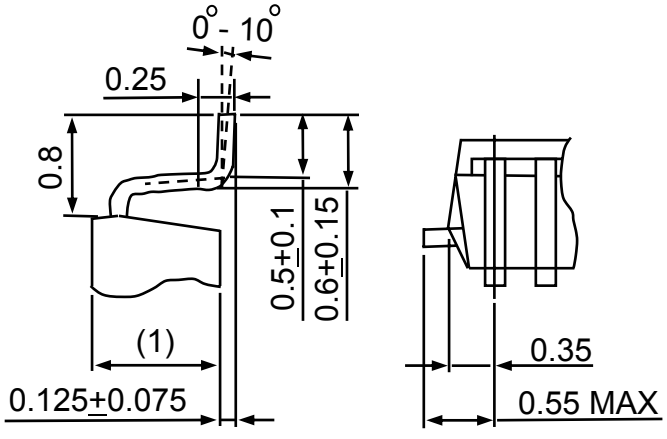


CLK,/CLK	**: Master Clock**
CKE	**: Clock Enable**
/CS	**: Chip Select**
/RAS	**: Row Address Strobe**
/CAS	**: Column Address Strobe**
/WE	**: Write Enable**
DQ0-15	**: Data I/O**
DQS LDQS,UDQS	**: Data Strobe**
DM LDM,UDM	**: Write Mask**
VREF	**: Reference Voltage**
A0-12	**: Address Input**
BA0,1	**: Bank Address Input**
VDD	**: Power Supply**
VDDQ	**: Power Supply for Output**
VSS	**: Ground**
VSSQ	**: Ground for Output**

EO Product

PACKAGE OUTLINE OF sTSOP





Detail A (NTS) Detail B (NTS)

Note)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

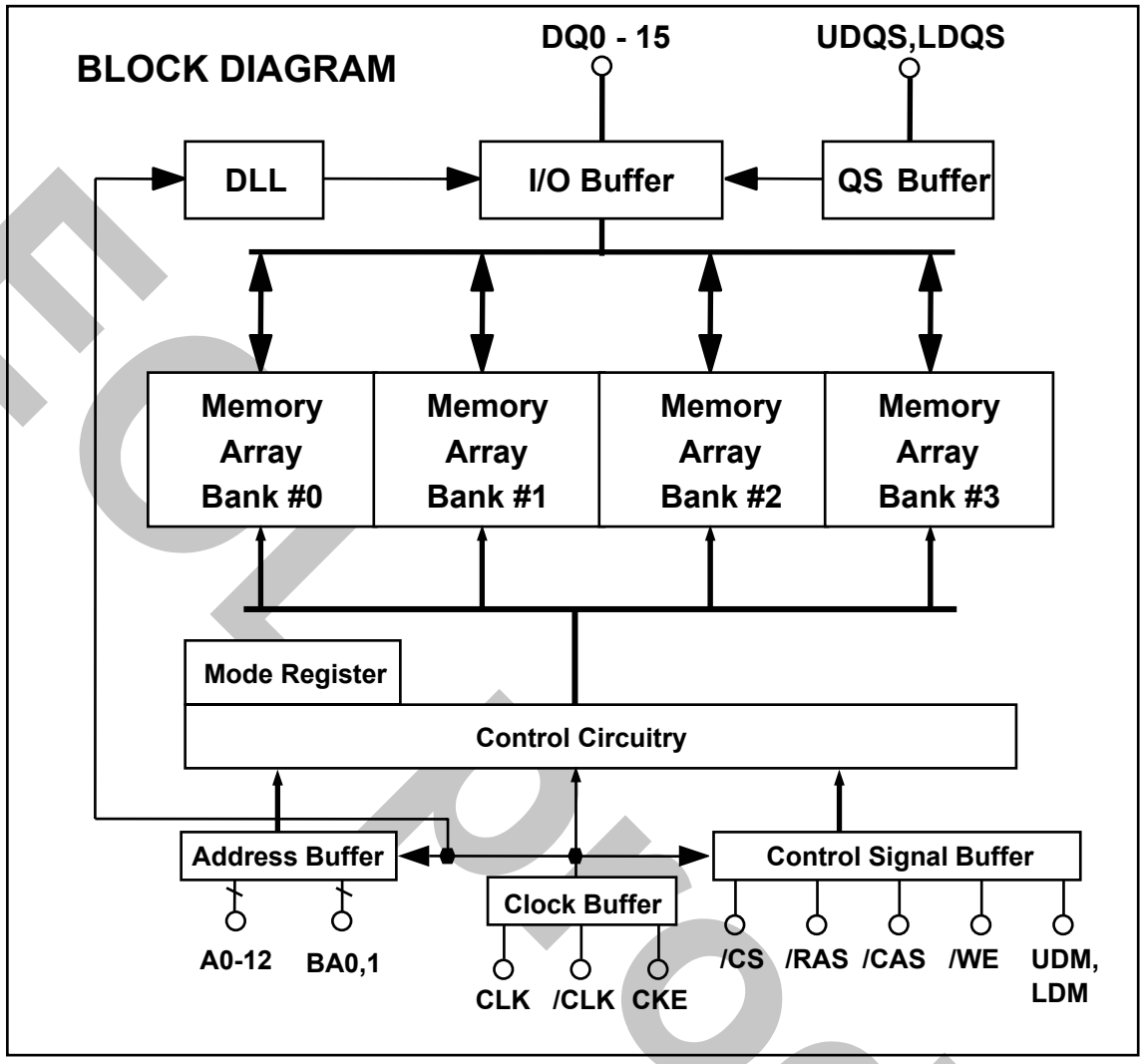
EOL product

PIN FUNCTION

SYMBOL	TYPE	DESCRIPTION
CLK, /CLK	Input	Clock: CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh.After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-12	Input	A0-12 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-12. The Column Address is specified by A0-9,11(x4), A0-9(x8) and A0-8(x16). A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
DQ0-15(x16), DQ0-7(x8), DQ0-3(x4),	Input / Output	Data Input/Output: Data bus
DQS	Input / Output	Data Strobe: Output pin during Read operation, input pin during Write operation. Edge-aligned with read data, placed at the centered of write data to capture the write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS correspond to the data on DQ8-DQ15.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a WRITE operations. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15.
VDD, VSS	Power Supply	Power Supply for the memory array and peripheral circuitry.
VDDQ, VSSQ	Power Supply	VDDQ and VSSQ are supplied to the Output Buffers only.
VREF	Input	SSTL_2 reference voltage.

EOL Product

BLOCK DIAGRAM



TYPE DESIGNATION CODE

This rule is applied to only Synchronous DRAM family.

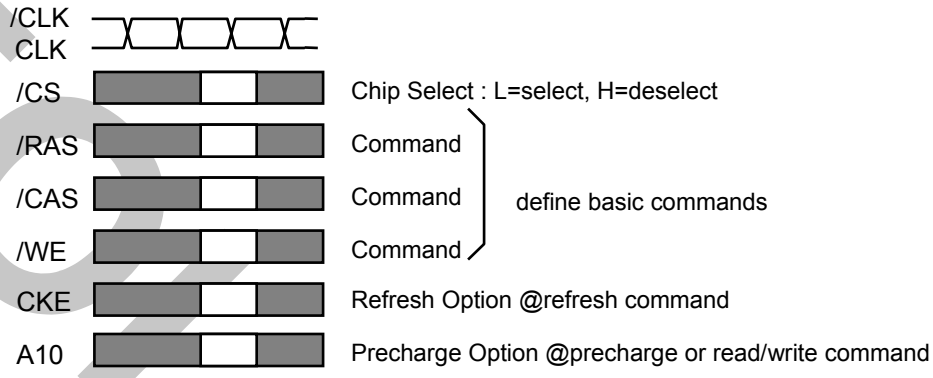
M 2 S 56 D 3 0 A KT – 60 UL

- Power Grade UL/U: Ultra Low power L: Low power, Blank: standard
- Speed Grade 75: 133MHz@CL=2.5,100MHz@CL=2.0 (DDR266B)
  75A: 133MHz@CL=2.5,133MHz@CL=2.0 (DDR266A)
  60: 166MHz@CL=2.5,133MHz@CL=2.0 (DDR333B)
- Package Type TP: TSOP(II), KT: sTSOP(Small TSOP)
- Process Generation
- Function Reserved for Future Use
- Organization 2^n 2: x4, 3: x8, 4: x16
- **DDR Synchronous DRAM**
- Density 56: 256M bits
- Interface V:LVTTL, S:SSTL_3, _2
- Memory Style (DRAM)
- Mitsubishi Main Designation

EOL Product

BASIC FUNCTIONS

The M2S56D20/30/40A provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS ,CKE and A10 are used as chip select, refresh option, and precharge option, respectively. Refer to the command truth table for the detailed definition of commands.



Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates one row in an idle bank indicated by BA.

Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H in this command, the bank is deactivated after the burst read (auto-precharge, **READA**)

Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is defined by burst length. When A10 =H in this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**)

Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read /write operation. When A10 =H in this command, all banks are deactivated (precharge all, **PREA**).

Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh addresses including bank address are generated internally. After this command, the banks are precharged automatically.

EOL product

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	BA0,1	A10 /AP	A0-9, 11-12	Note
Deselect	DESEL	H	X	H	X	X	X	X	X	X	
No Operation	NOP	H	X	L	H	H	H	X	X	X	
Row Address Entry & Bank Activate	ACT	H	H	L	L	H	H	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	V	L	X	
Precharge All Banks	PREA	H	H	L	L	H	L	X	H	X	
Column Address Entry & Write	WRITE	H	H	L	H	L	L	V	L	V	
Column Address Entry & Write with Auto-Precharge	WRITEA	H	H	L	H	L	L	V	H	V	
Column Address Entry & Read	READ	H	H	L	H	L	H	V	L	V	
Column Address Entry & Read with Auto-Precharge	READA	H	H	L	H	L	H	V	H	V	
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	
		L	H	L	H	H	H	X	X	X	
Burst Terminate	TERM	H	H	L	H	H	L	X	X	X	1
Mode Register Set	MRS	H	H	L	L	L	L	L	L	V	2

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. Applies only to read bursts while autoprecharge is disabled; this command is undefined (and should not be used) during read bursts while autoprecharge is enabled, as well as during write bursts.

2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register;BA0=1 ,BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-codes to be written to the selected Mode Register.

Not product

FUNCTION TRUTH TABLE (1/4)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
IDLE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA	
	L	L	H	L	BA, A10	PRE / PREA	NOP	4
	L	L	L	H	X	REFA	Auto-Refresh	5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set	5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	NOP	
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ(Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	Terminate Burst	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

E0 Product

FUNCTION TRUTH TABLE (2/4)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
WRITE(Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge	3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ with Auto-Precharge	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL for Same Bank	6
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL for Same Bank	6
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE with Auto-Precharge	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL for Same Bank	7
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL for Same Bank	7
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

Eol for Product

FUNCTION TRUTH TABLE (3/4)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
PRE-CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)	
	L	H	H	H	X	NOP	NOP (Idle after tRP)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	NOP (Idle after tRP)	4
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)	
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

Eol Product

FUNCTION TRUTH TABLE (4/4)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
REFRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRFC)	
	L	H	H	H	X	NOP	NOP (Idle after tRFC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tMRD)	
	L	H	H	H	X	NOP	NOP (Idle after tMRD)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:
1. All entries are valid only when CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of specific bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Refer to Read with Auto-Precharge in page 28.
7. Refer to Write with Auto-Precharge in page 30.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

EOL product

FUNCTION TRUTH TABLE for CKE

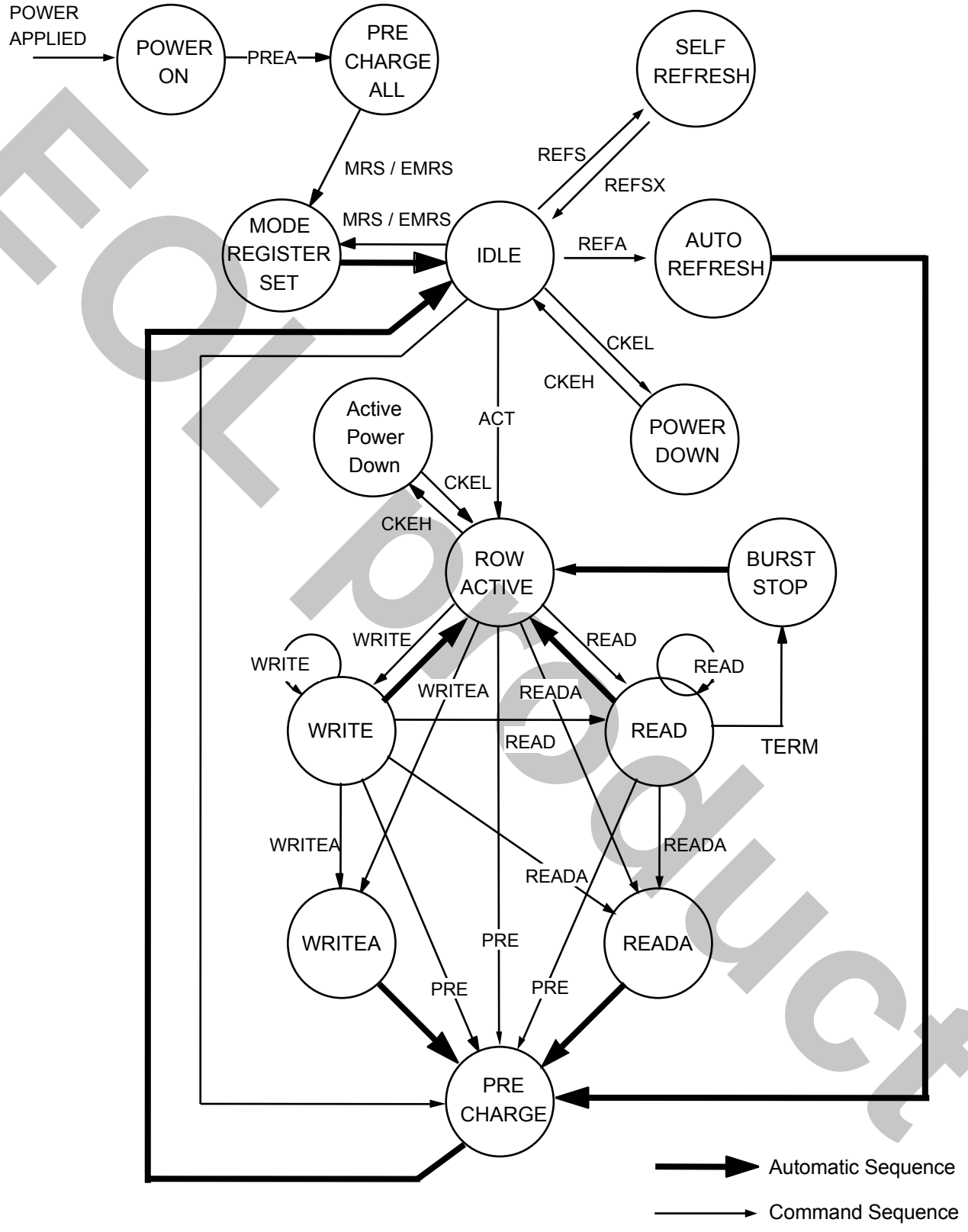
Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Address	Action	Notes
SELF-REFRESHING	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRFC)	1
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRFC)	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	L	X	X	ILLEGAL	1
	L	H	L	L	X	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)	1
POWER DOWN	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power Down to Idle	
	L	L	X	X	X	X	X	NOP (Maintain Power Down)	
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function Truth Table	2
	H	L	L	L	L	H	X	Enter Self-Refresh	2
	H	L	H	X	X	X	X	Enter Power Down	2
	H	L	L	H	H	H	X	Enter Power Down	2
	H	L	L	H	H	L	X	ILLEGAL	2
	H	L	L	H	L	X	X	ILLEGAL	2
	H	L	L	L	X	X	X	ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Current State =Power Down	2
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle	3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle	3
	L	L	X	X	X	X	X	Maintain CLK Suspend	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. Low to High transition of CKE re-enable CLK and other inputs asynchronously.
   A minimum setup time must be satisfied before any command except REFSX.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

Eol product

SIMPLIFIED STATE DIAGRAM



EOL Product

POWER ON SEQUENCE

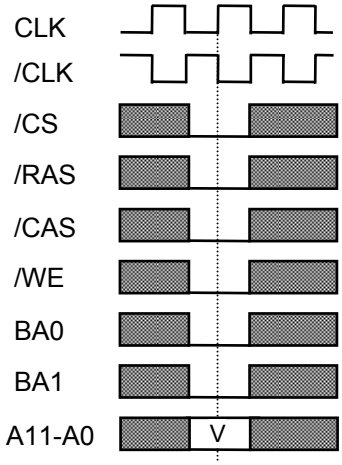
The following power on sequences are necessary to guarantee the proper operations of the DDR SDRAM.

1. Apply VDD before or at the same time as VDDQ
2. Apply VDDQ before or at the same time as VTT & VREF
3. Maintain stable conditions for 200us after stable power and CLK are applied, assert NOP or DSEL
4. Issue Precharge command for all banks of the device
5. Issue EMRS to program proper functions
6. Issue MRS to configure the Mode Register and to reset the DLL
7. Issue 2 or more Auto Refresh commands
8. Maintain stable conditions for 200 cycle

After these sequences, the DDR SDRAM is in the idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by configuring the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After tMRD from an MRS command, the DDR SDRAM is ready to accept the new command.



BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	DR	0	LTMODE			BT	BL		

	CL	/CAS Latency
Latency Mode	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	R
	1 0 0	R
	1 0 1	R
	1 1 0	2.5
	1 1 1	R

	BL	BT=0	BT=1
Burst Length	0 0 0	R	R
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	R	R

DLL Reset	0	NO
	1	YES

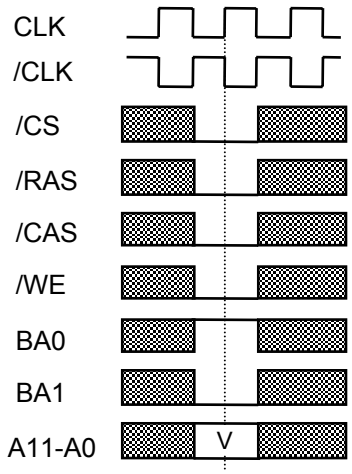
Burst Type	0	Sequential
	1	Interleaved

R: Reserved for Future Use

Eol Project

EXTENDED MODE REGISTER

DLL disable / enable mode can be programmed in the extended mode register (EMRS). The extended mode register stores these data until the next EMRS command, which may be issued when all banks are in idle state. After tMRD from a EMRS command, the DDR SDRAM is ready to accept the new command.

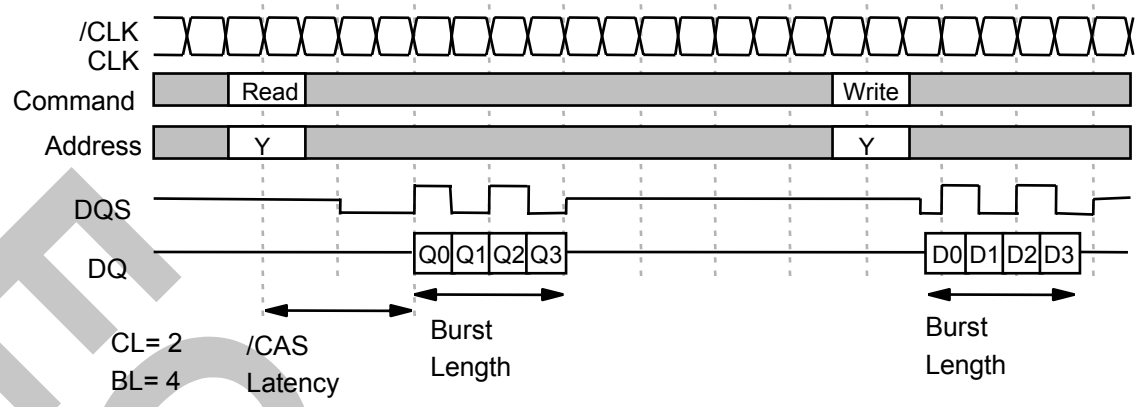


BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	0	0	0	0	0	0	DS	DD

DLL Disable	0	DLL Enable
	1	DLL Disable

Drive Strength	0	Normal
	1	Weak (Optional)

EOL product



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

EOL Product

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VDD	Supply Voltage	with respect to VSS	-0.5 to 3.7	V
VDDQ	Supply Voltage for Output	with respect to VSSQ	-0.5 to 3.7	V
VI	Input Voltage	with respect to VSS	-0.5 to VDD+0.5	V
VO	Output Voltage	with respect to VSSQ	-0.5 to VDDQ+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	TA = 25 °C	1000	mW
Topr	Operating Temperature		0 to 70	°C
Tstg	Storage Temperature		-65 to 150	°C

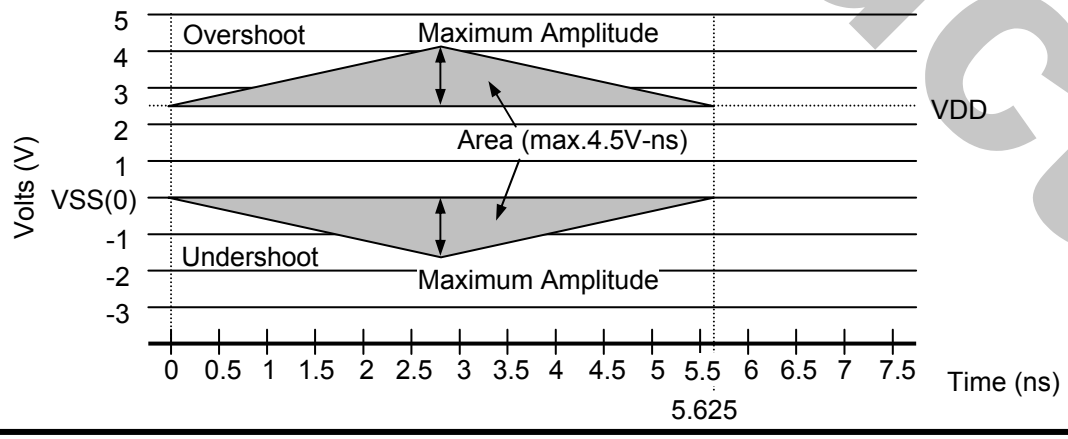
DC OPERATING CONDITIONS

(TA=0 to 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	2.3	2.5	2.7	V	
VDDQ	Supply Voltage for Output	2.3	2.5	2.7	V	
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	5
VIH(DC)	High-Level Input Voltage	VREF + 0.15		VDDQ+0.3	V	
VIL(DC)	Low-Level Input Voltage	-0.3		VREF - 0.15	V	
VIN(DC)	Input Voltage Level, CLK and /CLK	-0.3		VDDQ + 0.3	V	
VID(DC)	Input Differential Voltage, CLK and /CLK	0.36		VDDQ + 0.6	V	7
VTT	I/O Termination Voltage	VREF - 0.04		VREF + 0.04	V	6

AC OVERSHOOT/UNDERSHOOT SPECIFICATION

Parameter	Specification
Maximum peak amplitude allowed for overshoot	1.6V
Maximum peak amplitude allowed for undershoot	1.6V
The area between the overshoot signal and VDD must be less than or euqal to	4.5 V-ns
The area between the undershoot signal and VSS must be less than or euqal to	4.5 V-ns



Not for Product

AVERAGE SUPPLY CURRENT from VDD

(TA=0 to 70°C, VDD = VDDQ = 2.5V ± 0.2V, VSS = VSSQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/Test Conditions	Organization	Limits(Max.)		Unit	Notes
			-60	-75A / -75		
IDD0	OPERATING CURRENT: One Bank; Active-Precharge; t RC = t RC MIN; t CK = t CK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	ALL	100	85	mA	
IDD1	OPERATING CURRENT: One Bank; Active-Read-Precharge; Burst = 2; t RC = t RC MIN; CL = 2.5; t CK = t CK MIN; IOUT= 0mA; Address and control inputs changing once per clock cycle	x4	110	95		
		x8	120	100		
		x16	140	115		
IDD2P	PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; CKE ≤VIL (MAX); t CK = t CK MIN	ALL	10	6		
IDD2F	IDLE STANDBY CURRENT: /CS ≥ VIH (MIN); All banks idle; CKE ≥ VIH (MIN); t CK = t CK MIN; Address and other control inputs changing once per clock cycle	ALL	35	30		
IDD3P	ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; CKE ≤ VIL (MAX); t CK = t CK MIN	ALL	20	15		
IDD3N	ACTIVE STANDBY CURRENT: /CS ≥ VIH (MIN); CKE ≥ VIH (MIN); One bank; Active-Precharge; t RC = t RAS MAX; t CK = t CK MIN; DQ,DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	ALL	55	45		
IDD4R	OPERATING CURRENT: Burst = 2; Reads; Continuous burst;One bank active; Address and control inputs changing once per clock cycle;CL=2.5; t CK = t CK MIN; IOUT = 0 mA	x4	180	140		
		x8	190	150		
		x16	220	180		
IDD4W	OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL=2.5; t CK = t CK MIN;DQ, DM and DQS inputs changing twice per clock cycle	x4	180	130		
		x8	190	140		
		x16	220	160		
IDD5	AUTO REFRESH CURRENT: t RC = t RFC (MIN)	ALL	150	140		
IDD6	SELF REFRESH CURRENT: CKE ≤ 0.2V	-60/-75A/-75	3	3		9
		-60/-75A/-75 L	2	2		9,21
		-60/-75AU/-75 UL	1	1		9,22
IDD7	OPERATING CURRENT-Four bank Operation: Four bank are interleaved with BL=4, refer to the Notes 20	x4	270	215		20
		x8	290	235		20
		x16	330	270		20

AC OPERATING CONDITIONS AND CHARACTERISTICS

(TA=0 to 70°C, VDD = VDDQ = 2.5V ± 0.2V, VSS = VSSQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter / Test Conditions	Limits		Unit	Notes
		Min.	Max.		
VIH(AC)	High-Level Input Voltage (AC)	VREF + 0.31		V	
VIL(AC)	Low-Level Input Voltage (AC)		VREF - 0.31	V	
VID(AC)	Input Differential Voltage, CLK and /CLK	0.7	VDDQ + 0.6	V	7
VIX(AC)	Input Crossing Point Voltage, CLK and /CLK	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V	8
IOZ	Off-state Output Current /Q floating Vo=0 to VDDQ	-5	5	uA	
II	Input Current / VIN=0 to VDDQ	-2	2	uA	
IOH	Output High Current (VOUT = VTT+0.84V)	-16.8		mA	
IOL	Output High Current (VOUT = VTT-0.84V)	16.8		mA	

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AC TIMING REQUIREMENTS (1/2)

(TA=0 to 70°C, VDD = VDDQ = 2.5V ±0.2V, VSS = VSSQ = 0V, unless otherwise noted)

Symbol	AC Characteristics Parameter		-60		-75A		-75		Unit	Notes
			Min.	Max	Min.	Max	Min.	Max		
tAC	DQ Output Valid data delay time from CLK//CLK		-0.70	0.70	-0.75	0.75	-0.75	0.75	ns	
tDQSCK	DQ Output Valid data delay time from CLK//CLK		-0.60	0.60	-0.75	0.75	-0.75	0.75	ns	
tCH	CLK High level width		0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCL	CLK Low level width		0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCK	CLK cycle time	CL=2.5	6	15	7.5	15	7.5	15	ns	
		CL=2	7.5	15	7.5	15	10	15	ns	
tDS	Input Setup time (DQ,DM)		0.45		0.5		0.5		ns	26,27
tDH	Input Hold time(DQ,DM)		0.45		0.5		0.5		ns	26,27
tDIPW	DQ and DM input pulse width (for each input)		1.75		1.75		1.75		ns	
tHZ	Data-out-high impedance time from CLK//CLK		-0.70	0.70	-0.75	0.75	-0.75	0.75	ns	14
tLZ	Data-out-low impedance time from CLK//CLK		-0.70	0.70	-0.75	0.75	-0.75	0.75	ns	14
tDQSQ	DQ Valid data delay time from DQS			0.45		0.5		0.5	ns	
tHP	Clock half period		tCLmin or tCHmin		tCLmin or tCHmin		tCLmin or tCHmin		ns	
tQH	Output DQS valid window		tHP-tQHS		tHP-tQHS		tHP-tQHS		ns	
tQHS	Data Hold Skew Factor			0.55		0.75		0.75	tCK	
tDQSS	Write command to first DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25	tCK	
tDQSH	DQS input High level width		0.35		0.35		0.35		tCK	
tDQSL	DQS input Low level width		0.35		0.35		0.35		tCK	
tDSS	DQS falling edge to CLK setup time		0.2		0.2		0.2		tCK	
tDSH	DQS falling edge hold time from CLK		0.2		0.2		0.2		tCK	
tMRD	Mode Register Set command cycle time		12		15		15		ns	
tWPRES	Write preamble setup time		0		0		0		ns	16
tWPST	Write postamble		0.4	0.6	0.4	0.6	0.4	0.6	tCK	15
tWPRE	Write preamble		0.25		0.25		0.25		tCK	
tIH	Address and Control input hold time(fast slew rate)		0.75		0.9		0.9		ns	23,25
tIS	Address and Control input hold time(fast slew rate)		0.75		0.9		0.9		ns	23,25
tIH	Address and Control input hold time(Slow slew rate)		0.8		0.9		0.9		ns	24,25
tIS	Address and Control input hold time(Slow slew rate)		0.8		0.9		0.9		ns	24,25
tRPST	Read postamble		0.4	0.6	0.4	0.6	0.4	0.6	tCK	
tRPRE	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	tCK	

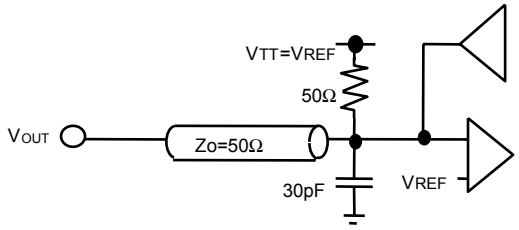
Not Product

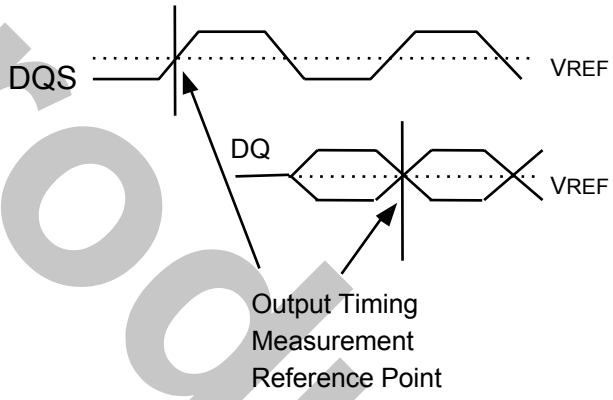
AC TIMING REQUIREMENTS (2/2)

(TA=0 to 70°C, VDD = VDDQ = 2.5V ±0.2V, VSS = VSSQ = 0V, unless otherwise noted)

Symbol	AC Characteristics Parameter	-60		-75A		-75		Unit	Notes
		Min.	Max	Min.	Max	Min.	Max		
tRAS	Row Active time	42	120,000	45	120,000	45	120,000	ns	
tRC	Row Cycle time(operation)	60		65		65		ns	
tRFC	Auto Ref. to Active/Auto Ref. command period	72		75		75		ns	
tRCD	Row to Column Delay	18		20		20		ns	
tRP	Row Precharge time	18		20		20		ns	
tRRD	Act to Act Delay time	12		15		15		ns	
tWR	Write Recovery time	15		15		15		ns	
tDAL	Auto Precharge write recovery + precharge time	35		35		35		ns	
tWTR	Internal Write to Read Command Delay	1		1		1		tCK	
tXSNR	Exit Self Ref. to non-Read command	75		75		75		ns	
tXSRD	Exit Self Ref. to -Read command	200		200		200		tCK	
tXPNR	Exit Power down to command	1		1		1		tCK	
tXPRD	Exit Power down to -Read command	1		1		1		tCK	18
tREFI	Average Periodic Refresh interval		7.8		7.8		7.8	us	17

Output Load Condition





CAPACITANCE

(TA=0 to 70°C, VDD = VDDQ = 2.5V ± 0.2V, VSS = VSSQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Delta Cap.(Max.)	Unit	Notes
			Min.	Max.			
CI(A)	Input Capacitance, address pin	VI=1.25v	2.0	3.0	0.50	pF	11
CI(C)	Input Capacitance, control pin	f=100MHz	2.0	3.0		pF	11
CI(K)	Input Capacitance, CLK pin	VI=25mVrms	2.0	3.0	0.25	pF	11
CI/O	I/O Capacitance, I/O, DQS, DM pin		4.0	5.0	0.50	pF	11

Not product

Note:

1. All voltages are referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics, may be conducted at nominal reference/supply voltage levels. However, the specifications and device operations are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use the VIL to VIH swing of up to 1.5V in the test environment. Input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed $\pm$2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized.
11. This parameter is sampled. VDDQ = 2.5V$\pm$0.2V, VDD = 2.5V $\pm$ 0.2V , f = 100 MHz, TA = 25^{o}C, VOUT(DC) = VDDQ/2, VOUT(PEAK TO PEAK) = 25mV. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
12. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE$\leq$ 0.3VDDQ is recognized as LOW.
14. t HZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and satisfies the input slew rate specifications. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
17. A maximum of eight AUTO REFRESH commands can be asserted to any given DDR SDRAM device.
18. tXPRD should be 200 tCLK when the clocks are unstable during the power down mode.
19. (no data : deleted 10/'02)

(Notes continued on next page)

Not Product

Note (Continued) :

20. IDD7 : Operating current is measured under the conditions
    (1).Four Bank are being interleaved with tRC(min),burst mode,address and control inputs on NOP edge are not changing.Iout = 0mA
    (2).Timing Patterns
    -DDR266B(-75) (133MHz,CL=2.5) : tCK=7.5ns, CL=2.5, BL=4, tRRD=2*tCK, tRCD=3*tCK,
    Setup:A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
    Read :A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 -repeat the same timing with random address changing 50% of data changing at every transfer

    -DDR266A(-75A) (133MHz,CL=2) : tCK=7.5ns, CL=2, BL=4, tRRD=2*tCK, tRCD=3*tCK,
    Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
    Read : A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 -repeat the same timing with random address changing 50% of data changing at every transfer

    -DDR333B(-60) (166MHz,CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRRD=2*tCK, tRCD=3*tCK,
    Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
    Read : A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 -repeat the same timing with random address changing 50% of data changing at every transfer
    *Legend: A=Active,R=Read, RA=Read with Autoprecharge ,P=Precharge, N=DESELECT

21. Low Power Version (-60L/-75AL/-75L)
22. Ultra Low Power Version (-60UL/-75AU/-75UL)
23. For command/address and CK & /CK slew rate > 1.0V/ns.
24. For command/address and CK & /CK slew rate > 0.5V/ns
25. Input Setup & Hold Time Derating for Slew Rate

Input slew Rate	ΔtIS	ΔtIH	Unit
0.5V/ns	0	0	ps
0.4V/ns	+50	+50	ps
0.3V/ns	+100	+100	ps

This derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns.The input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

26. I/O Setup & Hold Time Derating for Slew Rate

I/O Input slew Rate	ΔtDS	ΔtDH	Unit
0.5V/ns	0	0	ps
0.4V/ns	+75	+75	ps
0.3V/ns	+150	+150	ps

This derating factor will be used to increase tDS and tDH in the case where the I/O slew rate is below 0.5V/ns.The I/O slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The I/O slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

(Notes continued on next page)

E0F product

Note (Continued) :

27. I/O Setup & Hold Time Derating for Rise/Fall Delta Slew Rate

Delta slew Rate	∆tDS	∆tDH	Unit
±0.0ns/V	0	0	ps
±0.25ns/V	+50	+50	ps
±0.5ns/V	+100	+100	ps

This derating table is used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ. The delta Rise/Fall Rate is calculated as;

{1/(Slew Rate1)} - {1/(Slew Rate2)}

For example:

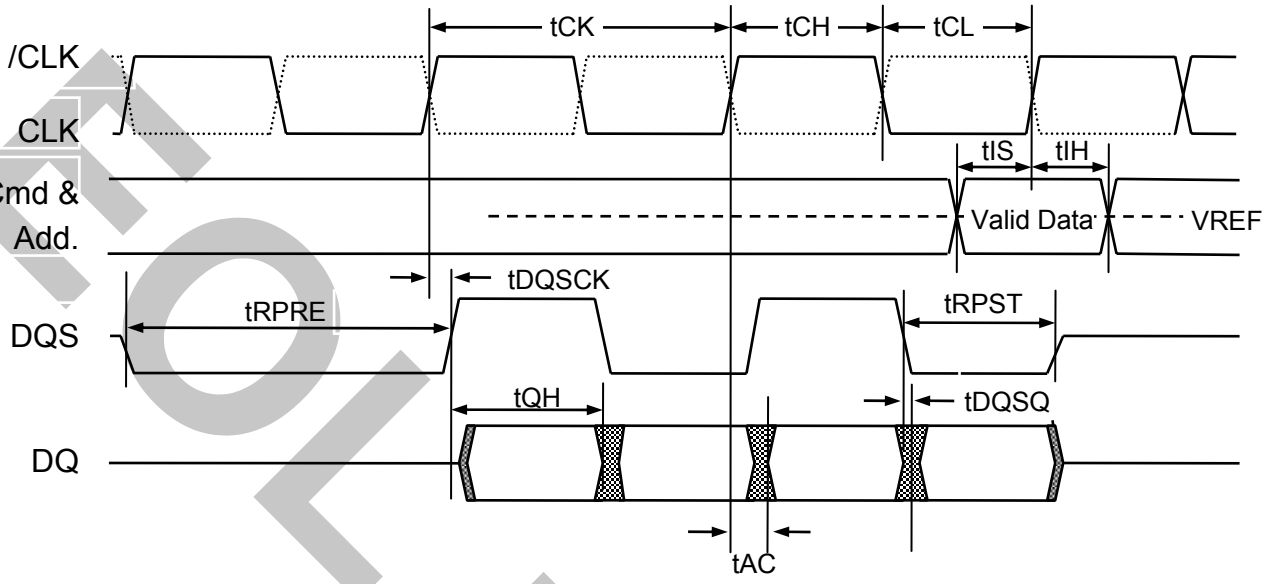
If Slew Rate1 is 0.5V/ns and Slew Rate2 is 0.4V/ns, then delta Rise/Fall Rate = - 0.5V/ns.

Using the table given, this would result in the need for an increase in tDS and tDH for 100ps.

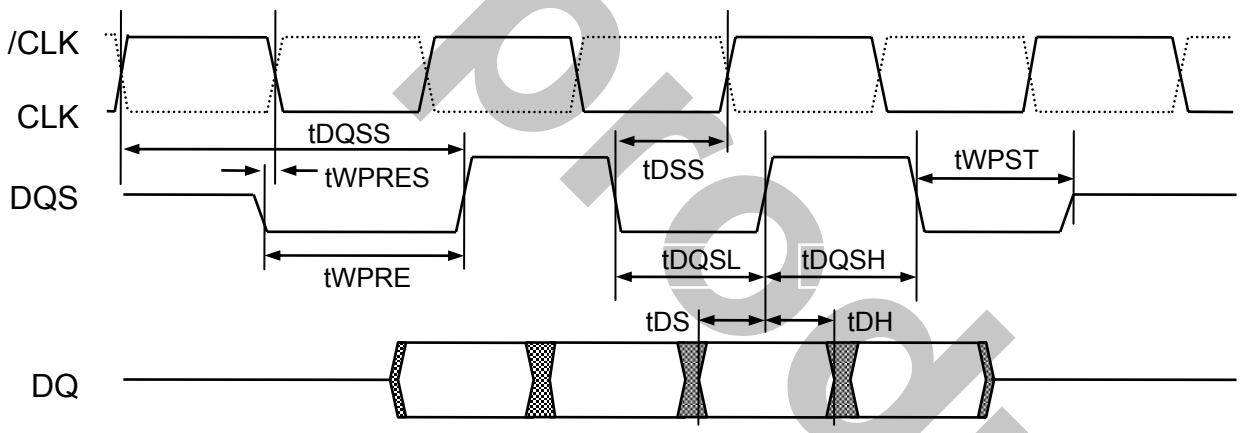
EOL product

TIMING CHART

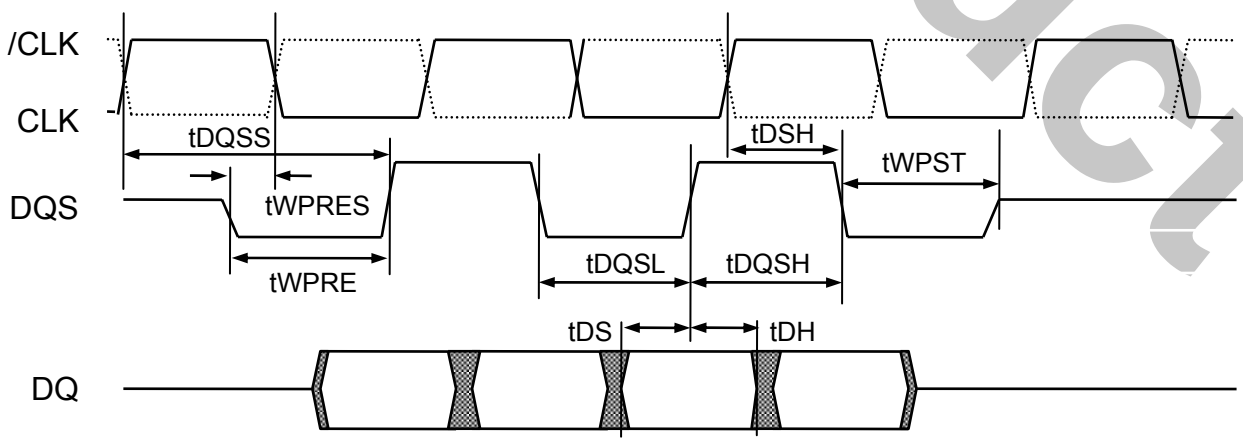
Read Operation



Write Operation / tDQSS=max.



Write Operation / tDQSS=min.



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OPERATIONAL DESCRIPTION

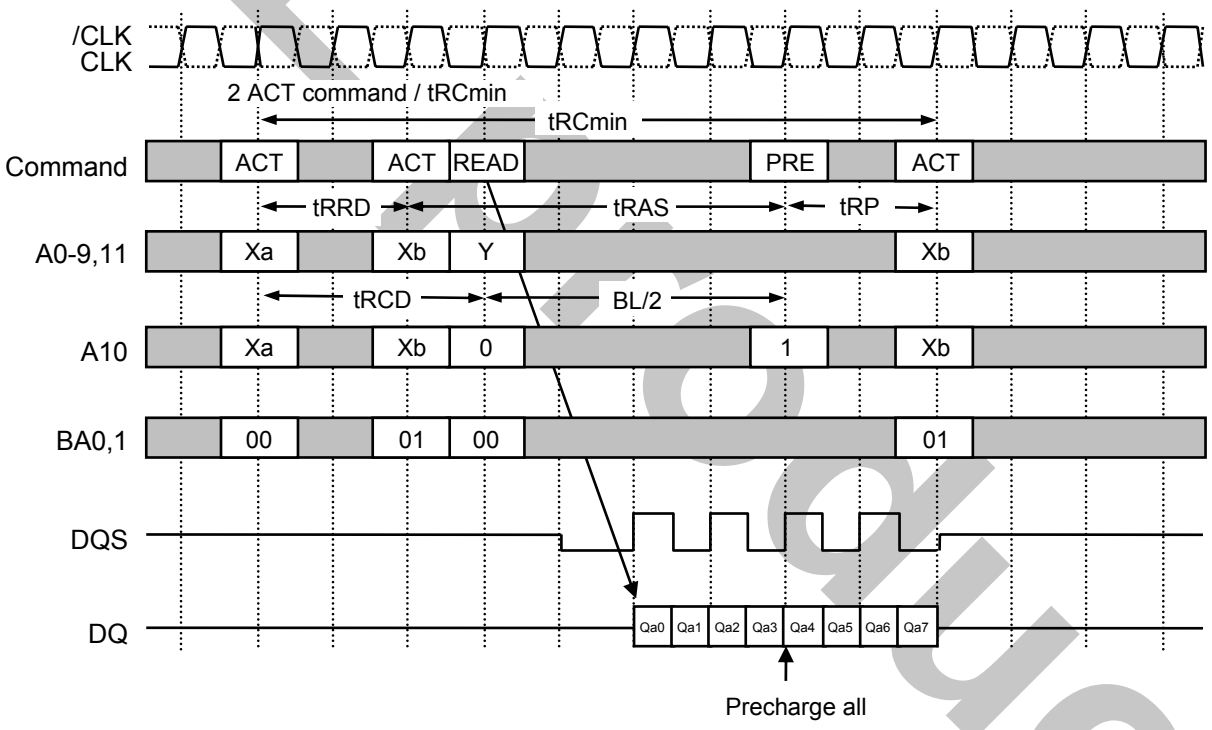
BANK ACTIVATE (ACT)

The DDR SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row address A12-0. The minimum activation interval between banks is tRRD.

PRECHARGE (PRE)

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA,PRE+A10=H) is available to deactivate all banks at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.

Bank Activation and Precharge All (BL=8, CL=2)



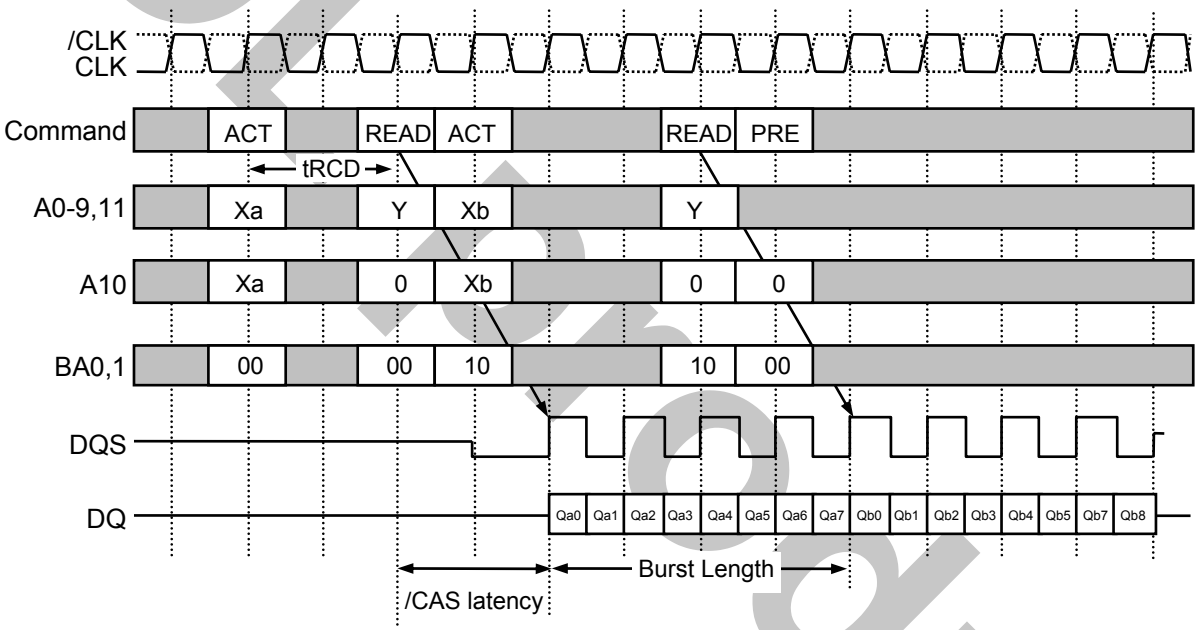
A precharge command can be issued after BL/2 time from a read command.

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READ

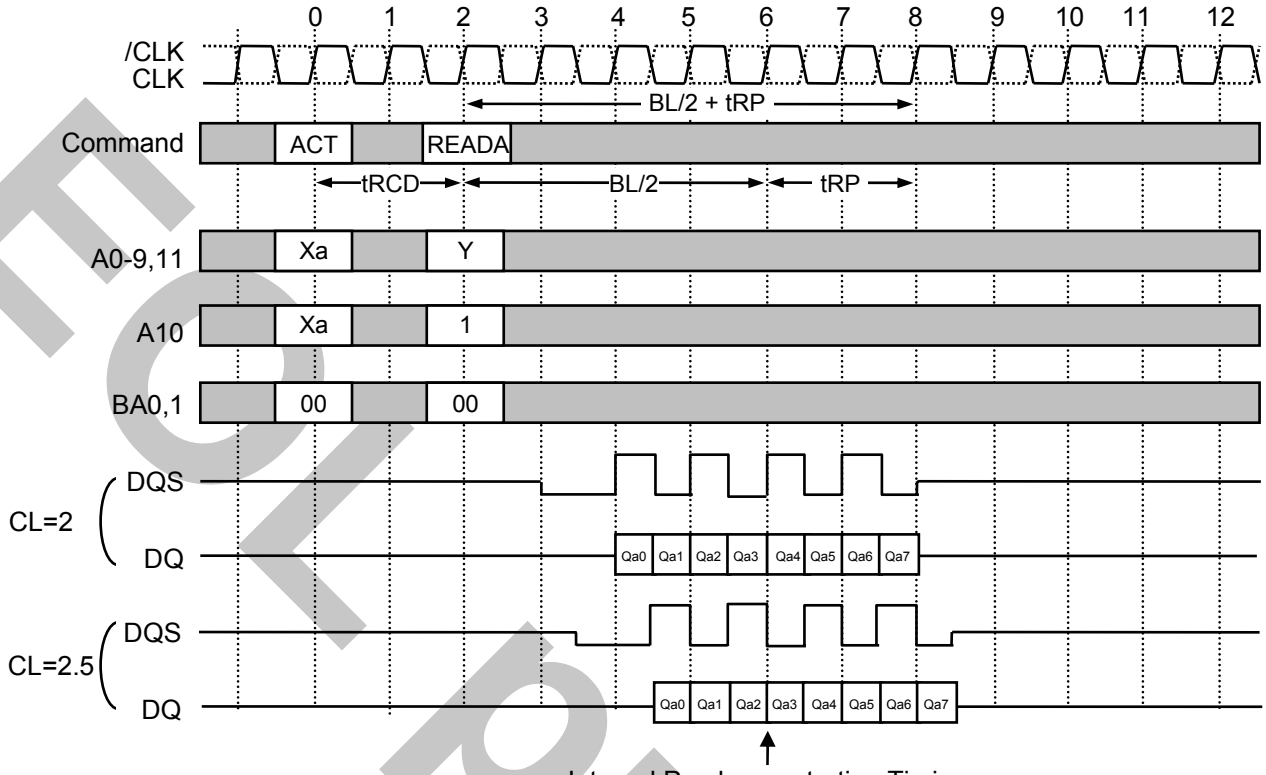
After tRCD from the bank activation, a READ command can be issued. 1st Output data is available after the /CAS Latency from the READ, followed by (BL-1) consecutive data. (BL : Burst Length) The start address is specified by A11,A9-A0(x4)/A9-A0(x8)/A8-A0(x16), and the address sequence of burst data is defined by the Burst Type. A READ command may be issued to any active bank, so the row precharge time (tRP) can be hidden during the continuous burst data by interleaving the multiple banks. When A10 is high in READ command, the auto-precharge (READA) is performed. Any command (READ,WRITE,PRE,ACT) asserted to the same bank is inhibited till the internal precharge is completed. The internal precharge operation starts at BL/2 time after READA command. The next ACT command can be issued after (BL/2+tRP) time from the previous READA.

Multi Bank Interleaving READ (BL=8, CL=2)



Not Product

READ with Auto-Precharge (BL=8, CL=2,2.5)



Asserted Command	For Different Bank							
	3	4	5	6	7	8	9	10
READ	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal
READA	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal
WRITE(CL=2)	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal
WRITE(CL=2.5)	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
WRITEA(CL=2)	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal
WRITEA(CL=2.5)	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
ACT	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal
PCG	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal

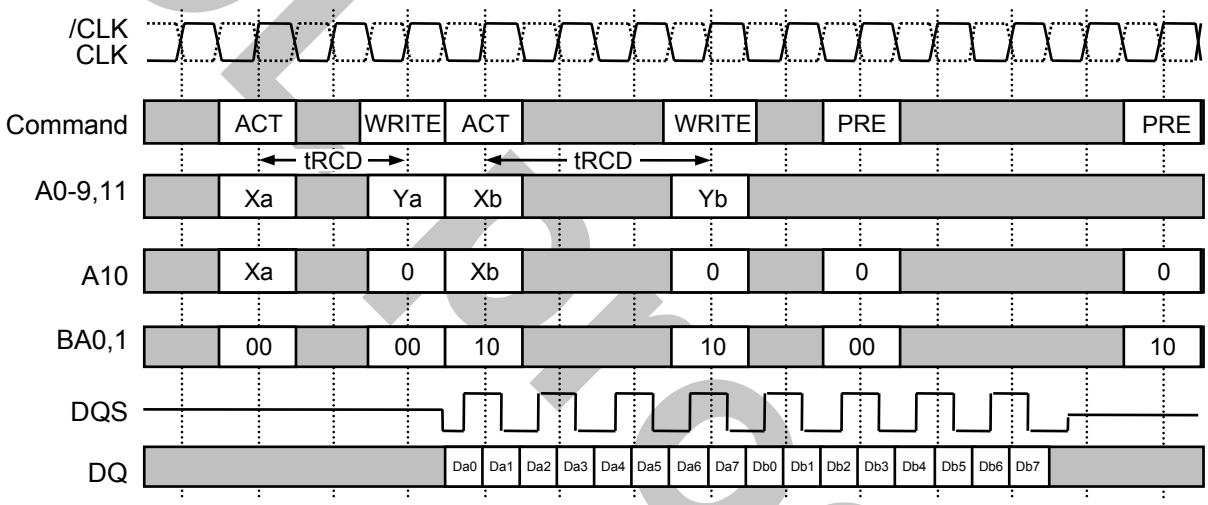
Operating description when new command is asserted.

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WRITE

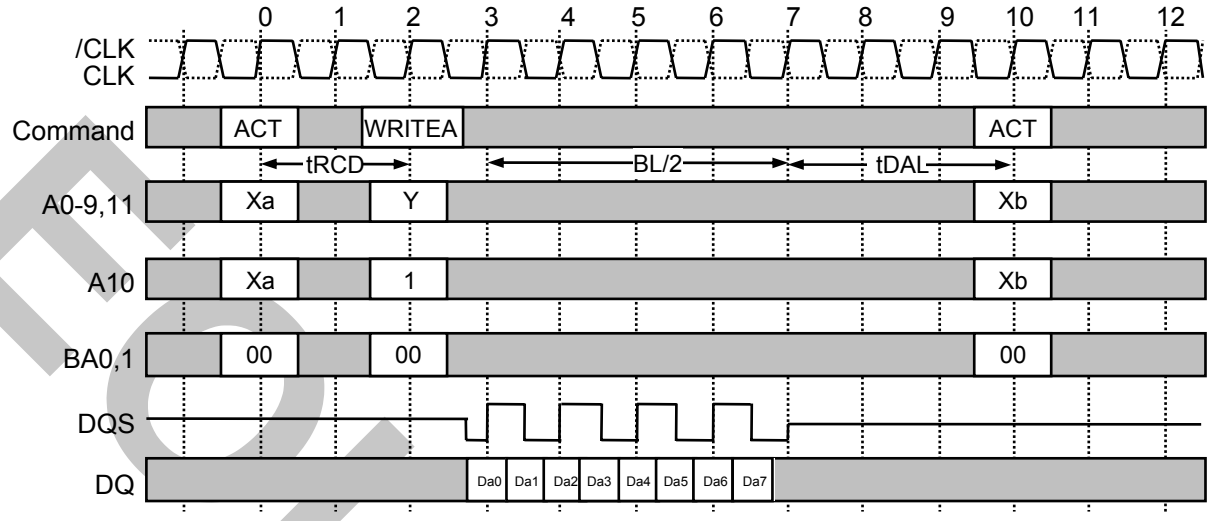
After tRCD time from the bank activation, a WRITE command can be issued. 1st input data is sampled at the WRITE command with data strobe input, followed by (BL-1) data being written into RAM.The Burst Length is BL. The start address is specified by A11,A9-A0(x4)/A9-A0(x8)/A8-A0(x16), and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden during the continuous input data by interleaving the multiple banks. The write recovery time (tWR) is required from the last written data to the next PRE command. When A10 is high in a WRITE command, the auto-precharge(WRITEA) is performed. Any command (READ,WRITE,PRE,ACT) asserted to the same bank is inhibited till the internal precharge operation is completed. The next ACT command can be issued after tDAL from the last input data cycle.

Multi Bank Interleaving WRITE (BL=8)



Not Product

WRITE with Auto-Precharge (BL=8)



Asserted Command	For Different Bank							
	3	4	5	6	7	8	9	10
READ	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal
READA	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal
WRITE	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal
WRITEA	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal
ACT	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal
PCG	Legal	Legal	Legal	Legal	Legal	Legal	Legal	Legal

Operating description when new command is asserted.

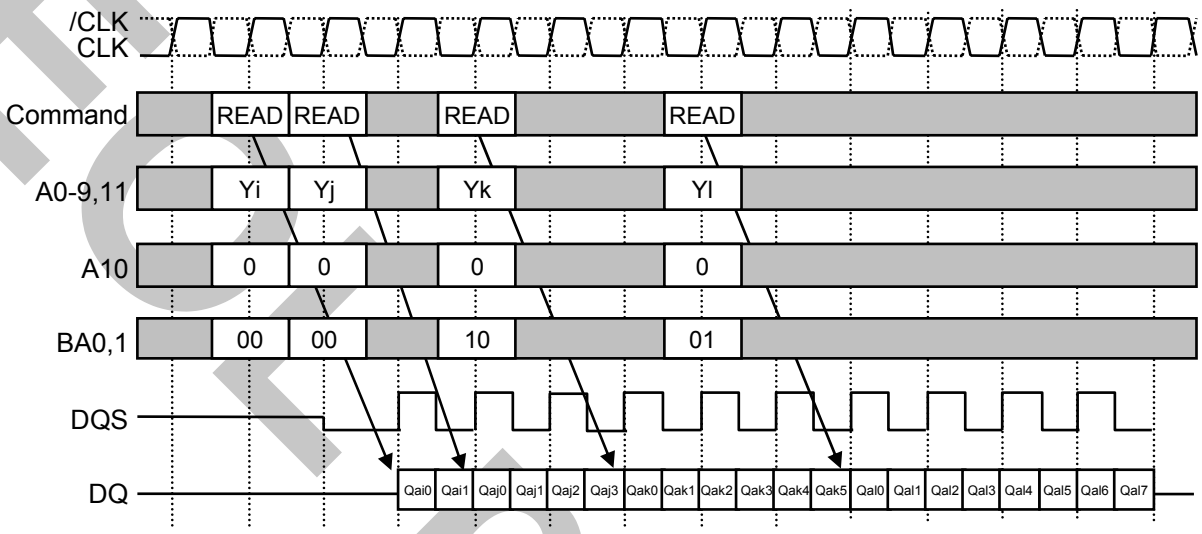
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BURST INTERRUPTION

[Read Interrupted by Read]

Burst read operation can be interrupted by the new Read command issued to any other bank. Random column access is allowed. READ to READ interval is 1CLK as the minimum.

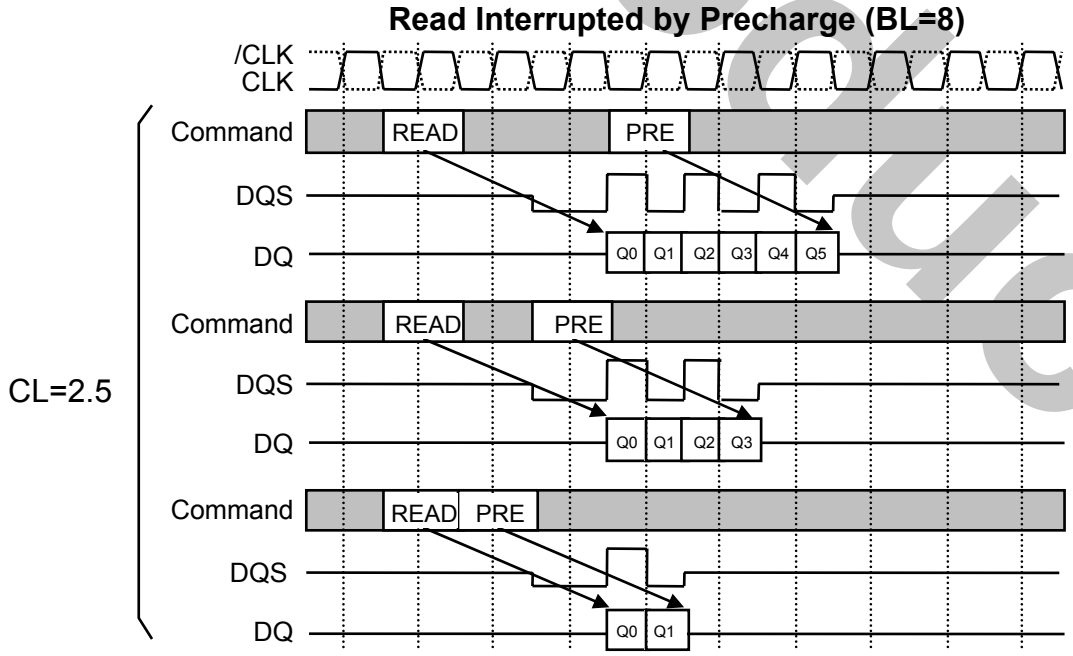
Read Interrupted by Read (BL=8, CL=2)



[Read Interrupted by precharge]

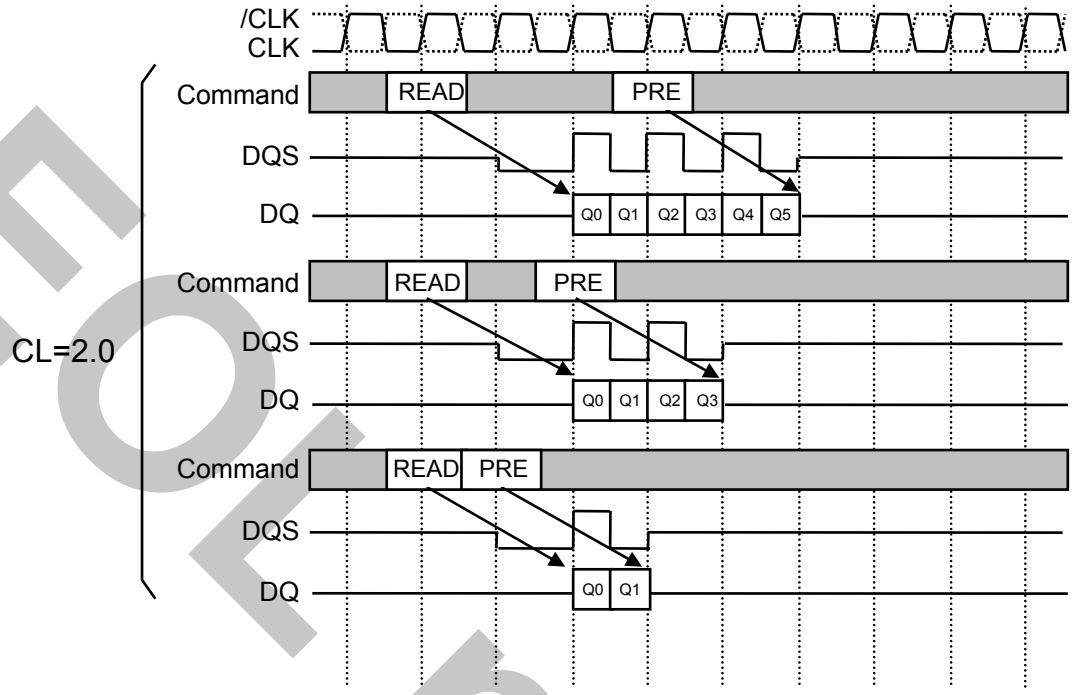
Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is 1 CLK minimum. The time between PRE command to output disable is equal to the CAS Latency. As a result, READ to PRE interval determines valid data length to be outputted. The figure below shows the examples of BL=8.

Read Interrupted by Precharge (BL=8)



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Read Interrupted by Precharge (BL=8)



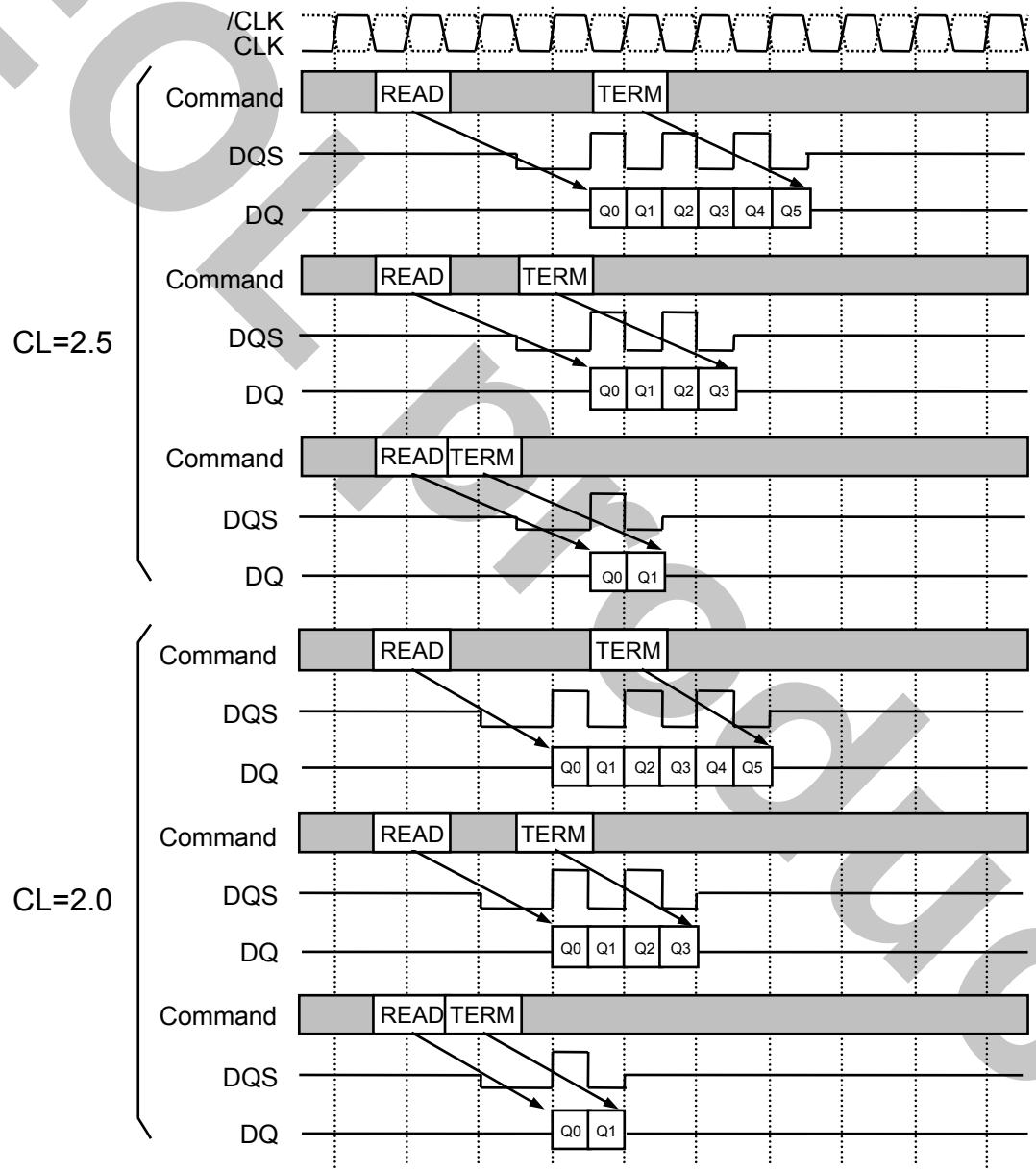
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[Read Interrupted by Burst Stop]

Burst read operation can be interrupted by a burst stop command(TERM). READ to TERM interval is 1 CLK minimum. The time between TERM command to output disable is equal to the CAS Latency. As a result, READ to TERM interval determines valid data length to be outputted. The figure below shows example of BL=8.

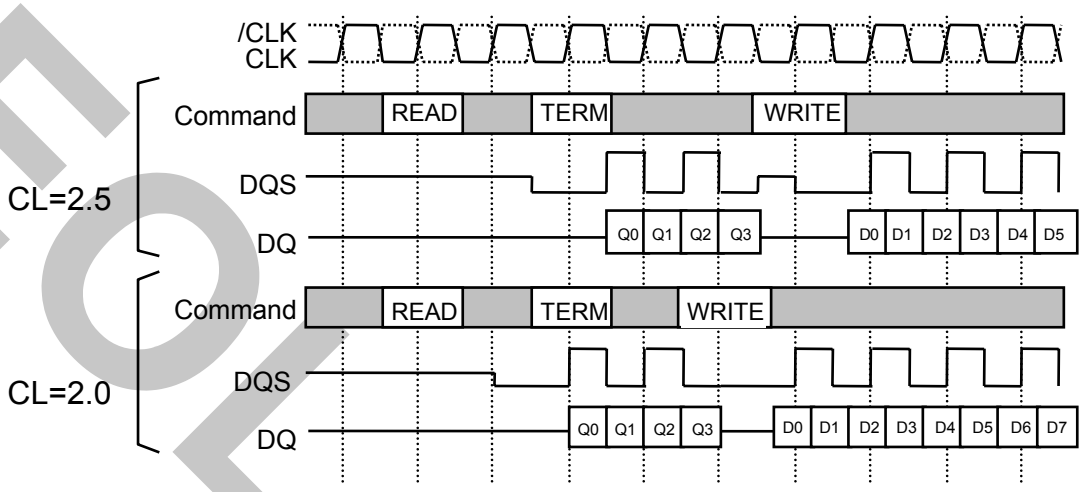
EOL Product

Read Interrupted by TERM (BL=8)



[Read Interrupted by Write with TERM]

Read Interrupted by TERM (BL=8)

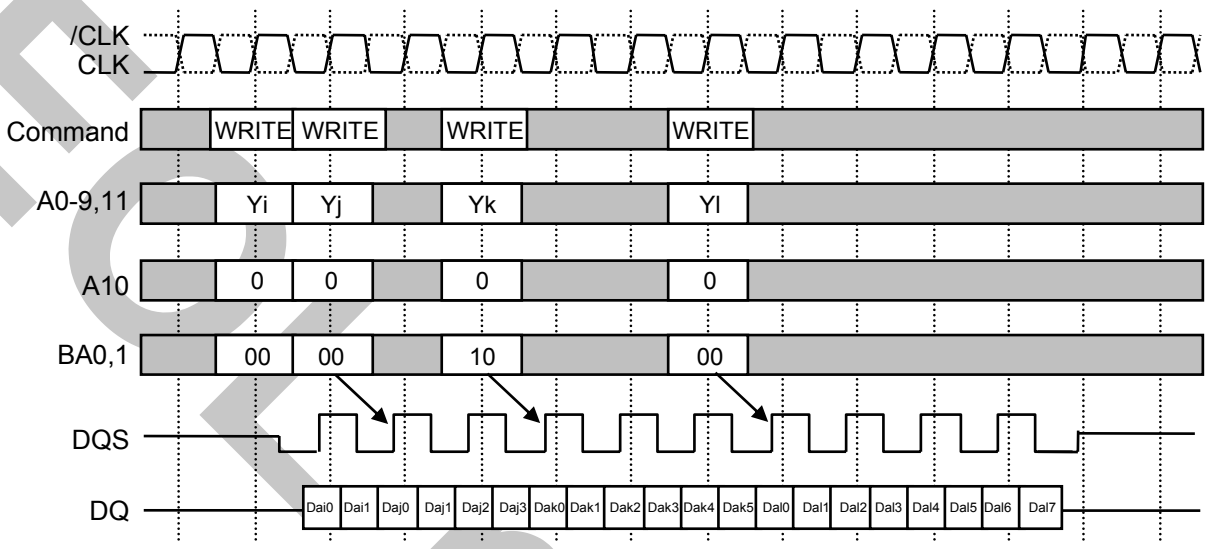


EOL product

[Write interrupted by Write]

Burst write operation can be interrupted by Write to any bank. Random column access is allowed. WRITE to WRITE interval is 1 CLK minimum.

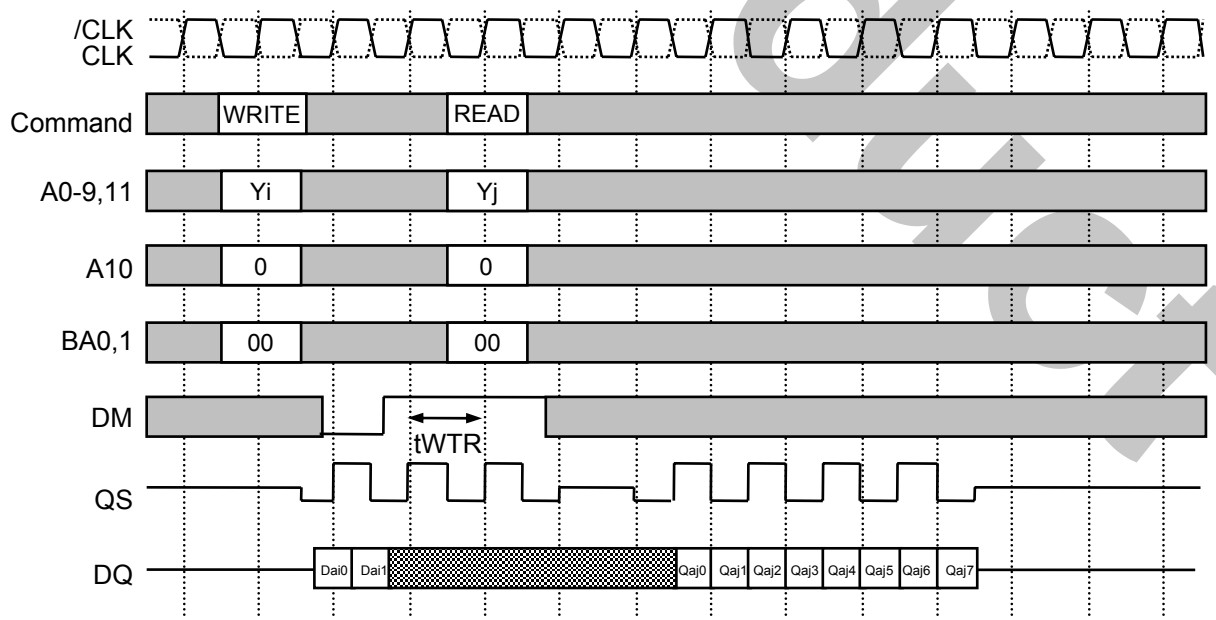
Write Interrupted by Write (BL=8)



[Write interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. Internal WRITE to READ command interval(tWTR) is 1 CLK minimum. The input data masked by DM in the interrupted READ cycle is "don't care". tWTR is referenced from the first positive edge after the last data input.

Write Interrupted by Read (BL=8, CL=2.5)

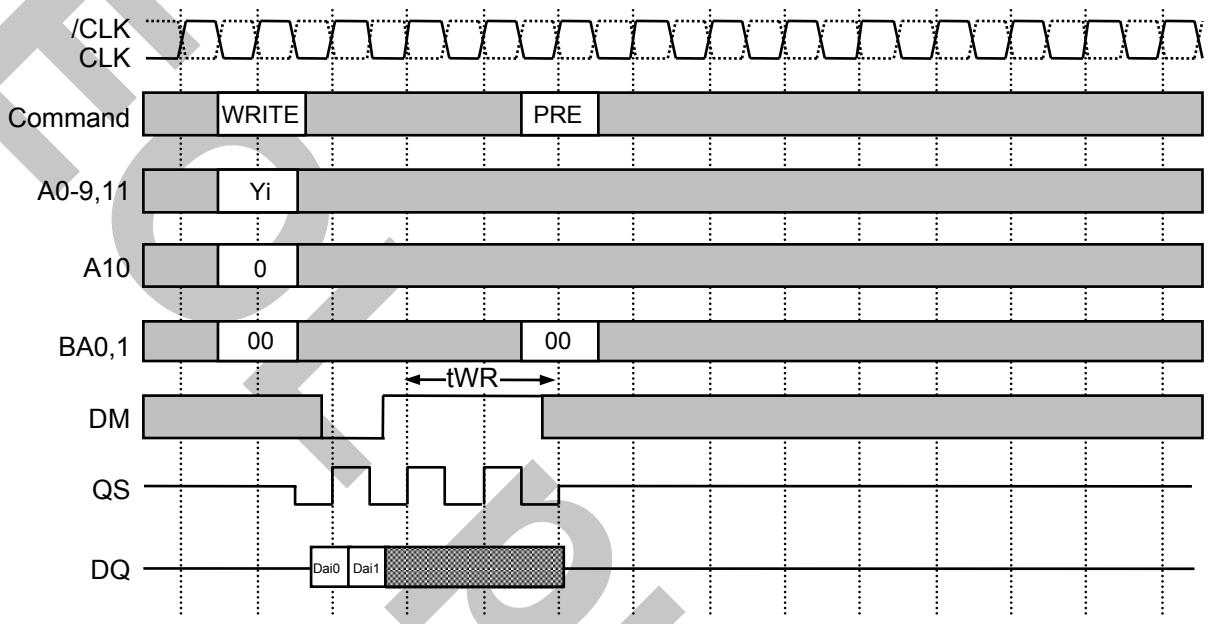


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[Write interrupted by Precharge]

Burst write operation can be interrupted by precharge of the same or all bank. Random column access is allowed. tWR is referenced from the first positive CLK edge after the last data input.

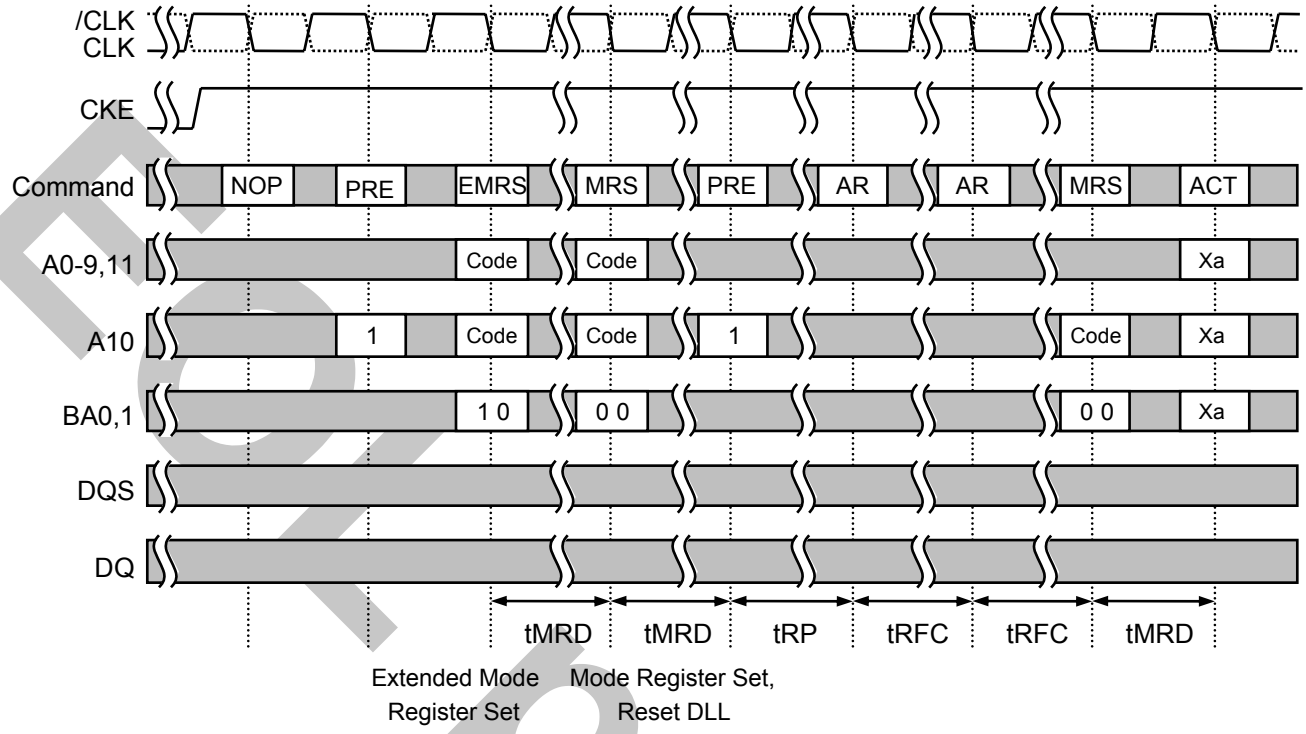
Write Interrupted by Precharge (BL=8, CL=2.5)



Ecl-product

[Initialize and Mode Register sets]

Initialize and MRS



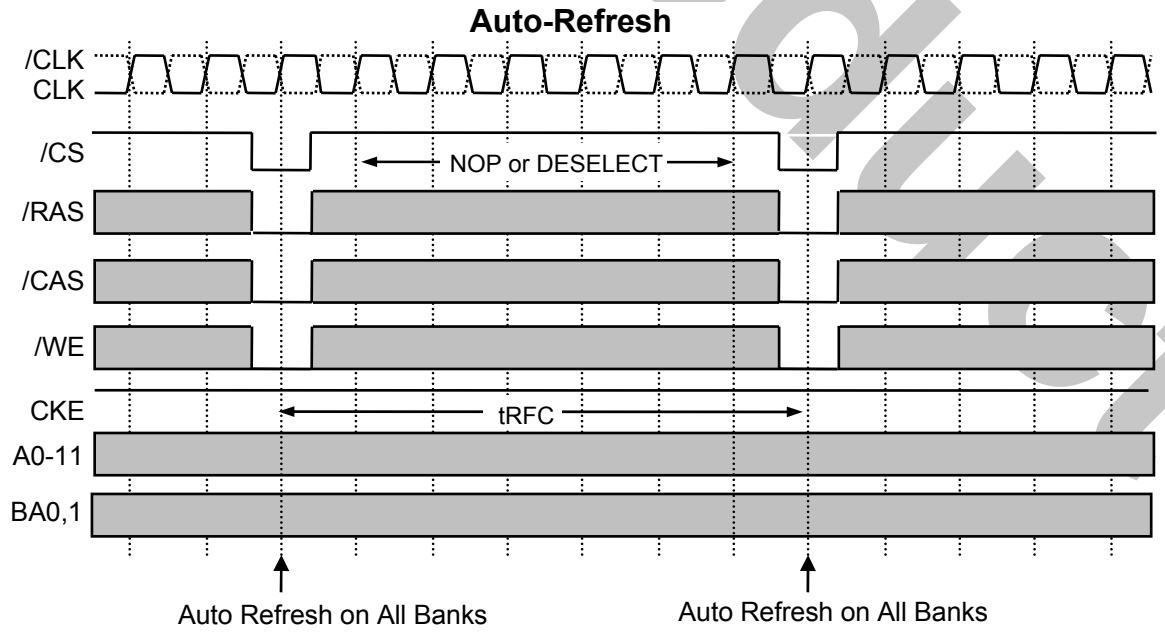
[AUTO REFRESH]

Auto-refresh cycle is initiated with a REFA(/CS=/RAS=/CAS=L,/WE=CKE=H) command.

The refresh address is generated internally. 8192 REFA cycles within 64ms refresh

256 Mbits memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto refresh, all banks must be in the idle state. The minimum internal between auto-refresh is tRFC . No command is allowed within tRFC time after the REFA command.

Auto-Refresh



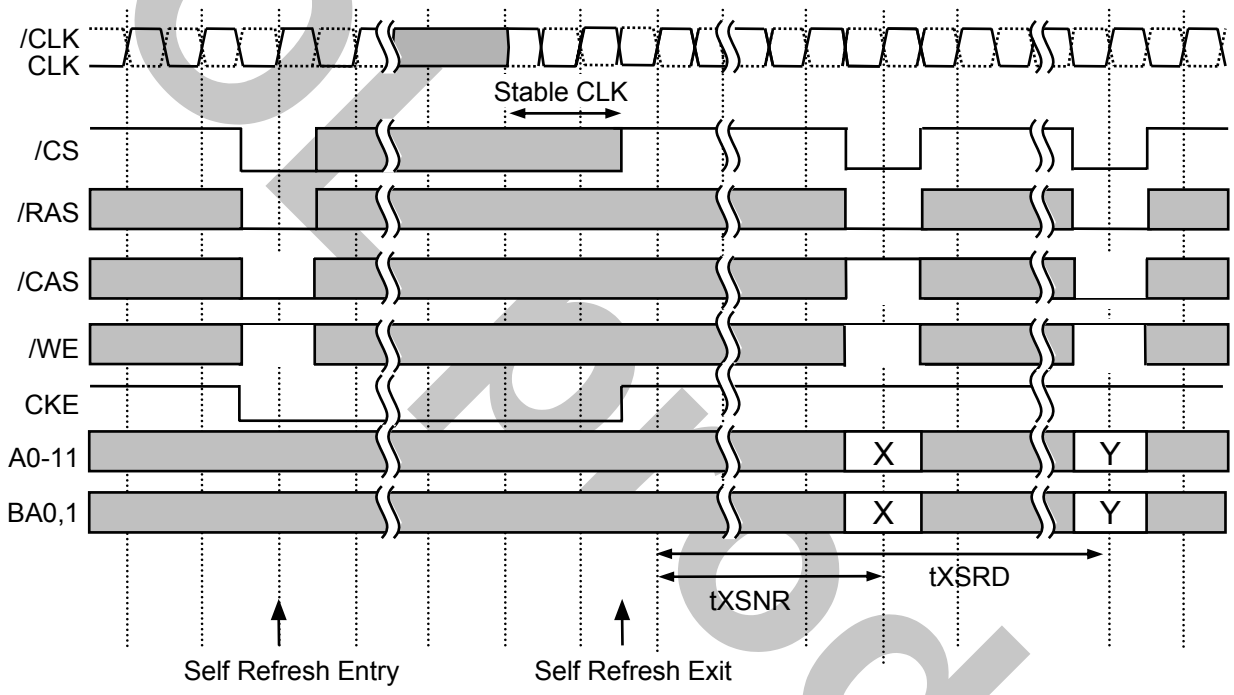
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[SELF REFRESH]

Self -refresh mode is entered by asserting a REFS command (/CS=/RAS=/CAS=L,/WE=H,CKE=L). The self-refresh mode is maintained as long as CKE is kept low. During the self-refresh mode, CKE becomes asynchronous and the only enable input. All other inputs including CLK are disabled and ignored to save the power consumption. In order to exit the self-refresh mode, the device shall be supplied the stable CLK inputs, followed by DESEL or NOP command, then asserting CKE for the period longer than tXSNR/tXSRD.

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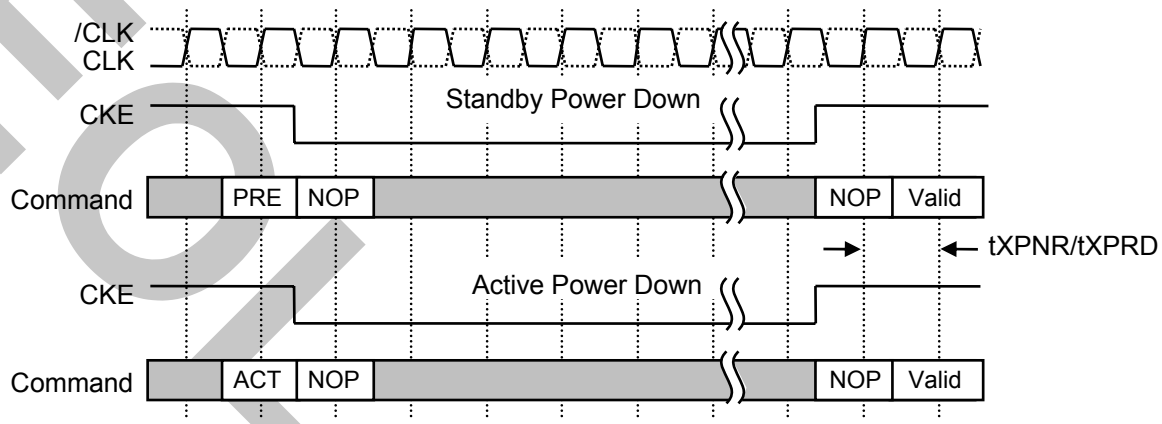
Self-Refresh



[Power DOWN]

The purpose of CLK suspend is power down. CKE is synchronous input except during the self-refresh mode. A commands are ignored. From CKE=H to normal function, DLL recovery time is NOT required when the stable CLK is supplied during the power down mode.

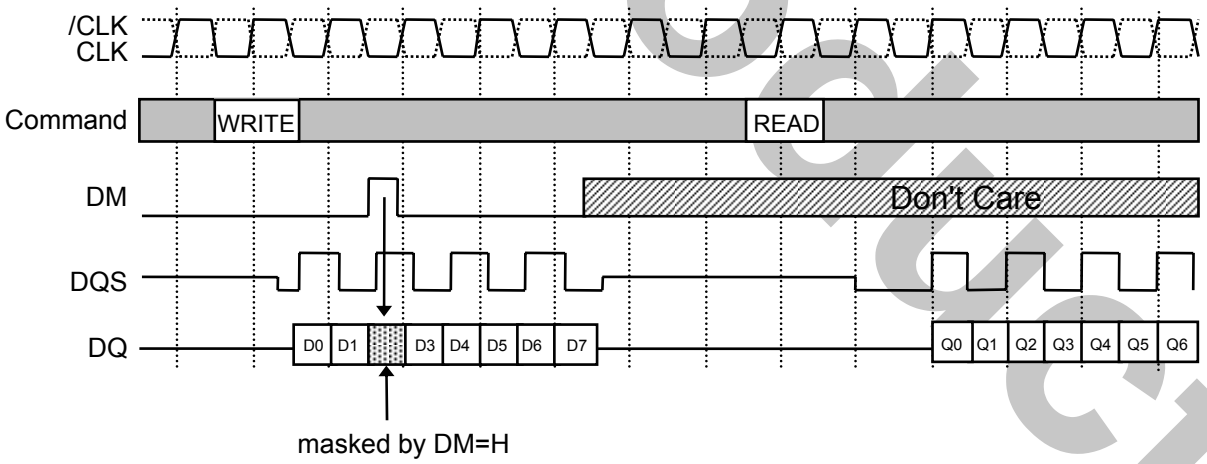
Power Down by CKE



[DM CONTROL]

DM is defined as the data mask for write data. During writes, DM masks the input data cycle by cycle. Latency of DM to write mask is 0.

DM Function(BL=8,CL=2)



Eol product

EOL Product

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

EO PROJECT

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[Product applications]
Elpida Memory, Inc. makes every attempt to ensure that its products are of high quality and reliability. However, users are instructed to contact Elpida Memory's sales office before using the product in aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment, medical equipment for life support, or other such application in which especially high quality and reliability is demanded or where its failure or malfunction may directly threaten human life or cause risk of bodily injury.

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