Ultralow Power +3.3 V, RS-232 Notebook PC Serial Port Drivers/Receivers

ADM560/ADM561

FEATURES

RS-232 compatible
Operates with 3 V or 5 V logic
Ultralow power CMOS: 1.3 mA operation
Low power shutdown: 0.2 µA
Suitable for serial port mice
116 kbps data rate
1 µF charge pump capacitors
Single +3 V to +3.6 V power supply
Two receivers active in shutdown (ADM560)

APPLICATIONS

Notebook computers
Peripherals
Modems
Printers
Battery-operated equipment

FUNCTIONAL BLOCK DIAGRAM

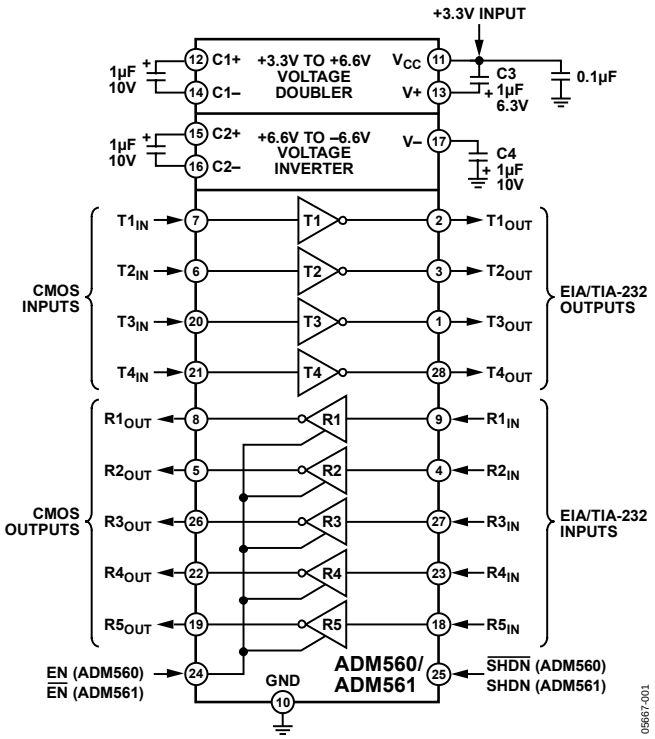

Figure 1.

GENERAL DESCRIPTION

The ADM560/ADM561 are four driver/five receiver interface devices designed to meet the EIA-232 standard and operate with a single +3.3 V power supply. The devices feature an on-board dc-to-dc converter, eliminating the need for dual ±5 V power supplies. This dc-to-dc converter contains a voltage doubler and voltage inverter, both of which internally generate ±6.6 V from the input +3.3 V power supply.

The ADM560 and the ADM561 consume only 5 mW making them ideally suited for battery and other power-sensitive applications. A shutdown facility is also provided to reduce the power to 0.66 µW.

The ADM560 contains active low shutdown and an active high receiver enable signal. In shutdown mode, two receivers remain active, thereby allowing monitoring of peripheral devices. This feature allows the device to be shut down until a peripheral device begins communication. The active receivers alert the processor, and then take the ADM560 out of shutdown mode.

The ADM561 features active high shutdown and an active low receiver enable. In this device, all receivers are disabled in shutdown.

The ADM560/ADM561 are fabricated using CMOS technology for minimal power consumption. They feature a high level of over-voltage protection and latch-up immunity. The receiver inputs can withstand up to ±25 V levels. The transmitter inputs can be driven from either 3 V or 5 V logic levels. This allows operation in mixed 3 V/5 V power supply systems.

The ADM560/ADM561 are packaged in a 28-lead SOIC and a 28-lead SSOP package.

Rev. B
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REVISION HISTORY

9/06—Rev. A to Rev. B

Updated Format ..... Universal
Changes to Specifications 3

10/05—Rev. 0 to Rev. A

Updated Format ..... Universal
Changes to Specifications 3
Update to Outline Dimensions 9
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7/94—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = +3.3 V ± 10%, C1 to C4 = 1 µF, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Swing	±5.0	±5.5		V	V_{CC} = 3.3 V, three transmitter outputs loaded with 3 kΩ to ground
	±4	±4.5		V	V_{CC} = 3.0 V, all transmitter outputs, loaded with 3 kΩ to ground
V_{CC} Power Supply Current		3.5	5	mA	No load, $T_{IN} = V_{CC}$
		3.5	5	mA	No load, T_{IN} = GND
Shutdown Supply Current		0.2	5	µA	$\overline{SHDN}$ = GND (ADM560), SHDN = V_{CC} (ADM561), $T_{IN} = V_{CC}$
Input Logic Threshold Low, V_{INL}			0.4	V	T_{IN}, EN, $\overline{EN}$, SHDN, $\overline{SHDN}$
Input Logic Threshold High, V_{INH}	2.4			V	T_{IN}, EN, $\overline{EN}$, SHDN, $\overline{SHDN}$
Logic Pull-Up Current		3	20	µA	T_{IN} = GND
EIA-232 Input Voltage Range	−25		+25	V	
EIA-232 Input Threshold Low	0.4	0.8		V	
EIA-232 Input Threshold High		1.1	2.4	V	
EIA-232 Input Hysteresis		0.3		V	
EIA-232 Input Resistance	3	5	7	kΩ	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
CMOS Output Voltage High, V_{OH}	2.8			V	I_{OUT} = −40 mA
CMOS Output Leakage Current		+0.05	±5	µA	$\overline{EN} = V_{CC}$, EN = GND, 0 V ≤ $R_{OUT} \leq V_{CC}$
Output Enable Time		100		ns	
Output Disable Time		50		ns	
Receiver Propagation Delay					
TPHL		0.1	1	µs	
TPLH		0.5	2	µs	
Transition Region Slew Rate		4.5		V/µs	R_L = 3 kΩ, C_L = 2500 pF measured from +3 V to −3 V or −3 V to +3 V
Transmitter Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short-Circuit Current		±10		mA	

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
V+	(V_{CC} − 0.3 V) to +14 V
V−	+0.3 V to −14 V
Input Voltages	
T_{IN}	−0.3 V to (V+, +0.3 V)
R_{IN}	25 V
Output Voltages	
T_{OUT}	(V+, +0.3 V) to (V−, −0.3 V)
R_{OUT}	−0.3 V to (V_{CC} + 0.3 V)
Short-Circuit Duration	
T_{OUT}	Continuous
Power Dissipation	
SSOP	900 mW
SOIC	900 mW
Operating Temperature Range	
Commercial (J Version)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
ESD Rating	>2000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

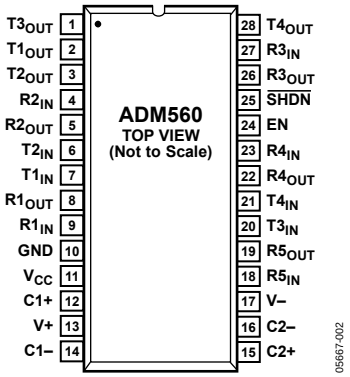


Figure 2.ADM560 Pin Configuration

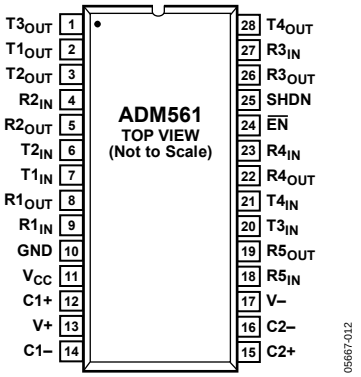


Figure 3. ADM561 Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
2, 3, 1, 28	$T1_{OUT}$ to $T4_{OUT}$	Transmitter (Driver) Outputs. Typically ±6 V.
9, 4, 27, 23, 18	$R1_{IN}$ to $R5_{IN}$	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each of these inputs.
8, 5, 26, 22, 19	$R1_{OUT}$ to $R5_{OUT}$	Receiver Outputs. These are 3 V logic levels.
7, 6, 20, 21	$T1_{IN}$ to $T4_{IN}$	Transmitter (Driver) Inputs. These inputs accept 3 V or 5 V logic levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
10	GND	Ground Pin. Must be connected to 0 V.
11	V_{CC}	Power Supply Input 3.3 V ± 10%.
12, 14	C1+, C1−	External Capacitor 1 is connected between these pins.
13	V+	Internally Generated Positive Supply. +6.6 V nominal.
15, 16	C2+, C2−	External Capacitor 2 is connected between these pins.
17	V−	Internally Generated Negative Supply. −6.6 V nominal.
24	EN/$\overline{EN}$	Receiver Enable. EN, active high on ADM560. $\overline{EN}$, active low on ADM561. Refer to Table 4.
25	$\overline{SHDN}$/SHDN	Shutdown Control. $\overline{SHDN}$, active low on ADM560. SHDN, active high on ADM561. Refer to Table 4.

Table 4. ADM560/ADM561 Enable and Shutdown Control

	ADM560	ADM561
Normal Operation	$\overline{SHDN}$ = 1	SHDN = 0
	EN = 1; receivers active	$\overline{EN}$ = 0; receivers active
	EN = 0; receivers inactive	$\overline{EN}$ = 1; receivers inactive
Shutdown Mode	$\overline{SHDN}$ = 0	SHDN = 1
	EN = 1; Receiver R1 to Receiver R3 inactive	$\overline{EN}$ = 0; receivers inactive
	EN = 1; Receiver R4 and Receiver R5 active	$\overline{EN}$ = 1; receivers inactive
	EN = 0; Receiver R1 to Receiver R5 inactive	

TYPICAL PERFORMANCE CHARACTERISTICS

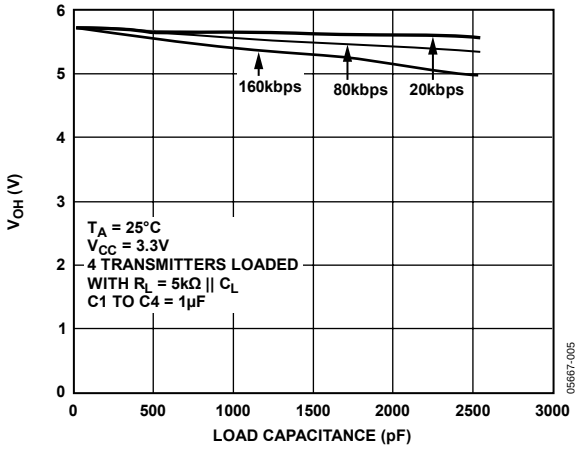


Figure 4. Transmitter Output Voltage High vs. Load Capacitance

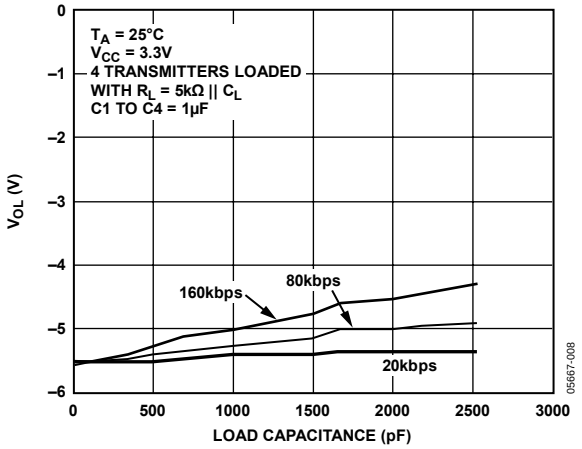


Figure 7. Transmitter Output Voltage Low vs. Load Capacitance

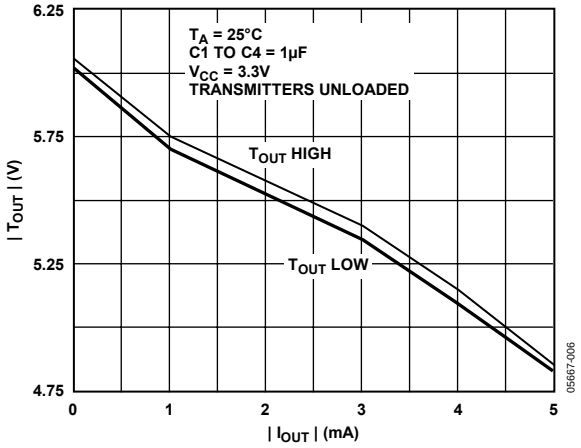


Figure 5. Transmitter Output Voltage vs. Load Current

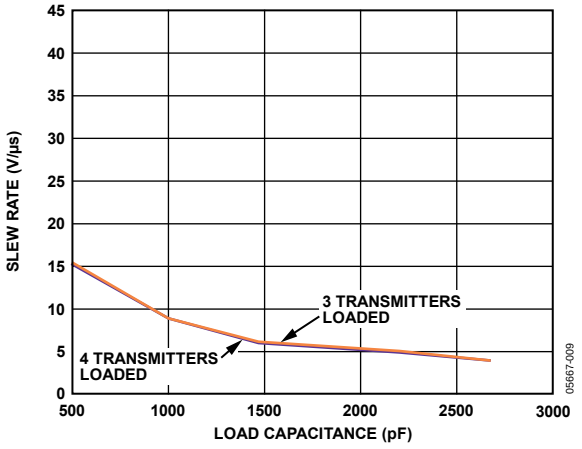


Figure 8. Transmitter Slew Rate vs. Load Capacitance

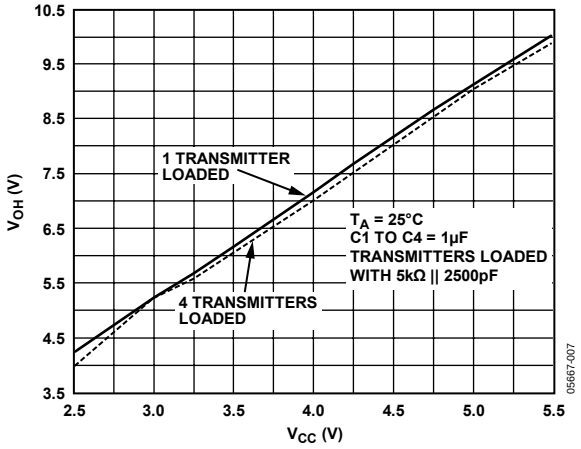


Figure 6. Transmitter Output Voltage High vs. V_{CC}

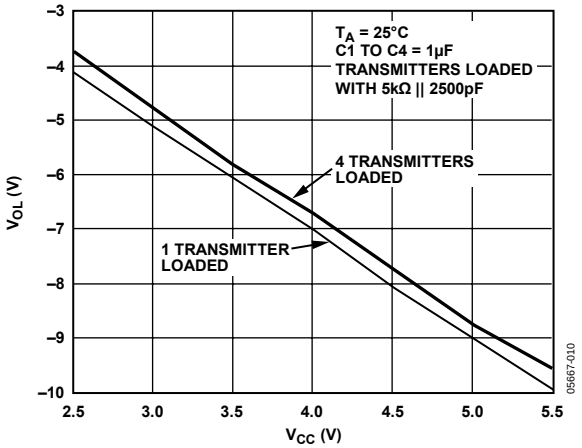


Figure 9. Transmitter Output Voltage Low vs. V_{CC}

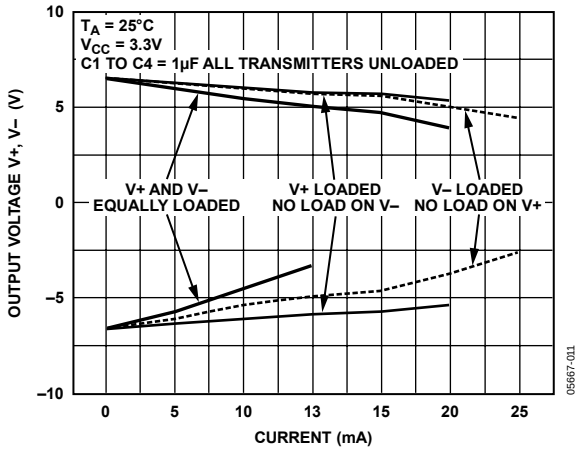


Figure 10. V+, V– vs. Load Current

THEORY OF OPERATION

The ADM560/ADM561 are RS-232 transmission line drivers/receivers, and operate from a single +3.3 V supply. This is achieved by integrating step-up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation at an absolute minimum. The ADM560/ADM561 are a modification, enhancement, and improvement to the ADM241L family and its derivatives thereof. These devices are essentially plug-in compatible and do not have materially different applications.

The ADM560/ADM561 contain an internal voltage doubler and a voltage inverter that generates ±6.6 V from the +3.3 V input. Four external 1 µF capacitors are required for the internal voltage converters.

CIRCUIT DESCRIPTION

The internal circuitry consists of three main sections. These are as follows:

- A charge pump voltage converter.
- 3 V logic to EIA-232 transmitters.
- EIA-232 to 3 V logic receivers.

Charge Pump DC-to-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±6.6 V supply from the input +3.3 V level. This is done in two stages using a switched capacitor technique (see Figure 11 and Figure 12). First, the +3.3 V input supply is doubled to +6.6 V using Capacitor C1 as the charge storage element. The +6.6 V level is then inverted to generate −6.6 V using Capacitor C2 as the storage element.

Capacitor C3 and Capacitor C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The C1 and C2 charge pump capacitors can also be reduced at the expense of the higher output impedance on the V+ and V− supplies.

The V+ and V− supplies are also used to power external circuitry if the current requirements are small.

Transmitter (Driver) Section

The drivers convert 3 V or 5 V logic input levels into EIA-232 output levels. With V_{CC} = +3.3 V and driving an EIA-232 load, the output voltage swing is typically ±5.5 V.

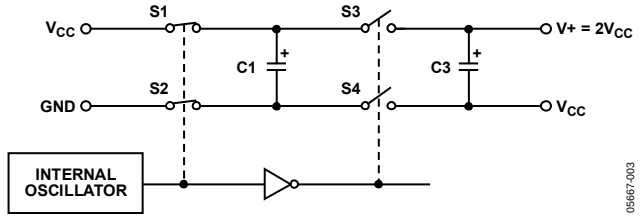


Figure 11. Charge Pump Voltage Double Operation

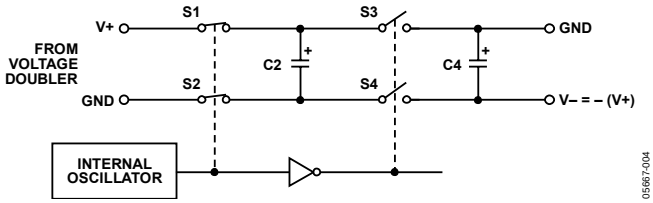


Figure 12. Charge Pump Voltage Inverted Operation

Unused inputs can be left unconnected as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state. The input pull-up resistors typically source 8 µA when grounded, so connect unused inputs to V_{CC} or leave unconnected in order to minimize power consumption.

Receiver Section

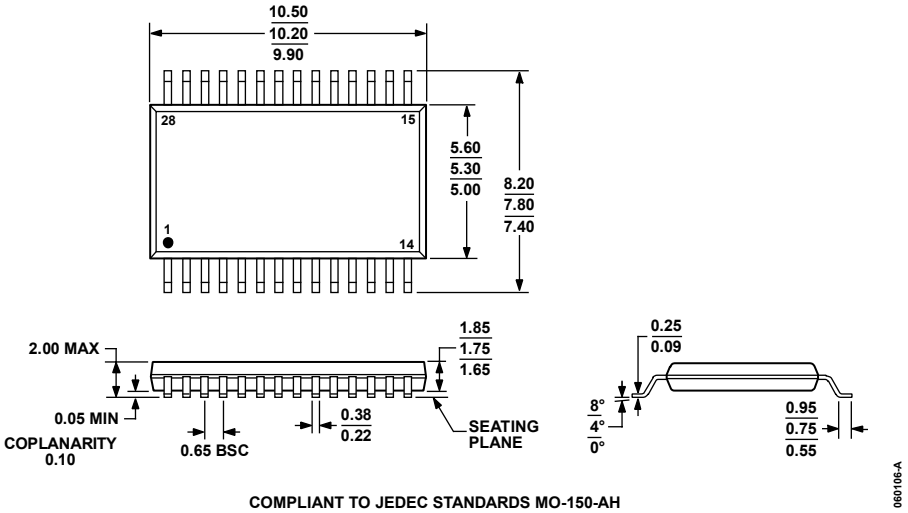
The receivers are inverting level shifters; they accept EIA-232 input levels and translate them into 3 V logic output levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±25 V. The guaranteed switching thresholds are 0.4 V minimum and 2.4 V maximum. Unconnected inputs are pulled to 0 V by the internal 5 kΩ pull-down resistor. This results in a Logic 1 output level for unconnected inputs or for inputs connected to GND.

The receivers have a Schmitt trigger input with a hysteresis level of 0.3 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

ENABLE AND SHUTDOWN

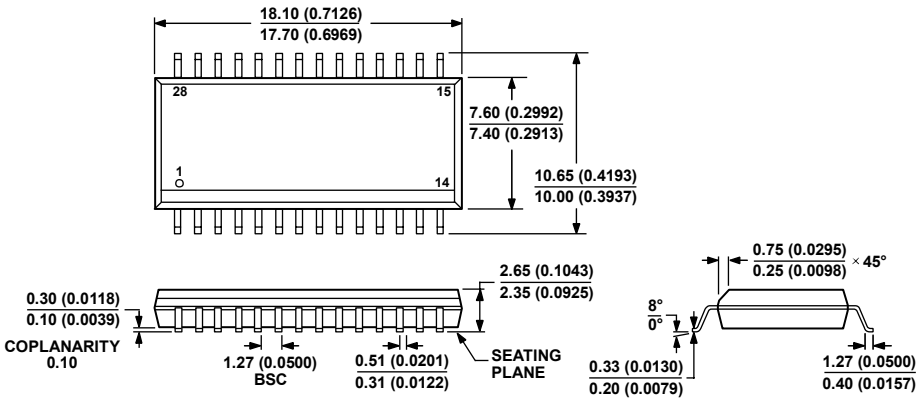
Table 4 shows the truth table for the enable and shutdown control signals. When disabled all receivers are placed in a high impedance state. In shutdown, all transmitters are disabled and all receivers on the ADM561 are disabled. On the ADM560, Receiver R4 and Receiver R5 remain enabled in shutdown.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AH

Figure 13. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 14. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM560JR	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM560JR-REEL	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM560JRZ[1]	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM560JRZ-REEL[1]	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM560JRS	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADM560JRS-REEL	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADM560JRSZ[1]	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADM560JRSZ-REEL[1]	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADM561JR	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM561JR-REEL	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM561JRZ[1]	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM561JRZ-REEL[1]	0°C to +70°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
ADM561JRS	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADM561JRS-REEL	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADM561JRSZ[1]	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADM561JRSZ-REEL[1]	0°C to +70°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28

[1] Z = Pb-free part.

NOTES

NOTES

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