

BLM7G1822S-20PB; BLM7G1822S-20PBG

LDMOS 2-stage power MMIC

Rev. 3 — 1 July 2015

Product data sheet

1. Product profile

1.1 General description

The BLM7G1822S-20PB(G) is a dual section, 2-stage power MMIC using NXP's state of the art GEN7 LDMOS technology. This multiband device is perfectly suited as general purpose driver or small cell final in the frequency range from 1805 MHz to 2170 MHz. Available in gull wing or straight lead outline.

Table 1. Performance

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $I_{DQ1} = 27\text{ mA}$; $I_{DQ2} = 76\text{ mA}$.

Test signal: 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF; per section unless otherwise specified in a class-AB production circuit.

Test signal	f	V _{DS}	P _{L(AV)}	G _p	η_D	ACPR _{5M}
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
single carrier W-CDMA	2167.5	28	2	32.3	23	-41

1.2 Features and benefits

- Designed for broadband operation (frequency 1805 MHz to 2170 MHz)
- High section-to-section isolation enabling multiple combinations
- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

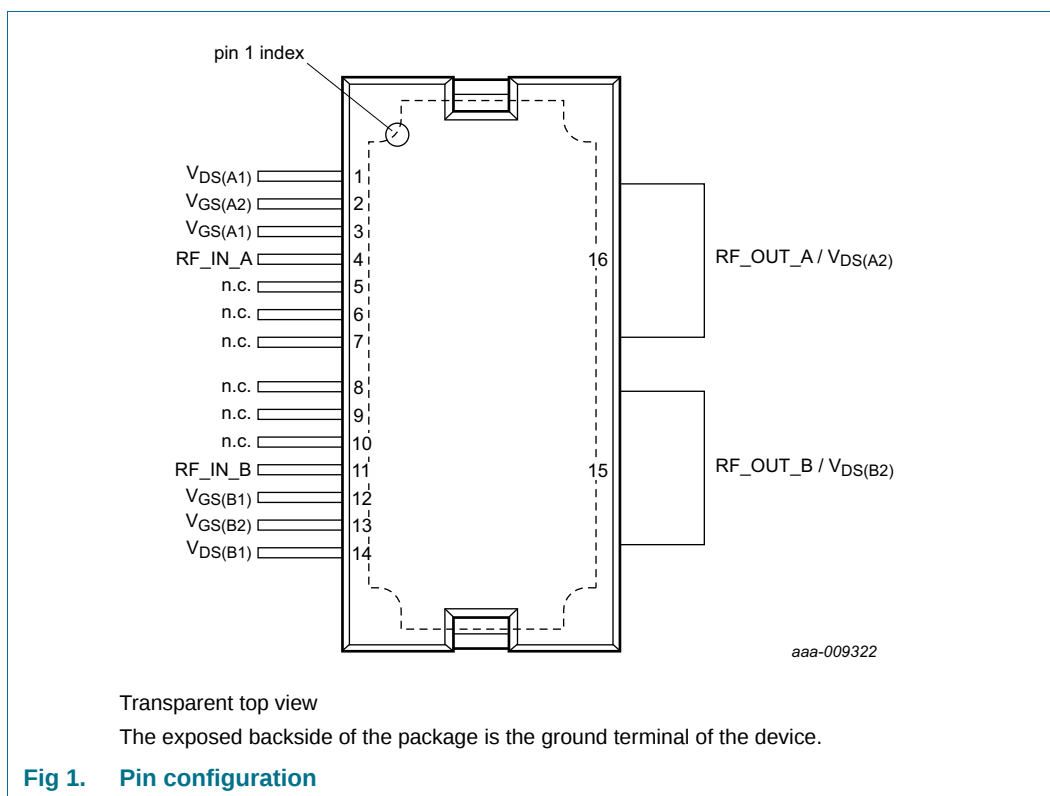
1.3 Applications

- RF power MMIC for multi-carrier and multi-standard GSM, W-CDMA and LTE base stations in the 1805 MHz to 2170 MHz frequency range. Possible circuit topologies are the following as also depicted in [Section 8.1](#):
 - ◆ Dual section or single ended
 - ◆ Doherty
 - ◆ Quadrature combined
 - ◆ Push-pull



2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{DS} (A1)	1	drain-source voltage of driver stage A1
V _{GS} (A2)	2	gate-source voltage of final stage A2
V _{GS} (A1)	3	gate-source voltage of driver stage A1
RF_IN_A	4	RF input section A
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input section B
V _{GS} (B1)	12	gate-source voltage of driver stage B1
V _{GS} (B2)	13	gate-source voltage of final stage B2
V _{DS} (B1)	14	drain-source voltage of driver stage B1

Table 2. Pin description ...continued

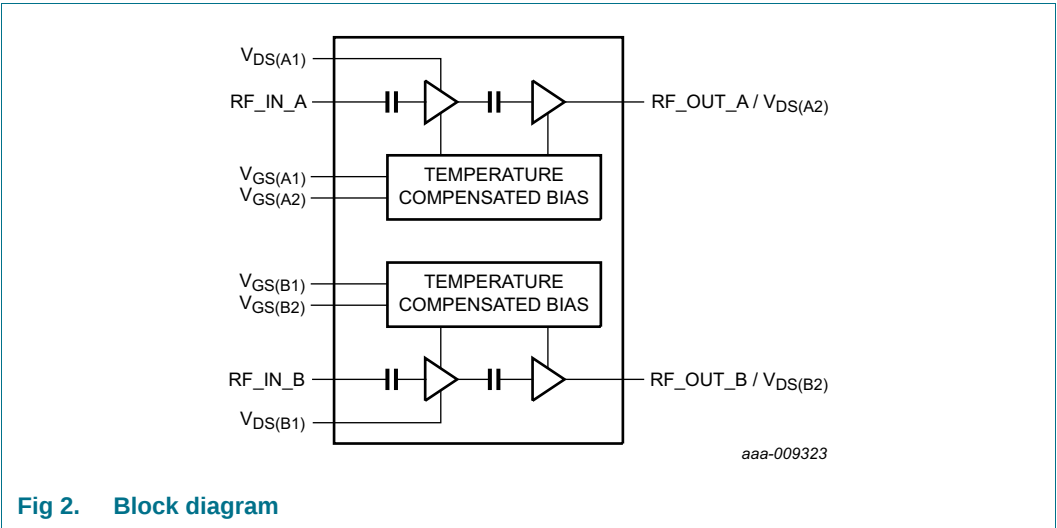
Symbol	Pin	Description
RF_OUT_B/ $V_{DS(B2)}$	15	RF output section B / drain-source voltage of final stage B2
RF_OUT_A/ $V_{DS(A2)}$	16	RF output section A / drain-source voltage of final stage A2
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM7G1822S-20PB	HSOP16F	plastic, heatsink small outline package; 16 leads(flat)	SOT1211-2
BLM7G1822S-20PBG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-2

4. Block diagram



5. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; $T_{case} = 90\text{ }^{\circ}\text{C}$; $P_L = 3.56\text{ W}$ [1]	1.9	K/W
		driver stage; $T_{case} = 90\text{ }^{\circ}\text{C}$; $P_L = 3.56\text{ W}$ [1]	6.2	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics

$T_{case} = 25\text{ }^{\circ}\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Final stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 150.8\text{ }\mu\text{A}$	65	-	-	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 76\text{ mA}$	1.5	2	2.5	V
		$V_{DS} = 28\text{ V}$; $I_D = 76\text{ mA}$ [1]	1.7	2.65	3.6	V
$\Delta I_{Dq}/\Delta T$	quiescent drain current variation with temperature	$-40\text{ }^{\circ}\text{C} \leq T_{case} \leq +85\text{ }^{\circ}\text{C}$ [1]	-	± 1	-	%
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = 5.55\text{ V}$; $V_{DS} = 10\text{ V}$	-	2.8	-	A
I_{GSS}	gate leakage current	$V_{GS} = 1.0\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
Driver stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 30.16\text{ }\mu\text{A}$	65	-	-	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 27\text{ mA}$	1.6	2.1	2.6	V
		$V_{DS} = 28\text{ V}$; $I_D = 27\text{ mA}$ [2]	1.9	2.85	3.8	V
$\Delta I_{Dq}/\Delta T$	quiescent drain current variation with temperature	$-40\text{ }^{\circ}\text{C} \leq T_{case} \leq +85\text{ }^{\circ}\text{C}$ [2]	-	± 1	-	%
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = 5.55\text{ V}$; $V_{DS} = 10\text{ V}$	-	0.55	-	A
I_{GSS}	gate leakage current	$V_{GS} = 1.0\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA

[1] In production circuit with 1105 Ω gate feed resistor.

[2] In production circuit with 765 Ω gate feed resistor.

Table 7. RF Characteristics

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ1} = 27\text{ mA}$; $I_{DQ2} = 76\text{ mA}$; $P_{L(AV)} = 2\text{ W}$. Per section unless otherwise specified, measured in a NXP wideband $f = 1807.5\text{ MHz}$ to 2167.5 MHz straight lead production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: single carrier W-CDMA [1]						
G _p	power gain	f = 1807.5 MHz	-	34	-	dB
		f = 2167.5 MHz	30.8	32.3	33.8	dB
η _D	drain efficiency	f = 1807.5 MHz	-	22	-	%
		f = 2167.5 MHz	20	23	-	%
RL _{in}	input return loss	f = 2167.5 MHz	-	−19	−10	dB
ACPR _{5M}	adjacent channel power ratio (5 MHz)	f = 1807.5 MHz	-	−41	-	dBc
		f = 2167.5 MHz	-	−41	−37	dBc
PAR _O	output peak-to-average ratio	f = 1807.5 MHz	-	8.4	-	dB
		f = 2167.5 MHz	7.2	8.4	-	dB
ΔI _{Dq} /ΔT	quiescent drain current variation with temperature	T = −40 °C to +85 °C				
		final stage I _{Dq} ; gate feed resistor = 1105 Ω	-	±1	-	%
		driver stage I _{Dq} ; gate feed resistor = 765 Ω	-	±1	-	%
Test signal: CW [2]						
Δφ _{s21}	phase response difference	between sections	−10	-	+10	deg
Δ S ₂₁ ²	insertion power gain difference	between sections	−0.5	-	+0.5	dB

[1] 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF.

[2] $f = 2170\text{ MHz}$.

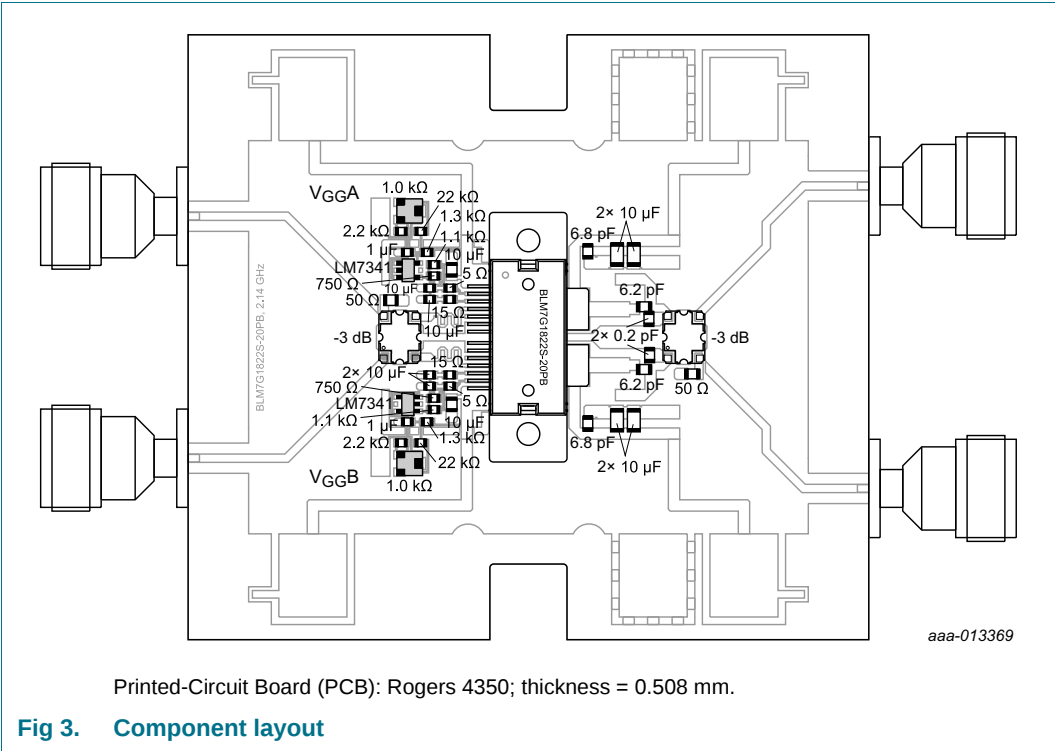
8. Application information

Table 8. Typical performance

Test signal: 1-tone CW; RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ1} = 45\text{ mA}$ (both sections); $I_{DQ2} = 140\text{ mA}$ (both sections) unless otherwise specified, measured in a NXP $f = 2110\text{ MHz}$ to 2170 MHz straight lead class AB application circuit (see Figure 3 for the component layout and Figure 4 for the electrical schematic).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	$f = 2140\text{ MHz}$	-	43.5	-	W
$P_{L(3dB)}$	output power at 3 dB gain compression	$f = 2140\text{ MHz}$	-	44.1	-	W
η_D	drain efficiency	at $P_{L(1dB)}$; $f = 2140\text{ MHz}$	-	47.6	-	%
G_p	power gain	$P_{L(AV)} = 1.585\text{ W}$; $f = 2140\text{ MHz}$	-	31.5	-	dB
B_{video}	video bandwidth	2-tone CW; $P_{L(AV)} = 1.585\text{ W}$; $f = 2140\text{ MHz}$	-	170	-	MHz
G_{flat}	gain flatness	over a frequency range of 60 MHz; $P_{L(AV)} = 1.585\text{ W}$	-	0.4	-	dB
$\Delta G/\Delta T$	gain variation with temperature	$f = 2140\text{ MHz}$	-	0.03	-	dB/ $^{\circ}\text{C}$
$ S_{12} ^2$	isolation	between sections A and B; $P_{L(AV)} = 1.585\text{ W}$; $f = 2140\text{ MHz}$	[1]	28.5	-	dB
K	Rollett stability factor	$T = -40\text{ }^{\circ}\text{C}$; $f = 0.1\text{ GHz}$ to 3 GHz	-	>1	-	

[1] Measured on dual section evaluation board $I_{DQ1} = 40\text{ mA}$ (both sections); $I_{DQ2} = 150\text{ mA}$ (both sections).



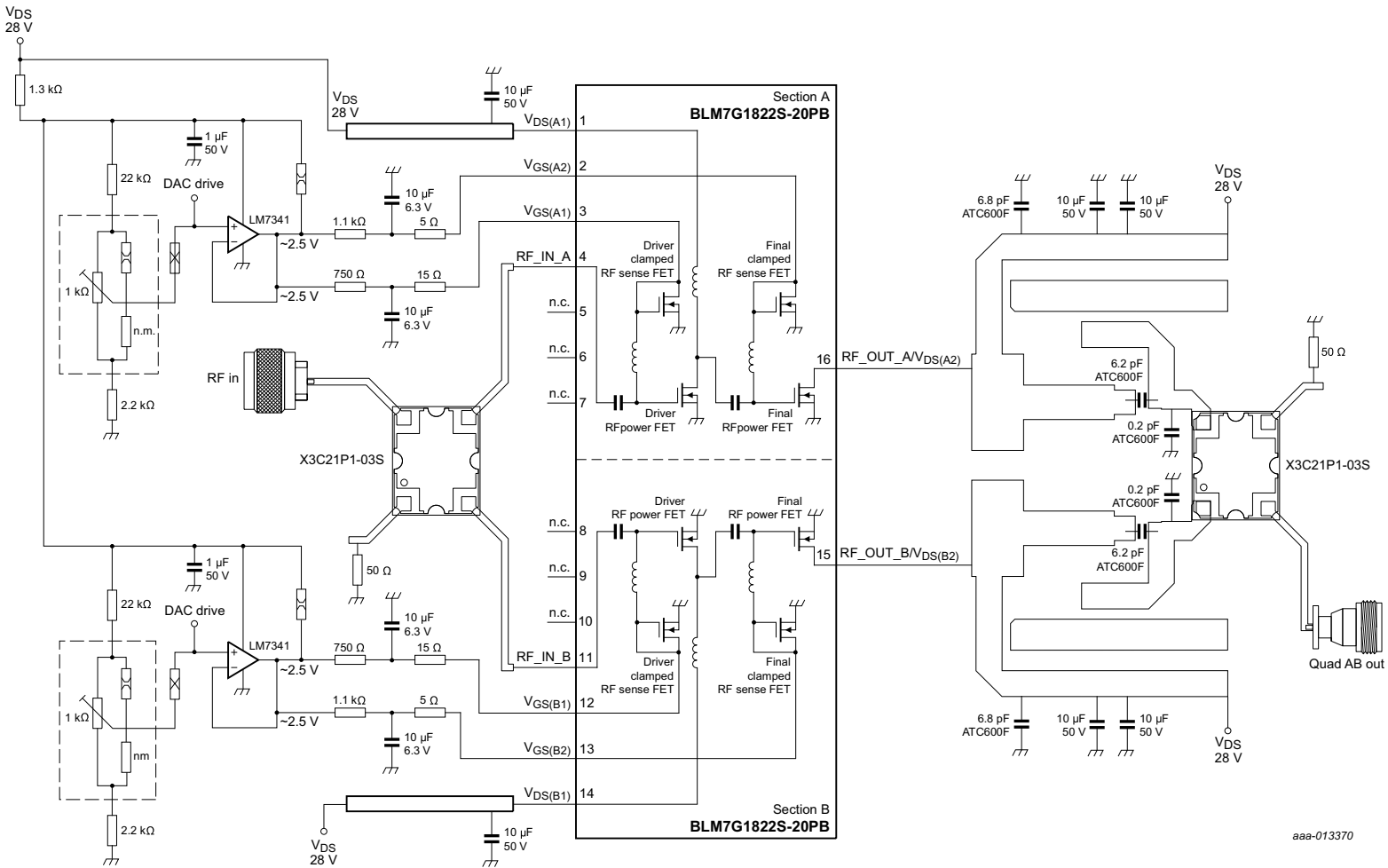


Fig 4. Electrical schematic

8.1 Possible circuit topologies

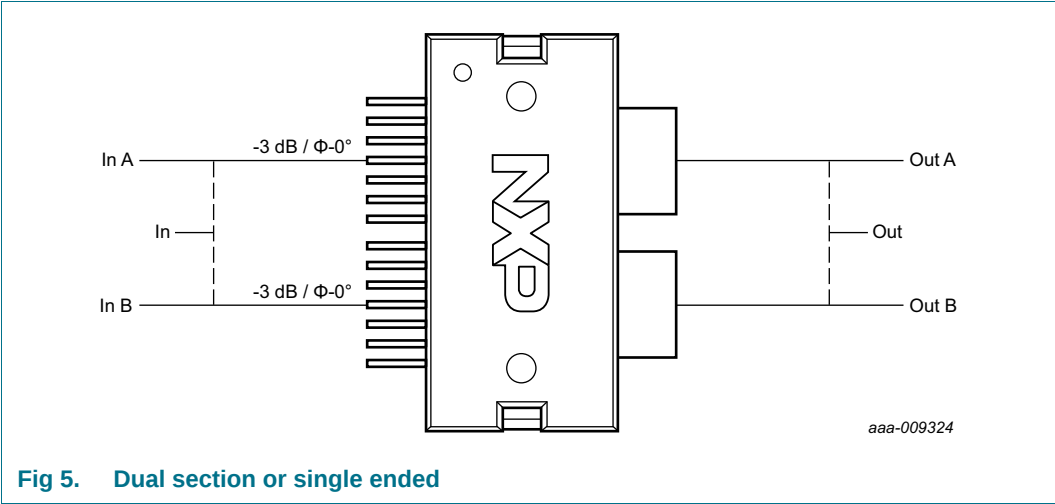


Fig 5. Dual section or single ended

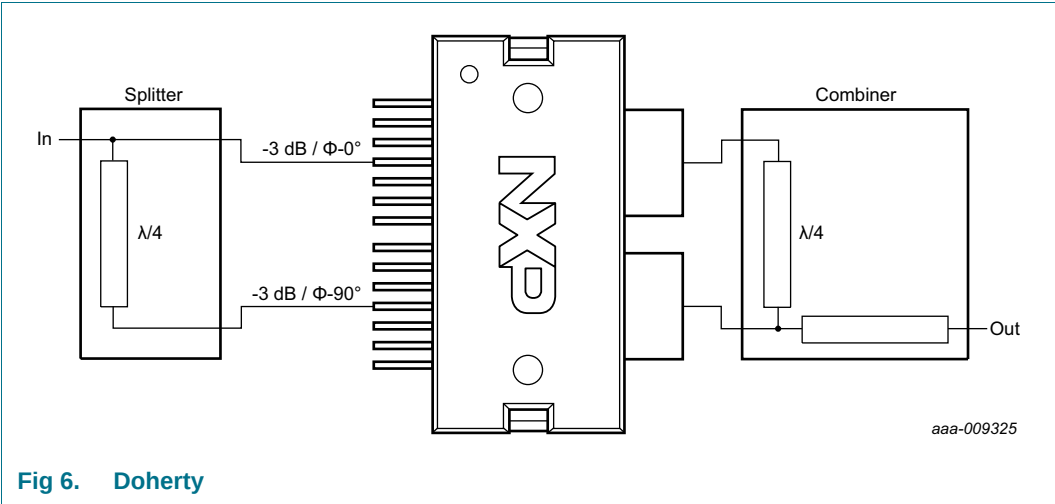


Fig 6. Doherty

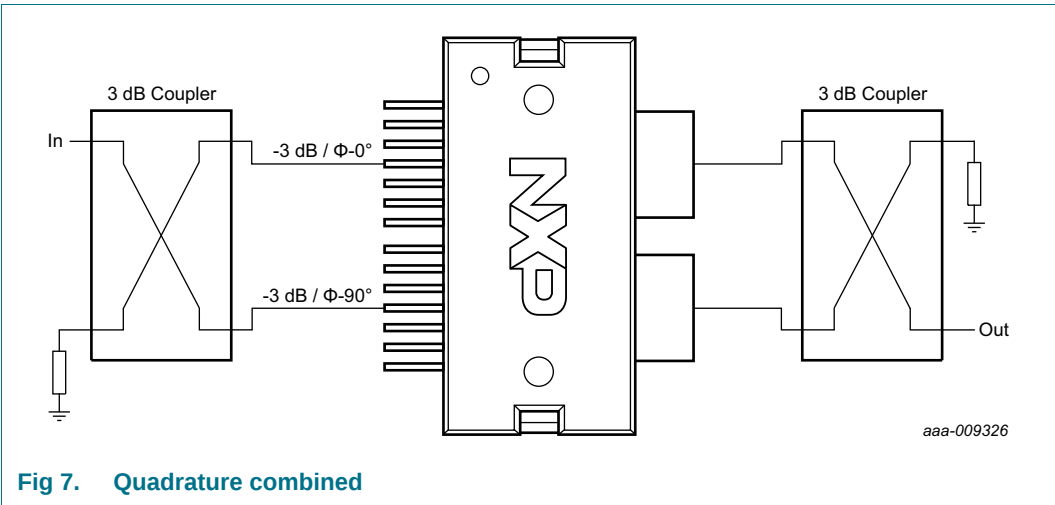
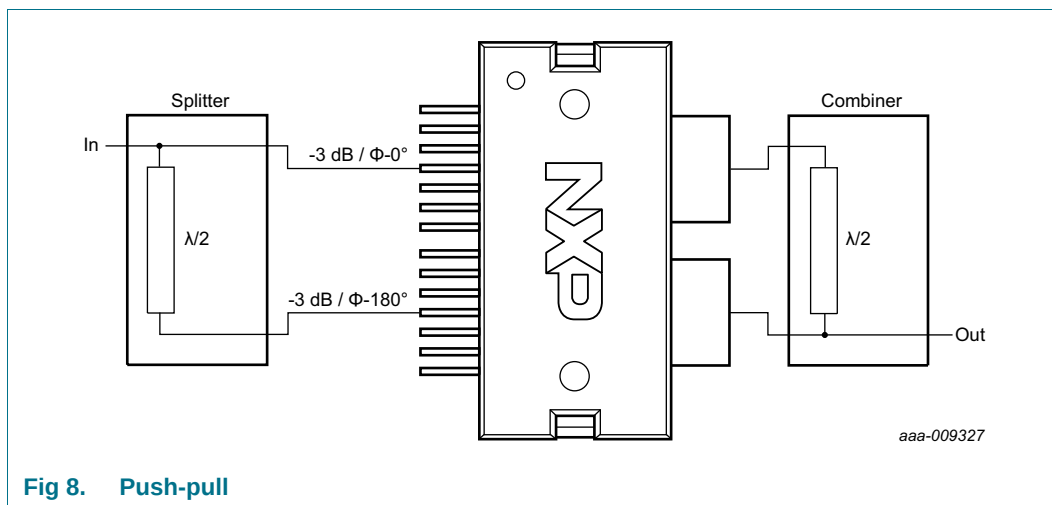


Fig 7. Quadrature combined



8.2 Ruggedness in class-AB operation

The BLM7G1822S-20PB and BLM7G1822S-20PBG are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 32$ V; $I_{DQ1} = 20$ mA (per section); $I_{DQ2} = 75$ mA (per section); $P_i = 16$ dBm (CW and corresponding to $P_{L(3dB)}$ under $Z_S = 50 \Omega$ load); $f = 2140$ MHz.

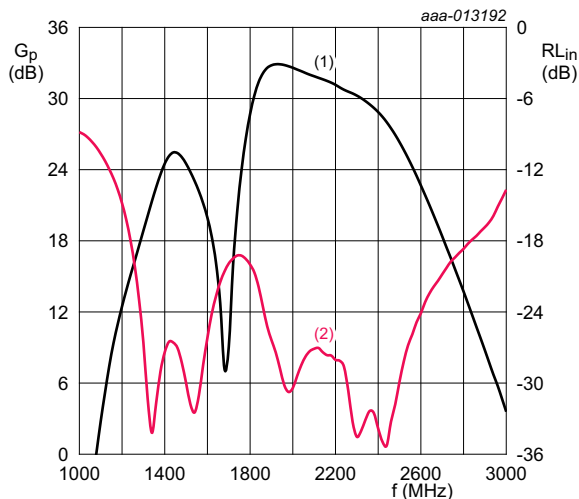
8.3 Impedance information

Table 9. Typical impedance at 3 dB compression point

Measured load-pull data per section; test signal: pulsed CW; $T_{case} = 25$ °C; $V_{DS} = 28$ V; $I_{DQ1} = 20$ mA; $I_{DQ2} = 65$ mA; $t_p = 100$ μs; $\delta = 10$ %; $Z_S = 50 \Omega$. Typical values unless otherwise specified.

f (MHz)	tuned for maximum output power					tuned for maximum efficiency				
	Z_L (Ω)	$G_{p(max)}$ (dB)	P_L (W)	η_{add} (%)	AM-PM conversion (deg)	Z_L (Ω)	$G_{p(max)}$ (dB)	P_L (W)	η_{add} (%)	AM-PM conversion (deg)
BLM7G1822S-20PB										
1700	15.3 – j14.5	33.2	42.7	50.6	8.3	28.5 – j20.2	34.6	41.6	56.5	9.2
1800	16.3 – j11.7	32.9	42.7	50.8	6.3	31.3 – j8.60	34.1	41.6	57.1	7.0
1900	16.1 – j9.70	32.1	42.8	50.8	6.1	26.5 – j0.01	33.3	41.7	57.3	6.9
2000	15.5 – j8.10	31.5	42.8	50.1	6.1	21.0 + j2.20	32.6	42.0	56.4	7.3
2100	14.4 – j6.90	31.5	42.9	50.0	6.9	15.6 + j2.00	32.9	42.1	55.8	8.6
2200	13.7 – j6.60	31.7	42.7	49.8	8.5	12.3 + j1.20	33.0	41.6	54.3	9.6
2300	12.8 – j6.80	31.4	42.5	49.1	10.6	10.0 + j0.10	32.5	41.3	53.6	10.3
BLM7G1822S-20PBG										
1700	15.8 – j16.1	33.5	42.5	52.9	9.2	28.9 – j21.8	35.1	41.6	57.9	11.1
1800	16.5 – j13.8	32.9	42.5	51.2	7.7	30.6 – j11.6	34.2	41.6	56.8	8.4
1900	16.7 – j12.4	32.2	42.5	50.2	7.2	27.9 – j4.64	33.5	41.7	55.9	7.8
2000	16.3 – j9.74	31.7	42.5	51.2	7.3	20.4 + j0.45	32.7	41.7	55.6	9.0
2100	15.6 – j8.61	31.5	42.6	52.0	9.5	15.9 + j0.68	32.6	41.7	56.5	11.8
2200	14.6 – j8.87	31.3	42.5	49.7	10.3	12.7 – j0.44	32.4	41.6	53.8	12.1
2300	13.4 – j9.32	30.5	42.4	48.2	12.8	10.7 – j1.98	31.7	41.6	53.7	13.2

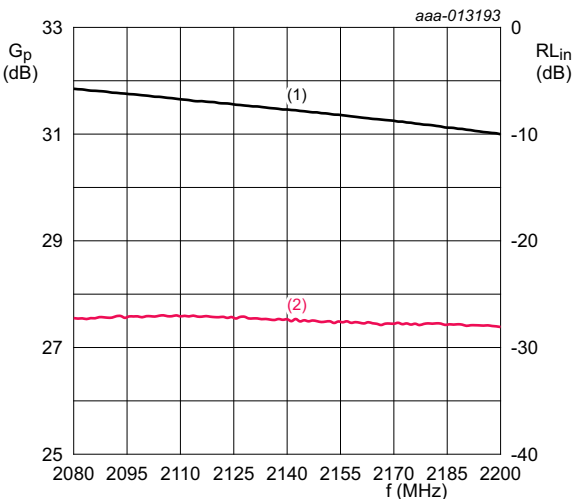
8.4 Graphs



$T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ1} = 22\text{ mA}$; $I_{DQ2} = 70\text{ mA}$; $P_L = 1.585\text{ W}$. Per section.

- (1) magnitude of G_p
- (2) magnitude of RL_{in}

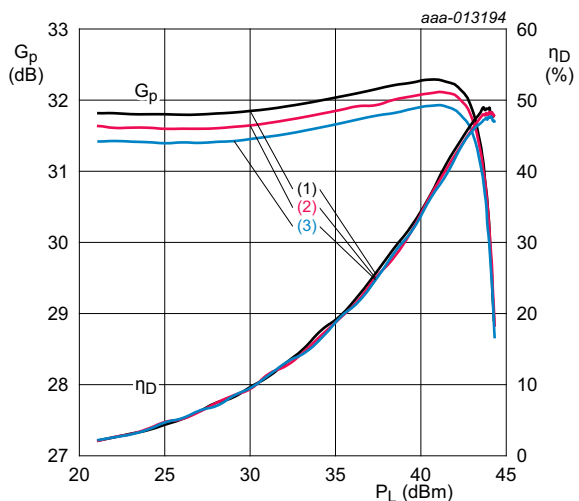
Fig 9. Wideband power gain and input return loss as function of frequency; typical values



$T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ1} = 22\text{ mA}$; $I_{DQ2} = 70\text{ mA}$; $P_L = 1.585\text{ W}$. Per section.

- (1) magnitude of G_p
- (2) magnitude of RL_{in}

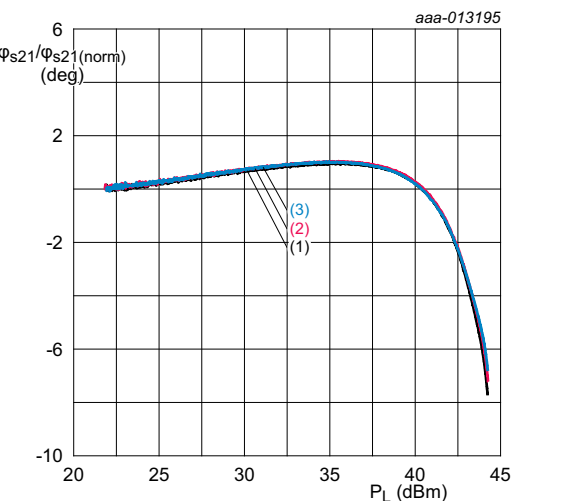
Fig 10. In-band power gain and input return loss as function of frequency; typical values



$T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ1} = 22\text{ mA}$; $I_{DQ2} = 70\text{ mA}$. Per section.

- (1) $f = 2110\text{ MHz}$
- (2) $f = 2140\text{ MHz}$
- (3) $f = 2170\text{ MHz}$

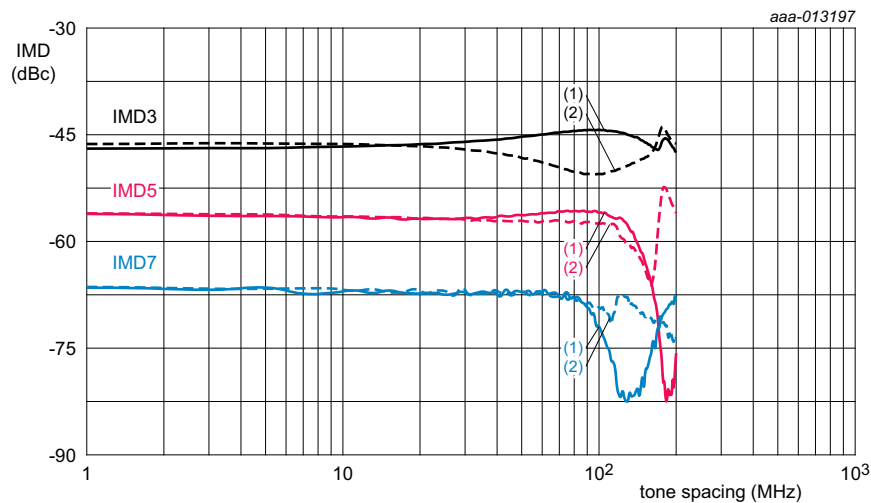
Fig 11. Power gain and drain efficiency as function of output power; typical values



Normalized at $P_L = 22\text{ dBm}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ1} = 22\text{ mA}$; $I_{DQ2} = 70\text{ mA}$. Per section.

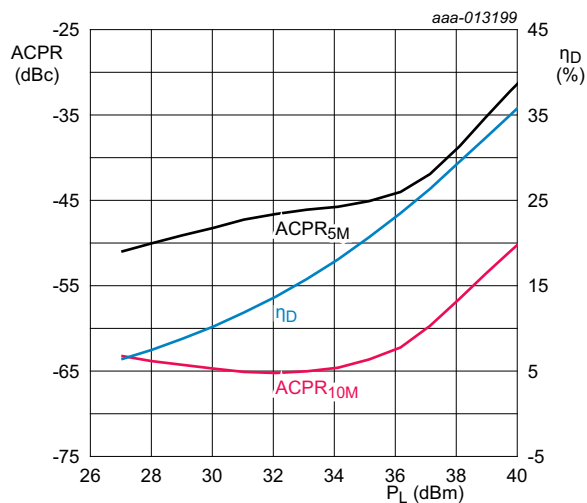
- (1) $f = 2110\text{ MHz}$
- (2) $f = 2140\text{ MHz}$
- (3) $f = 2170\text{ MHz}$

Fig 12. Normalized phase response as a function of output power; typical values



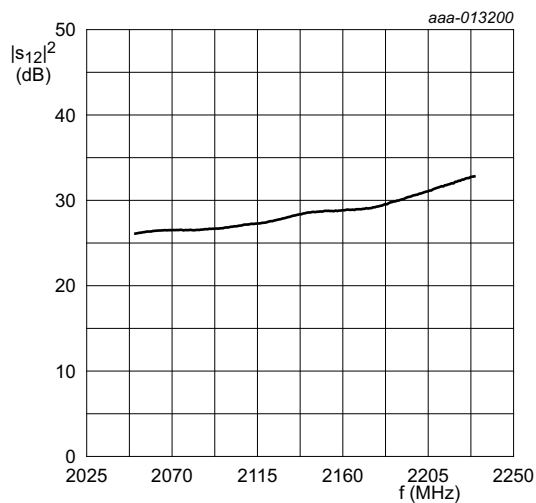
$T_{\text{case}} = 25\text{ }^{\circ}\text{C}$; $V_{\text{DS}} = 28\text{ V}$; $I_{\text{DQ1}} = 22\text{ mA}$; $I_{\text{DQ2}} = 70\text{ mA}$; $f = 2140\text{ MHz}$; 2-tone CW; $P_{\text{L(AV)}} = 0.25\text{ W}$. Per section.
 (1) IMD low
 (2) IMD high

Fig 13. Intermodulation distortion as a function of tone spacing; typical values



$T_{\text{case}} = 25\text{ }^{\circ}\text{C}$; $V_{\text{DS}} = 28\text{ V}$; $I_{\text{DQ1}} = 22\text{ mA}$; $I_{\text{DQ2}} = 70\text{ mA}$;
 $f = 2140\text{ MHz}$; 1-carrier W-CDMA; test model 1;
 $\text{PAR} = 7.2\text{ dB}$ at 0.01 % probability on CCDF. Per section.

Fig 14. Adjacent channel power ratio and drain efficiency as function of output power; typical values



$T_{\text{case}} = 25\text{ }^{\circ}\text{C}$; $V_{\text{DS}} = 28\text{ V}$; $I_{\text{DQ1}} = 20\text{ mA}$; $I_{\text{DQ2}} = 75\text{ mA}$.
 Per section. Measured on evaluation board.

Fig 15. Isolation as a function of frequency; typical values

9. Package outline

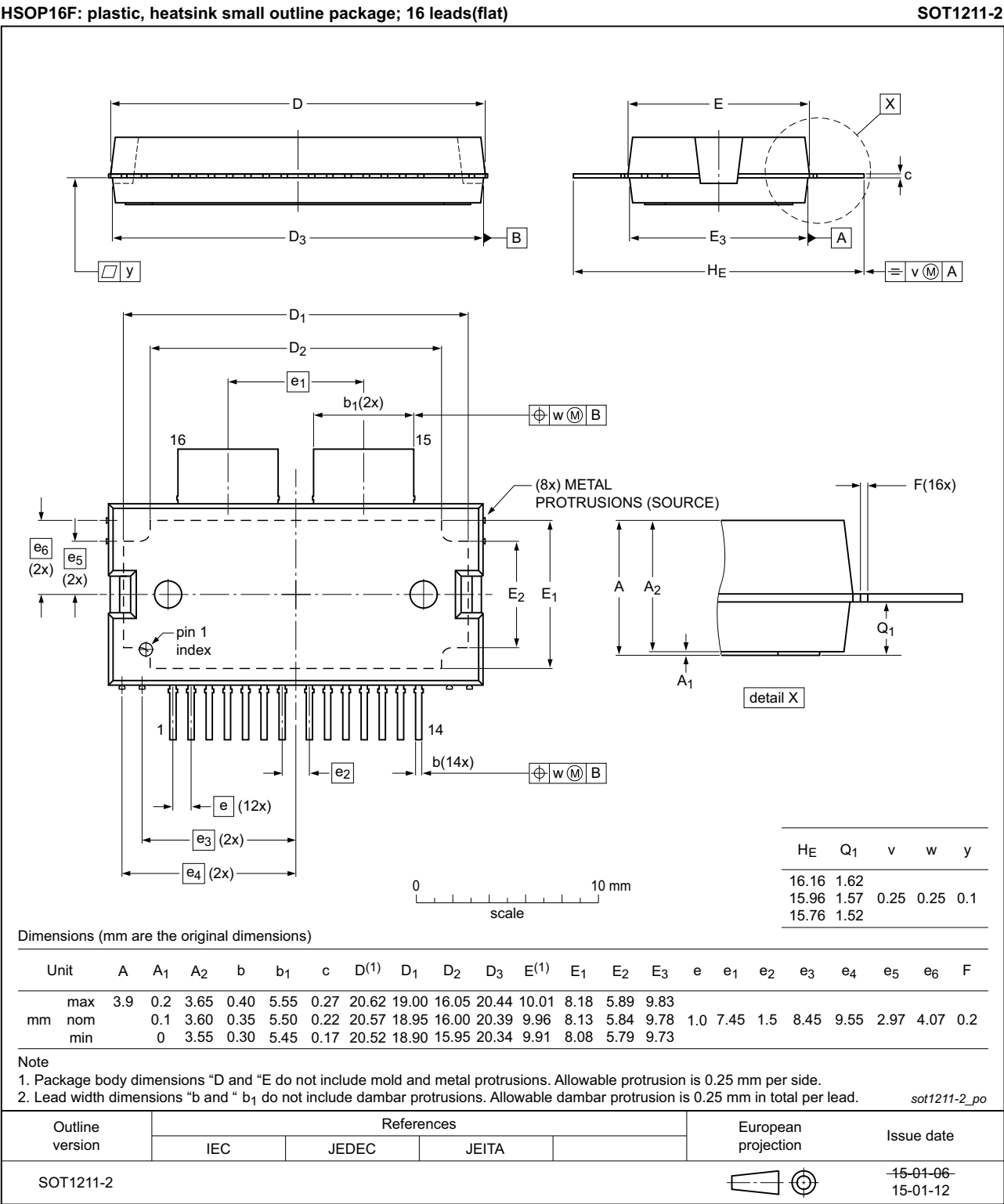


Fig 16. Package outline SOT1211-2 (HSOP16F)

HSOP16: plastic, heatsink small outline package; 16 leads

SOT1212-2

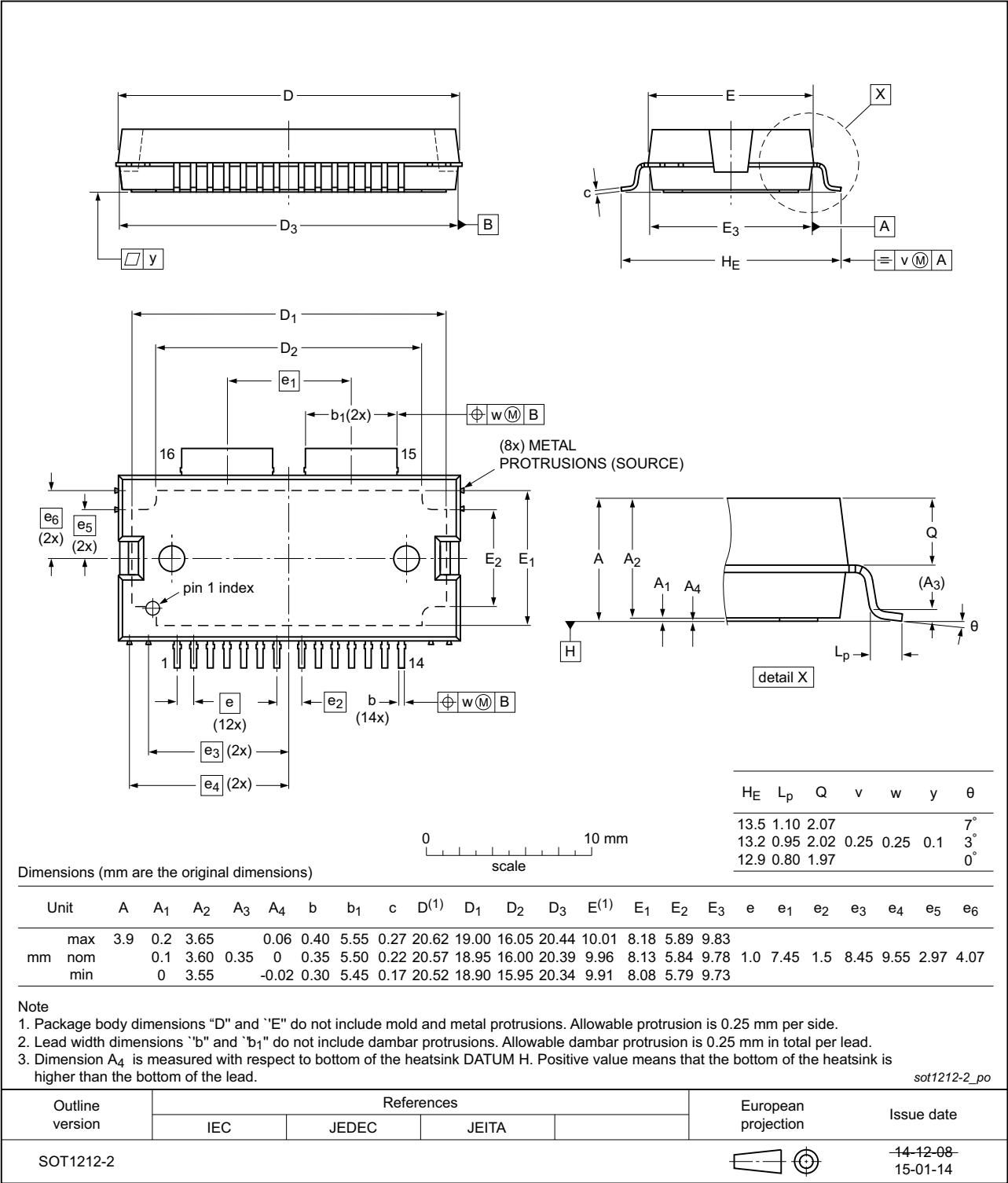


Fig 17. Package outline SOT1212-2 (HSOP16)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
AM	Amplitude Modulation
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GEN7	Seventh Generation
GSM	Global System for Mobile Communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
PM	Phase Modulation
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G1822S-20PB_S-20PBG v.3	20150701	Product data sheet	-	BLM7G1822S-20PB_S-20PBG v.2
Modifications:	• Table 1 on page 1: the table has been updated • Section 1.3 on page 1: first paragraph has been updated • Table 2 on page 2: the table has been updated • Table 3 on page 3: the package version of the BLM7G1822S-20PB has been changed to SOT1211-2 • Table 3 on page 3: the package version of the BLM7G1822S-20PBG has been changed to SOT1212-2 • Table 6 on page 4: the table has been updated • Table 7 on page 5: the table has been updated • Table 8 on page 5: the general conditions have been updated • Figure 3 on page 6: the title of the figure has been changed • Section 8.2 on page 9: the section has been updated • Table 9 on page 9: the table has been updated • Figure 16 on page 12: the figure now shows the SOT1211-2 package outline • Figure 17 on page 13: the figure now shows the SOT1212-2 package outline			
BLM7G1822S-20PB_S-20PBG v.2	20140626	Objective data sheet	-	BLM7G1822S-20PB_S-20PBG v.1
BLM7G1822S-20PB_S-20PBG v.1	20131219	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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