MF5

MF5 Universal Monolithic Switched Capacitor Filter



Literature Number: SNOSBC9A

National Semiconductor

February 1995

MF5 Universal Monolithic Switched Capacitor Filter

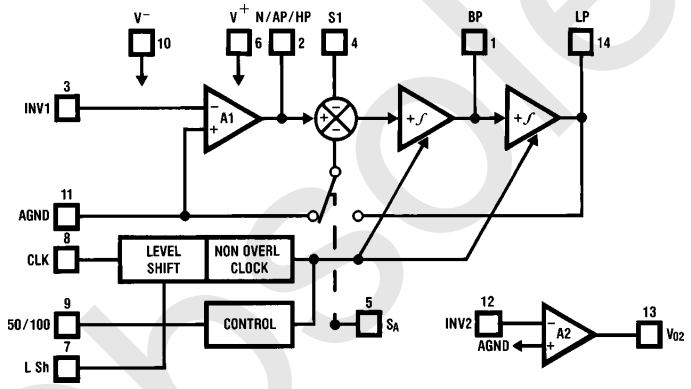
General Description

The MF5 consists of an extremely easy to use, general purpose CMOS active filter building block and an uncommitted op amp. The filter building block, together with an external clock and a few resistors, can produce various second order functions. The filter building block has 3 output pins. One of the output pins can be configured to perform highpass, allpass or notch functions and the remaining 2 output pins perform bandpass and lowpass functions. The center frequency of the filter can be directly dependent on the clock frequency or it can depend on both clock frequency and external resistor ratios. The uncommitted op amp can be used for cascading purposes, for obtaining additional allpass and notch functions, or for various other applications. Higher order filter functions can be obtained by cascading several MF5s or by using the MF5 in conjuction with the MF10 (dual switched capacitor filter building block). The MF5 is functionally compatible with the MF10. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

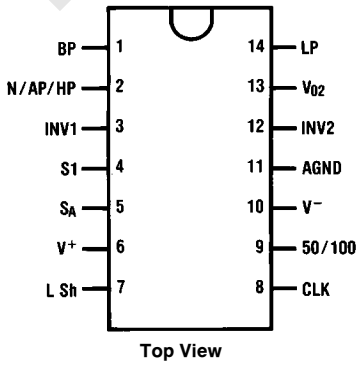
- Low cost
- 14-pin DIP or 14-pin Surface Mount (SO) wide-body package
- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variations
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_o \times Q$ range up to 200 kHz
- Operation up to 30 kHz (typical)
- Additional uncommitted op-amp

Block and Connection Diagrams



TL/H/5066–1

All Packages



Top View

TL/H/5066–2

Order Number MF5CN
See NS Package Number N14A

Order Number MF5CWM
See NS Package Number M14B

Obsolete

©1995 National Semiconductor Corporation

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	14V
Power Dissipation $T_A = 25°C$ (note 1)	500 mW
Storage Temp.	150°C
Soldering Information:	
N Package: 10 sec.	260°C
SO Package: Vapor phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Input Voltage (any pin)	$V^- \le V_{in} \le V^+$
Operating Temp. Range	$T_{MIN} \le T_A \le T_{MAX}$
MF5CN, MF5CWM	$0°C \le T_A \le 70°C$

Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Supply Voltage ($V^+ - V^-$)	Min				**8**	V
	Max				**14**	V
Maximum Supply Current		Clock applied to Pin 8 No Input Signal	4.5	6.0		mA
Clock Feedthrough	Filter Output		10			mV
	Op-amp Output		10			mV

Filter Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Center Frequency Range (f_o)	Max			30		**20**	kHz
	Min			0.1		**0.2**	Hz
Clock Frequency Range (f_{CLK})	Max			1.5		**1.0**	MHz
	Min			5.0		**10**	Hz
Clock to Center Frequency Ratio (f_{CLK}/f_o)		Ideal Q = 10 Mode 1	$V_{pin9} = +5V$ $F_{CLK} = 250$ kHz	50.11 ± 0.2%	50.11 ± 1.5%		
			$V_{pin9} = -5V$ $F_{CLK} = 500$ kHz	100.04 ± 0.2%	100.04 ± 1.5%		
f_{CLK}/f_o Temp. Coefficient		$V_{pin9} = +5V$ (50:1 CLK ratio)		±10			ppm/°C
		$V_{pin9} = -5V$ (100:1 CLK ratio)		±20			ppm/°C
Q Accuracy (Max) (Note 2)		Ideal Q = 10 Mode 1	$V_{pin9} = +5V$ $F_{CLK} = 250$ kHz		±10		%
			$V_{pin9} = -5V$ $F_{CLK} = 500$ kHz		±10		%
Q Temperature Coefficient		$V_{pin9} = +5V$ (50:1 CLK ratio)		−200			ppm/°C
		$V_{pin9} = -5V$ (100:1 CLK ratio)		−70			ppm/°C
DC Lowpass Gain Accuracy (Max)		Mode 1 R1 = R2 = 10 kΩ			±0.2		dB
DC Offset Voltage (Max) (Note 3)	V_{os1}			±5.0			mV
	V_{os2}	$V_{pin9} = +5V$ (50:1 CLK ratio)		−185			mV
	V_{os3}			+115			mV
	V_{os2}	$V_{pin9} = -5V$ (100:1 CLK ratio)		−310			mV
	V_{os3}			+240			mV

Obsolete

Filter Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$. (Continued)

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Output Swing (Min)	BP, LP pins	RL = 5 kΩ	±4.0	±3.8		V
	N/AP/HP pin	RL = 3.5 kΩ	±4.2	±3.8		V
Dynamic Range (Note 4)		V_{pin9} = +5V (50:1 CLK ratio)	83			dB
		V_{pin9} = −5V (100:1 CLK ratio)	80			dB
Maximum Output Short Circuit Current (Note 5)	Source		20			mA
	Sink		3.0			mA

OP-AMP Electrical Characteristics

$V^+ = +5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless other noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Gain Bandwidth Product			2.5			MHz
Output Voltage Swing (Min)		RL = 3.5 kΩ	±4.2	±3.8		V
Slew Rate			7.0			V/μs
DC Open-Loop Gain			80			db
Input Offset Voltage (Max)			±5.0	±20		mV
Input Bias Current			10			pA
Maximum Output Short Circuit Current (Note 5)	Source		20			mA
	Sink		3.0			mA

Logic Input Characteristics

Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$. All other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CMOS Clock Input	Min Logical "1" Input Voltage	$V^+ = +5V$, $V^- = -5V$, $V_{L.Sh.} = 0V$		3.0		V
	Max Logical "0" Input Voltage			−3.0		V
	Min Logical "1" Input Voltage	$V^+ = +10V$, $V^- = 0V$, $V_{L.Sh.} = +5V$		8.0		V
	Max Logical "0" Input Voltage			2.0		V
TTL Clock Input	Min Logical "1" Input Voltage	$V^+ = +5V$, $V^- = -5V$, $V_{L.Sh.} = 0V$		2.0		V
	Max Logical "0" Input Voltage			0.8		V

Note 1: The typical junction-to-ambient thermal resistance (θ_{JA}) of the 14 pin N package is 160°C/W, and 82°C/W for the M package.

Note 2: The accuracy of the Q value is a function of the center frequency (f_o). This is illustrated in the curves under the heading "Typical Performance Characteristics".

Note 3: V_{os1}, V_{os2}, and V_{os3} refer to the internal offsets as discussed in the Application Information section 3.4.

Note 4: For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μV rms for the MF5 with a 50:1 CLK ratio and 280 μV rms for the MF5 with a 100:1 CLK ratio.

Note 5: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% tested.

Note 8: Guaranteed, but not 100% tested. These limits are not used to calculate outgoing quality levels.

Obsolete

Pin Description

LP(14), BP(1), N/AP/HP(2): The second order lowpass, bandpass, and notch/allpass/highpass outputs. The LP and BP outputs can typically sink 1 mA and source 3 mA. The N/AP/HP output can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1V of each supply.

INV1(3): The inverting input of the summing op amp of the filter. This is a high impedance input, but the non-inverting input is internally tied to AGND, making INV1 behave like a summing junction (low impedance current input).

S1(4): S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

SA(5): This pin activates a switch that connects one of the inputs of the filter's second summer to either AGND (SA tied to V−) or to the lowpass (LP) output (SA tied to V+). This offers the flexibility needed for configuring the filter in its various modes of operation.

50/100(9): This pin is used to set the internal clock to center frequency ratio (f_{CLK}/f_o) of the filter. By tying the pin to V+ an f_{CLK}/f_o ratio of about 50:1 (typically 50.11 ± 0.2%) is obtained. Tying the 50/100 pin to either AGND or V− will set the f_{CLK}/f_o ratio to about 100:1 (typically 100.04 ± 0.2%).

AGND(11): This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

V+(6), V−(10): These are the positive and negative supply pins. The MF5 will operate over a total supply range of 8V to 14V. Decoupling the supply pins with 0.1 μF capacitors is highly recommended.

CLK(8): This is the clock input for the filter. CMOS or TTL logic level clocks can be accomodated by setting the L. Sh pin to the levels described in the L. Sh pin description. For optimum filter performance a 50% duty cycle clock is recommended for clock frequencies greater than 200 kHz. This gives each op amp the maximum amount of time to settle to a new sampled input.

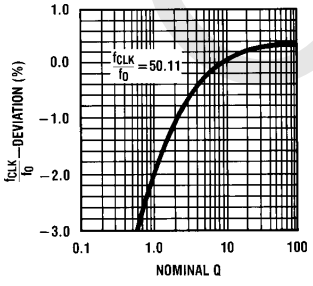
L. Sh(7): This pin allows the MF5 to accommodate either CMOS or TTL logic level clocks. For dual supply operation (i.e., ±5V), a CMOS or TTL logic level clock can be accepted if the L. Sh pin is tied to mid-supply (AGND), which should be the system ground. For single supply operation the L. Sh pin should be tied to mid-supply (AGND) for a CMOS logic level clock. The mid-supply bias should be a very low impedance node. See Applications Information for biasing techniques. For a TTL logic level clock the L. Sh pin should be tied to V− which should be the system ground.

INV2(12): This is the inverting input of the uncommitted op amp. This is a very high impedance input, but the non-inverting input is internally tied to AGND, making INV2 behave like a summing junction (low-impedance current input).

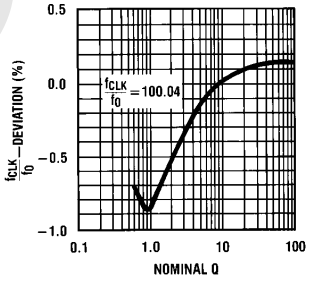
Vo2(13): This is the output of the uncommitted op amp. It will typically sink 1.5 mA and source 3.0 mA. It will typically swing to within 1V of each supply.

Typical Performance Characteristics

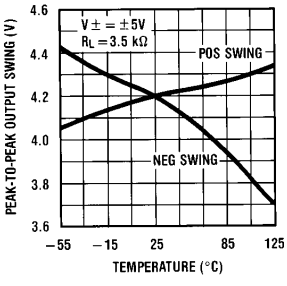
Deviation of $\frac{F_{CLK}}{F_o}$ vs Nominal Q



Deviation of $\frac{F_{CLK}}{F_o}$ vs Nominal Q



OPAMP Output Voltage Swing vs Temperature

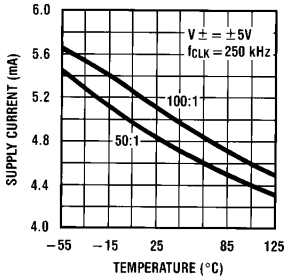


TL/H/5066–3

Obsolete

Typical Performance Characteristics (Continued)

Supply Current vs Temperature



TL/H/5066–4

1.0 Definitions of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 8.

f_o: center frequency of the second order function complex pole pair. f_o is measured at the bandpass output of the MF5, and is the frequency of maximum bandpass gain. (*Figure 1*).

f_{notch}: the frequency of minimum (ideally zero) gain at the notch output.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_o and if Q_z is high, it can be observed as the frequency of a notch at the allpass output. (*Figure 10*).

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass output of the MF5 and is equal to f_o divided by the −3dB bandwidth of the 2nd order bandpass filter (*Figure 1*). The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_z: the quality factor of the second order complex zero pair, if any. Q_z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q_z} + {\omega_o}^2\right)}{s^2 + \frac{s\omega_o}{Q} + {\omega_o}^2}$$

where $Q_z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_o$.

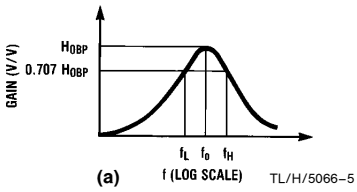
H_{OLP}: the gain (in V/V) of the lowpass output as $f \rightarrow 0$ Hz (*Figure 2*).

H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{clk}/2$ (*Figure 3*).

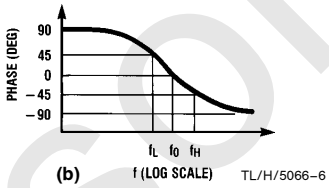
H_{ON}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz and as $f \rightarrow f_{clk}/2$, when the notch filter has equal gain above and below the center frequency (*Figure 4*). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (*Figures 11* and *8*), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz.

H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{clk}/2$.



TL/H/5066–5



TL/H/5066–6

$$H_{BP}(s) = \frac{H_{OBP}\frac{\omega_o}{Q}s}{s^2 + \frac{s\omega_o}{Q} + {\omega_o}^2}$$

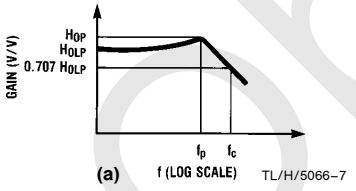
$$Q = \frac{f_o}{f_H - f_L};\quad f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

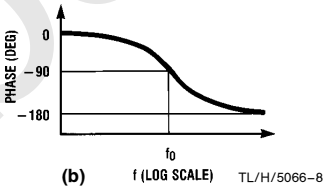
$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$\omega_o = 2\pi f_o$$

FIGURE 1. 2nd-Order Bandpass Response



TL/H/5066–7



TL/H/5066–8

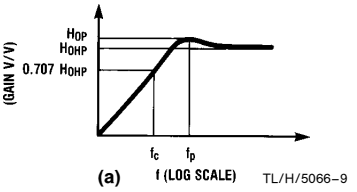
$$H_{LP}(s) = \frac{H_{OLP}{\omega_o}^2}{s^2 + \frac{s\omega_o}{Q} + {\omega_o}^2}$$

$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

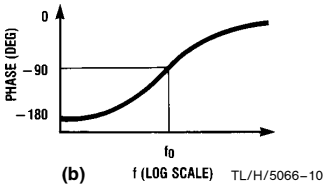
$$f_p = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2. 2nd-Order Low-Pass Response



TL/H/5066–9



TL/H/5066–10

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_o}{Q} + {\omega_o}^2}$$

$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

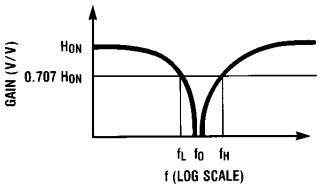
$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 3. 2nd-Order High-Pass Response

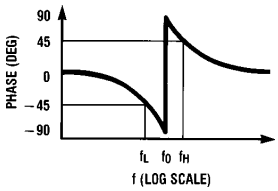
Obsolete

1.0 Definition of Terms (Continued)



TL/H/5066–11

(a)



TL/H/5066–12

(b)

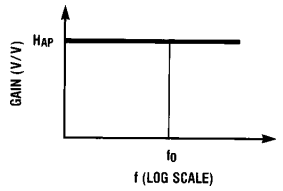
$$H_N(s) = \frac{H_{ON}(s^2 + \omega_o^2)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_o}{f_H - f_L}; \quad f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

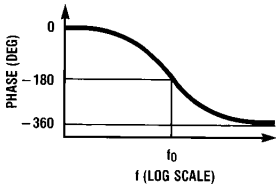
$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 4. 2nd-Order Notch Response



TL/H/5066–13

(a)

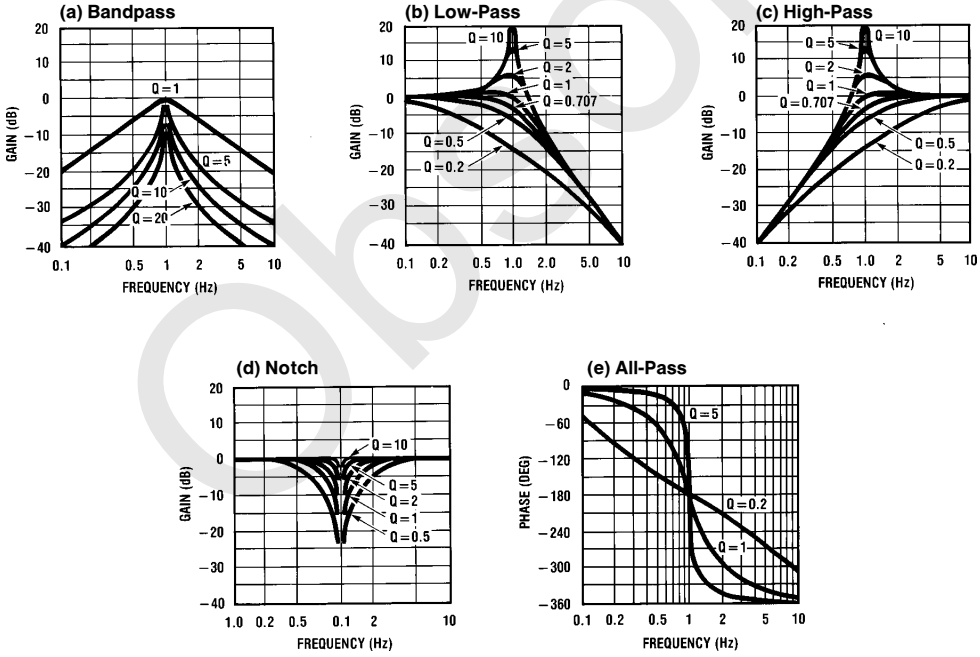


TL/H/5066–14

(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

FIGURE 5. 2nd-Order All-Pass Response



TL/H/5066–15

FIGURE 6. Responses of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

Obsolete

2.0 Modes of Operation

The MF5 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF5 closely approximates continuous filters, the following discussion is based on the well known frequency domain. Each MF5 can produce a full 2nd order function. See Table 1 for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_o$ **(See *Figure 7*)**

f_o = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = center frequency of the imaginary zero pair $= f_o$.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $f \rightarrow 0$, $f \rightarrow f_{CLK}/2$ $= \frac{-R_2}{R_1}$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$H_{OLP} = \frac{H_{OBP}}{Q}$ or $H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q.$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

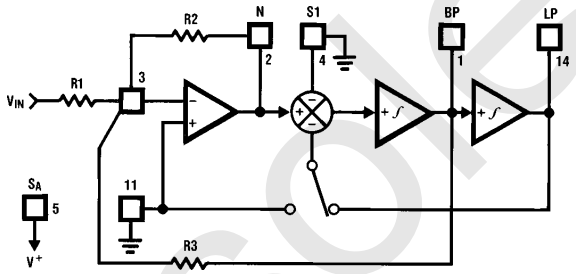
$H_{OLP} = -1$; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

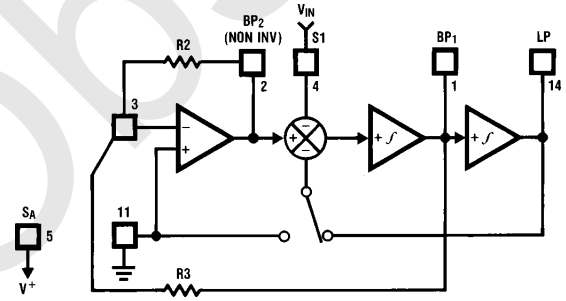
Circuit dynamics: $H_{OBP_1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ)



TL/H/5066–16

FIGURE 7. MODE 1



TL/H/5066–17

FIGURE 8. MODE 1a

Obsolete

2.0 Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_o$
(See *Figure 9*)

f_o = center frequency
$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$

$f_{notch} = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

Q = quality factor of the complex pole pair
$= \frac{\sqrt{R2/R4+1}}{R2/R3}$

H_{OLP} = Lowpass output gain (as $f \rightarrow 0$)
$= -\frac{R2/R1}{R2/R4+1}$

H_{OBP} = Bandpass output gain (at $f = f_o$) $= -R3/R1$

H_{ON_1} = Notch output gain (as $f \rightarrow 0$)
$= -\frac{R2/R1}{R2/R4+1}$

H_{ON_2} = Notch output gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = Q\sqrt{H_{ON_1}\,H_{ON_2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs
(See *Figure 10*)

$f_o = \frac{f_{CLK}}{100}\times\sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50}\times\sqrt{\frac{R2}{R4}}$

Q = quality factor of the complex pole pair
$= \sqrt{\frac{R2}{R4}}\times\frac{R3}{R2}$

H_{OHP} = Highpass gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

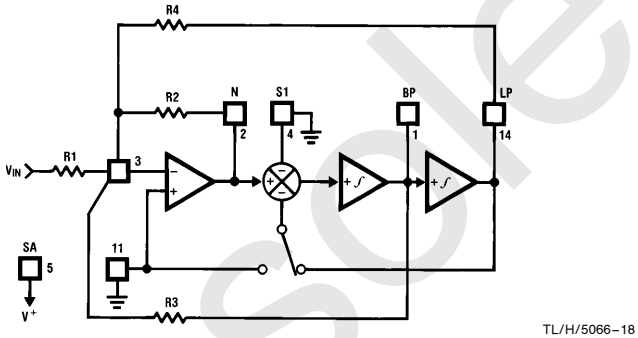
H_{OBP} = Bandpass gain (at $f = f_o$) $= -\frac{R3}{R1}$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R4}{R1}$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP}\times H_{OLP}}\times Q$

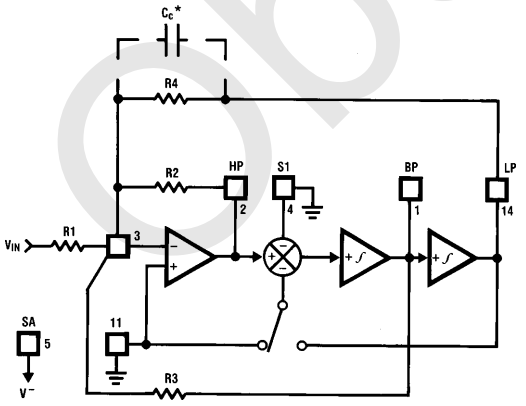
$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP(peak)} \cong Q \times H_{OHP}$ (for high Q's)



TL/H/5066–18

FIGURE 9. MODE 2



TL/H/5066–19

FIGURE 10. MODE 3

*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) across R4 to provide some phase lead.

Obsolete

2.0 Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op amp (See *Figure 11*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

f_n = notch frequency $= \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$

H_{on} = gain of notch at $f = f_o = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)\right\|$

H_{n1} = gain of notch (as $f \rightarrow 0$) $= \frac{R_g}{R_l} \times H_{OLP}$

H_{n2} = gain of notch $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$

MODE 4: Allpass, Bandpass, Lowpass Outputs (See *Figure 12*)

f_o = center frequency

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$;

f_z^* = center frequency of the complex zero pair $\cong f_o$

$$Q = \frac{f_o}{BW} = \frac{R3}{R2};$$

Q_z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

H^*_{OAP} = Allpass gain $\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$)

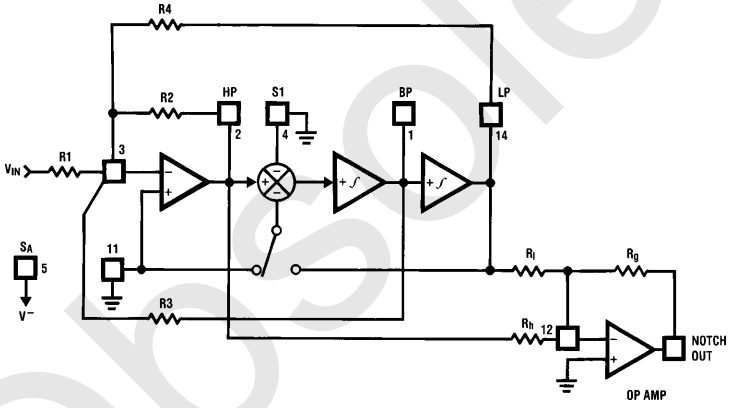
$$= -\left(\frac{R2}{R1} + 1\right) = -2$$

H_{OBP} = Bandpass gain (at $f = f_o$)

$$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

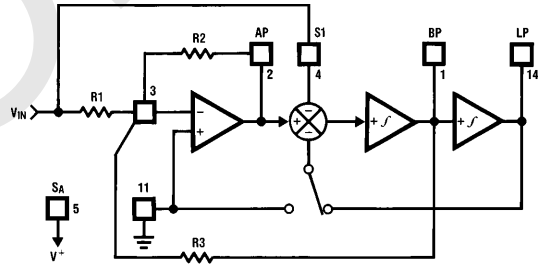
Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)\, Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.



TL/H/5066–20

FIGURE 11. MODE 3a



TL/H/5066–21

FIGURE 12. MODE 4

Obsolete

2.0 Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 13*)

$$f_o = \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1+R2/R4} \times \frac{R3}{R2}$$

$$Q_z = \sqrt{1-R1/R4} \times \frac{R3}{R1}$$

$$H_{0_{z1}} = \text{gain at C.Z. output (as } f \rightarrow 0 \text{ Hz)} = \frac{-R2\,(R4-R1)}{R1\,(R4+R2)}$$

$$H_{0_{z2}} = \text{gain at C.Z. output } \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$$

$$H_{OBP} = -\left(=\frac{R2}{R1}+1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2+R1}{R2+R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, HP, LP Filter (See *Figure 14*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

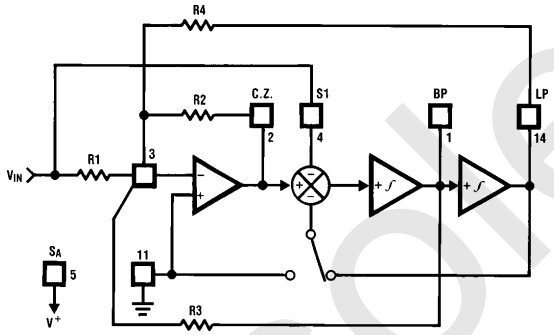
MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 15*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

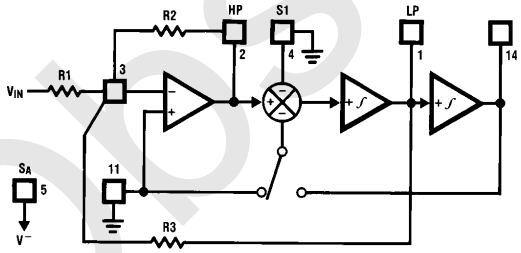
$$H_{OLP_1} = 1 \text{ (non-inverting)}$$

$$H_{OLP_2} = -\frac{R3}{R2}$$



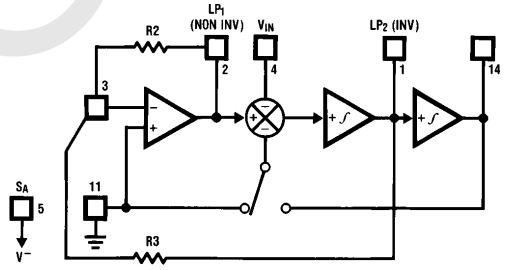
TL/H/5066–22

FIGURE 13. MODE 5



TL/H/5066–23

FIGURE 14. MODE 6a



TL/H/5066–24

FIGURE 15. MODE 6b

Obsolete

2.0 Modes of Operation (Continued)

TABLE I. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of resistors	Adjustable f_{CLK}/f_o	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} = +1$				2	No	May need input buffer. Poor dynamics for high Q.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4		Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3		Single pole.
6b		(2) $H_{OLP} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2		Single pole

3.0 Applications Information

The MF5 is a general-purpose second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). By connecting pin 9 to the appropriate DC voltage, the filter center frequency f_o can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_o can be very accurately set (within $\pm 0.6\%$) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_o ratio can be altered by external resistors as in *Figures 9, 10, 11, 13, 14*, and *15*. The filter Q and gain are determined by external resistors.

All of the five second-order filter types can be built using the MF5. These are illustrated in *Figures 1* through *5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF5s can be cascaded. The MF5 also includes an uncommitted CMOS operational amplifier for additional signal processing applications.

3.1 DESIGN EXAMPLE

An example will help illustrate the MF5 design procedure. For the example, we will design a 2nd order Butterworth low-pass filter with a cutoff frequency of 200 Hz, and a passband gain of -2. The circuit will operate from a ± 5V power supply, and the clock amplitude will be ± 5v (CMOS) levels).

From the specifications, the filter parameters are: $f_o = 200$ Hz, $H_{OLP} = -2$, and, for Butterworth response, $Q = 0.707$.

In section 2.0 are several modes of operation for the MF5, each having different characteristics. Some allow adjustment of f_{CLK}/f_o, others produce different combinations of filter types, some are inverting while others are non-inverting, etc. These characteristics are summarized in Table I. To keep the example simple, we will use mode 1, which has notch, bandpass, and lowpass outputs, and inverts the signal polarity. Three external resistors determine the filter's Q and gain. From the equations accompanying *Figure 7*, $Q = R_3/R_2$ and the passband gain $H_{OLP} = -R_2/R_1$. Since the input signal is driving a summing junction through R_1, the input impedance will be equal to R_1. Start by choosing a value for R_1. 10k is convenient and gives a reasonable input impedance. For $H_{OLP} = -2$, we have:

$R_2 = -R_1 H_{OLP} = 10k \times 2 = 20k$.

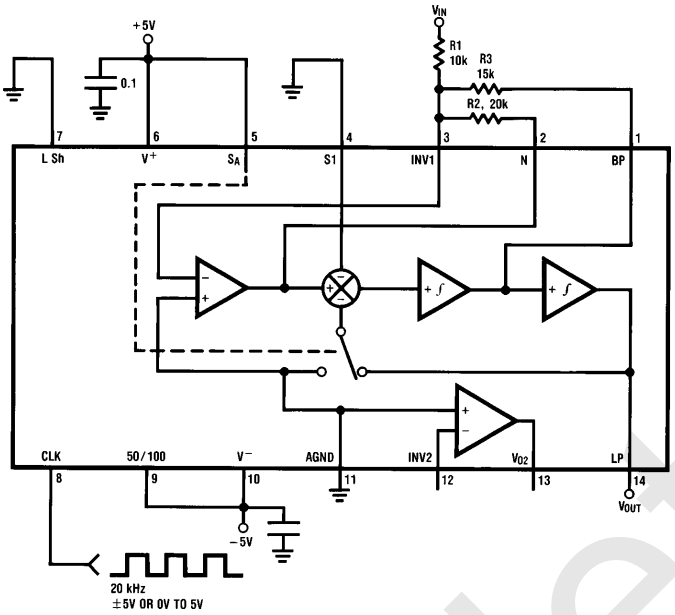
For $Q = 0.707$ we have:

$R_3 = R_2 Q = 20k \times 0.707 = 14.14k$. Use 15k.

For operation on ± 5V supplies, V^+ is connected to $+5$V, V^- to -5V, and AGND to ground. The power supplies should be ''clean'' (regulated supplies are preferred) and 0.1 μF bypass capacitors are recommended.

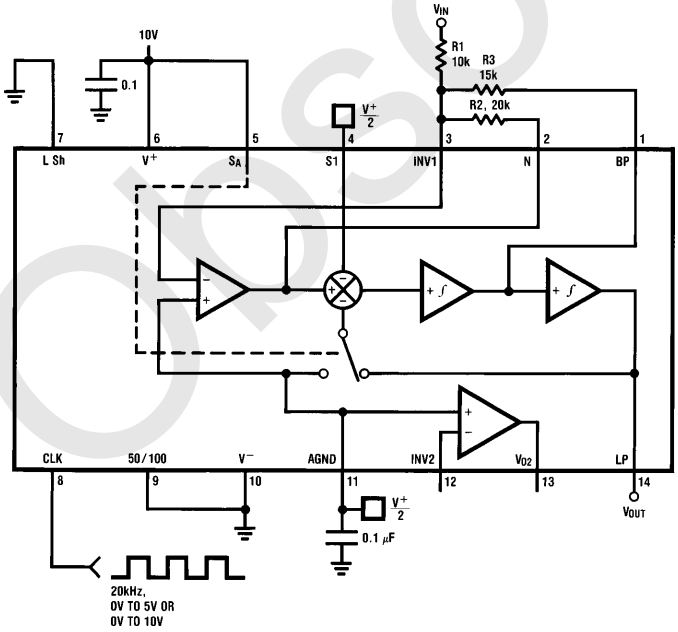
Obsolete

3.0 Applications Information (Continued)



TL/H/5066–25

FIGURE 16. 2nd-Order Butterworth Low-Pass Filter of Design Example. For $\frac{f_{CLK}}{f_0} = 50$, Connect Pin 9 to +5V, and Change Clock Frequency to 10 kHz.

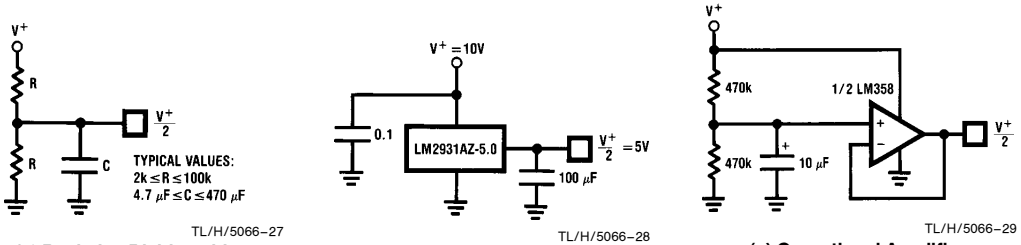


TL/H/5066–26

FIGURE 17. Butterworth Low-Pass Circuit of Example, but Designed for Single-Supply Operation

Obsolete

3.0 Applications Information (Continued)



(a) Resistive Divider with Decoupling Capaciter

(b) Voltage Regulator

(c) Operational Amplifier with Divider

FIGURE 18. Three Ways of Generating $\frac{V^+}{2}$ for Single-supply Operation

For a cutoff frequency of 200 Hz, the external clock can be either 10 kHz with pin 9 connected to V^+ (50:1) or 20 kHz with pin 9 tied to A_{GND} or V^- (100:1). The voltage on the Logic Level Shift pin (7) determines the logic threshold for the clock input. The threshold is approximately 2V higher than the voltage applied to pin 7. Therefore, when pin 7 is grounded, the clock logic threshold will be 2V, making it compatible with 0–5 volt TTL logic levels and ±5 volt CMOS levels. Pin 7 should be connected to a clean, low-impedance (less than 1000Ω) voltage source.

The complete circuit of the design example is shown for a 100:1 clock ratio in *Figure 16*.

3.2 SINGLE SUPPLY OPERATION

The MF5 can also operate with a single-ended power supply. *Figure 17* shows the example filter with a single-ended power supply. V^+ is again connected to the positive power supply (8 to 14 volts), and V^- is connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very ''clean'', as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (*Figure 18a*), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (*Figures 18b* and *18c*). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1μF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF5, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF5 are able to swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF5 is operating on ±5 volts, for example, the outputs will clip at about $8V_{p\text{-}p}$. The maximum input voltage multiplied by the filter gain should therefore be less than $8V_{p\text{-}p}$.

Note that if the filter has high Q, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (*Figure 6*). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_o. If the nominal gain of the filter H_{OLP} is equal to 1, the gain at f_o will be 10. The maximum input signal at f_o must therefore be less than 800 $mV_{p\text{-}p}$ when the circuit is operated on ±5 volt supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (*Figure 7*). The notch output will be very small at f_o, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_o and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figures 7* through *15* are equations labeled ''circuit dynamics'', which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The MF5's switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. *Figure 19* shows an equivalent circuit of the MF5 from which the output dc offsets can be calculated. Typical values for these offsets are:

V_{os1} = opamp offset = ±5mV

V_{os2} = −185mV @ 50:1 −310mV @ 100:1

V_{os3} = +115mV @ 50:1 +240mV @ 100:1

The dc offset at the BP output is equal to the input offset of the lowpass integrator (V_{os3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

3.0 Applications Information (Continued)

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{Rp} + 1\right) V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1+R4/R2} - \frac{V_{OS3}}{Q\sqrt{1+R2/R4}}:$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

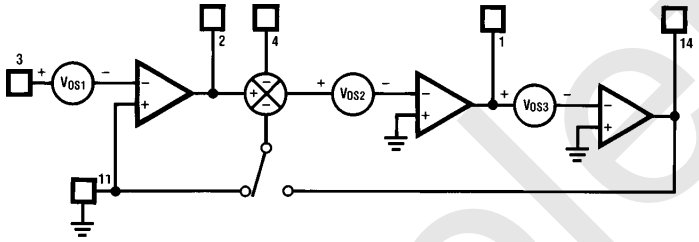
$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

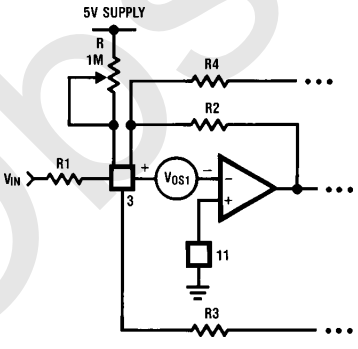
$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2}\left(\frac{R2}{R3}V_{OS3} + V_{OS2}\right) + -\frac{R4}{R2}\left(1 + \frac{R2}{R_p}\right) V_{OS1};\ R_p = R1//R3//R4$$



TL/H/5066–30

FIGURE 19. Block Diagram Showing MF5 Offset Voltage Sources



TL/H/5066–31

FIGURE 20. Method for Trimming V_{OS}, See Text, Section 3.4

Obsolete

3.0 Applications Information (Continued)

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower ac signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_o and Q. When operating in Mode 3, offsets can become excessively large if R_2 and R_4 are used to make f_{CLK}/f_o significantly higher than the nominal value, especially if Q is also high. An extreme example is a bandpass filter having unity gain, a Q of 20, and $f_{CLK}/f_o = 250$ with pin 9 tied to V^- (100:1 nominal). R_4/R_2 will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about +1.9V. Where necessary, the offset voltage can be adjusted by using the circuit of *Figure 20*. This allows adjustment of V_{os1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{os(BP)}$ in modes 1a and 3, for example).

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

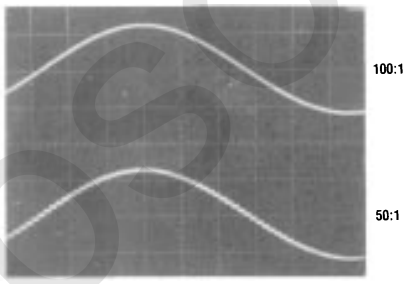
The MF5 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF5's sampling frequency is the same as its clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be ''reflected'' to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 100$ Hz will cause the system to respond as though the input frequency was $f_s/2$ - 100 Hz. This phenomenon is known as ''aliasing'', and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF5 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in ''steps'' in the output voltage which occur at the clock rate. (*Figure 21*) If necessary, these can be ''smoothed'' with a simple R-C low-pass filter at the MF5 output.

The ratio of f_{CLK} to f_c (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in 3.4.

The accuracy of the f_{CLK}/f_o ratio is dependent on the value of Q. This is illustrated in the curves under the heading ''Typical Performance Characteristics''. As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_o will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of Q and f_o should be limited to 300 kHz when $f_o < 5$ kHz, and to 200 kHz for $f_o > 5$ kHz.

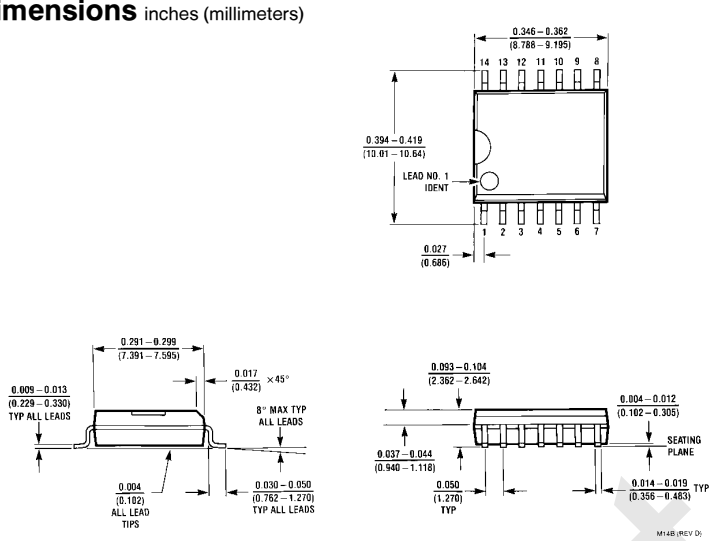


TL/H/5066–32

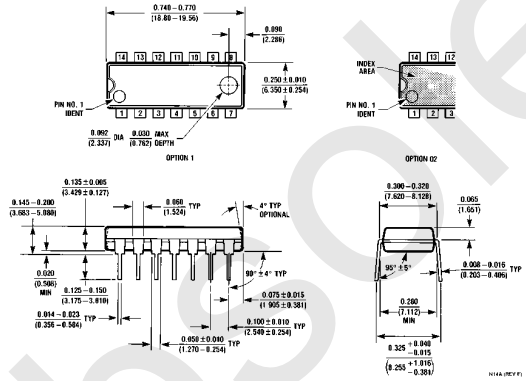
FIGURE 21. The Sampled-Data Output Waveform

Obsolete

Physical Dimensions inches (millimeters)



SO Package
Order Number MF5CWM
NS Package Number M14B



Molded Dual-In-Line Package (N)
Order Number MF5CN
NS Package Number N14A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

Obsolete

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated