

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

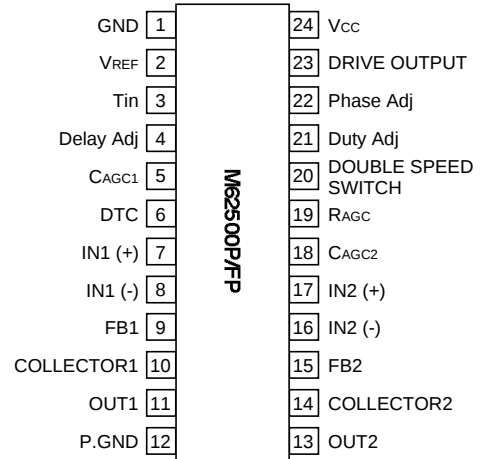
DESCRIPTION

The M62500 is a semiconductor integrated circuit designed and developed as a deflection control of the CRT display monitor. The built-in trigger mode oscillator allows stable PWM control to be gained against a wide range of change of external signals. The M62500 provides a low supply voltage output malfunction preventive circuit (UVLO) and software start function optimum to horizontal output correction of monitor, high voltage drive and high voltage regulator.

FEATURES

- PWM output in synchronization with external signals
- Wide range of PWM control frequency
15kHz to 150kHz
- The PWM output phase is adjustable against external signals
- Soft start
- Built-in low voltage output malfunction prevention circuit
Start $V_{CC} > 9V$
Stop $V_{CC} < 6V$

PIN CONFIGURATION (TOP VIEW)

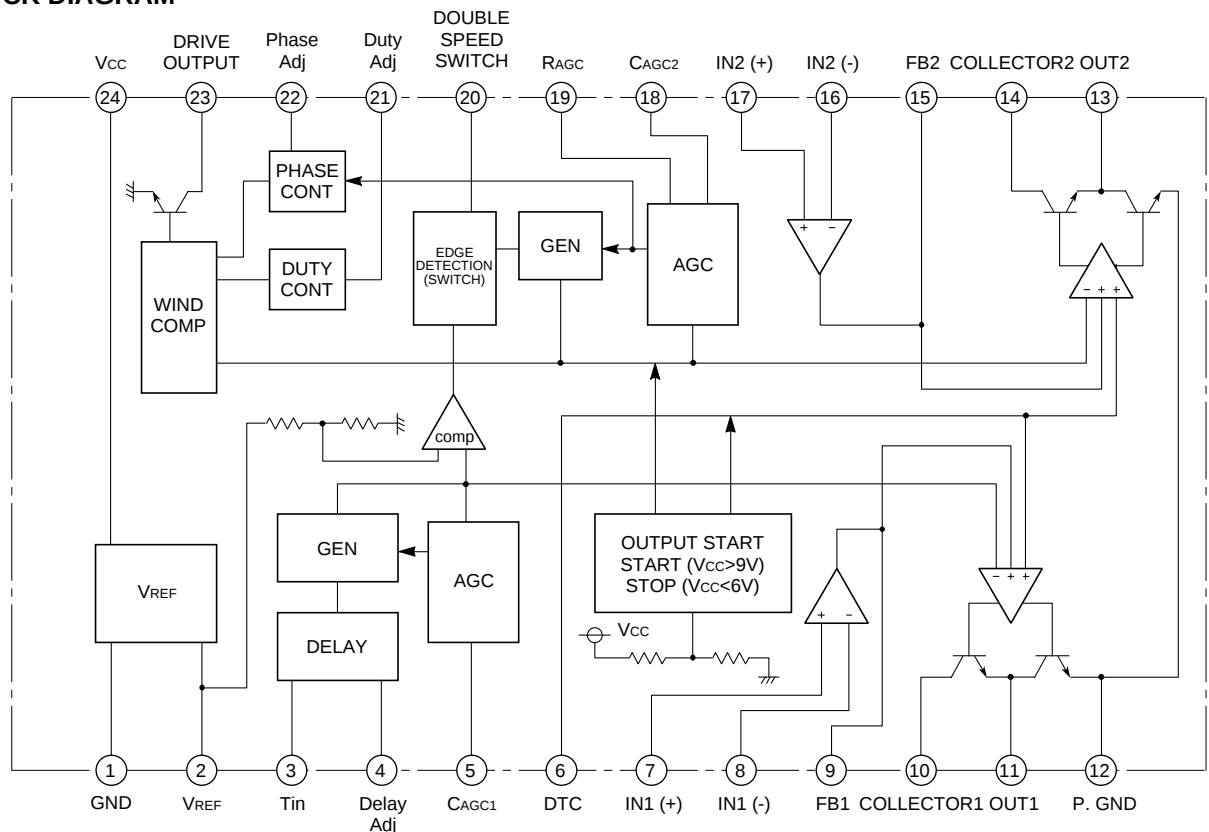


Outline 24P4D (P)
24P2V-A (FP)

APPLICATION

CRT display monitor

BLOCK DIAGRAM



SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Ratings		Unit
V _{CC}	Supply voltage	15		V
V _{OUT}	Output voltage	15		V
I _{OUT}	Output current	±150		mA
V _d	Drive output voltage	15		V
I _d	Drive output current	20		mA
V _{ICM}	Common mode input voltage range of error amplifier	-0.3 to V _{CC}		V
V _{ID}	Common mode differential input voltage of error amplifier	V _{CC}		V
P _d	Power dissipation	P	FP	mW
		1400	1000	
K _θ	Thermal derating	P	FP	mW/°C
		11.2	8	
T _{opr}	Operating temperature	-20 to +75		°C
T _{stg}	Storage temperature	-40 to +125		°C

Note. For the polarity of current, the direction in which current flows to the IC is specified positive (+), while the direction in which current flows out from the IC is specified to be negative (-).

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

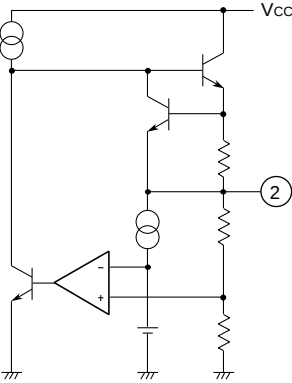
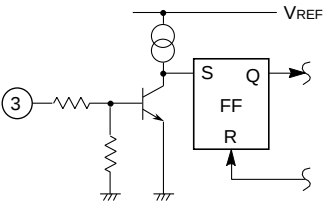
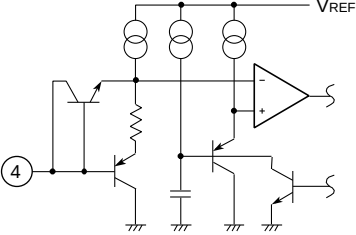
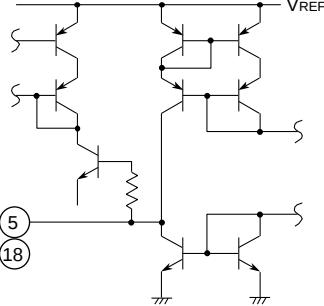
ELECTRICAL CHARACTERISTICS ($V_{CC}=12V$, $f_{IN}=40kHz$, $T_a=25^{\circ}C$, unless otherwise noted)

Block	Symbol	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
Supply voltage	V _{CC}	Range of power supply voltage		V _{CC} off		14	V
	I _{CC}	Dissipation current	Without signal	20	40	70	mA
	V _{CC} ON	Activation start voltage		8	9	10	V
	V _{CC} OFF	Activation stop voltage		5.4	6.0	6.6	V
Error amp. section	V _{IO}	Input offset voltage				7	mV
	I _{IB}	Input bias voltage		-100			nA
	I _{IO}	Input offset current		-100		100	nA
	V _{ICM}	Common mode input range		-0.3		V _{CC} -2	V
	A _V	Open loop gain		70	110		dB
	S _R	Through rate			4		V/μs
	V _{OR}	Output voltage range 1)		0.3		V _{REF} -1.5	V
	I _{SINK}	Output sink current		10			mA
	I _{SOURCE}	Output source current				-10	mA
	V _{SATL}	Output saturation voltage L	I _O =100mA		0.7	1.4	V
PWM output section	V _{SATH}	Output saturation voltage H	I _O =-100mA	9.5	10.5		V
	V _{REF}	Reference voltage	I _{REF} =-5mA	4.80	5.00	5.20	V
	Reg-in	Input stability	V _{CC} =7 to 14V I _{REF} =-5mA		1	10	mV
	Reg-L	Load voltage	I _{REF} =0 to -5mA		2	20	mV
	T _{CVREF}	Temperature coefficient of reference voltage	T _a =-20 to +75°C		0.01		%/°C
	I _{REF} MAX	Maximum reference current			-40		mA
	I _S	Short-circuit current			-70		mA
	I _{IN}	Input current	V _{IN} =5V	—	140	200	μA
	V _{IN} L	"L" input voltage		—	—	0.6	V
	V _{IN} H	"H" input voltage		2.0	—	—	V
Delay adj section	I _{Delay}	Input current		-0.6	-0.1	—	μA
	T _D min	Minimum delay time	V _{Delay} adj=0V	—	0.8	1	μs
	T _D max	Maximum delay time	V _{Delay} adj=3.0V	10	15	—	μs
	I _{DTC}	Input current		—	0.5	2.0	μA
PWM comp section	V _{th} U	Upper limit voltage of saw tooth wave		0.65V _{REF}	0.7V _{REF}	0.75V _{REF}	V
	V _{th} L	Lower limit voltage of saw tooth wave		0.28V _{REF}	0.3V _{REF}	0.32V _{REF}	V
	T _{Duty}	PWM output duty	V _{DTC} =2.5V	45	50	55	%
	I _{Duty}	Input current	V _{Duty} adj=2.5V	-6.5	-1.3	—	μA
Duty adj section	Duty min	Minimum duty		—	10	20	%
	Duty max	Maximum duty		80	95	—	%
	Duty	Duty	V _{Duty} adj=2.5V	45	50	55	%
	I _{Phase}	Input current	V _{Phase} adj=2.5V	-3.5	-0.7	—	μA
Phase adj section	T ₂ min	Minimum leading time of drive output		—	0.7	1.6	μs
	T ₂ max	Minimum leading time of drive output		9	9.4	—	μs
	T ₂	Leading time of drive output	V _{Phase} adj=1.0V	4.5	5.5	7.0	μs
	V _{SAT} D	Output saturation voltage	I _D =10mA			0.4	V
Drive output section	I _{LD}	Output leak current	V _{DO} =12V			1	μA
	I _{fh}	fh pin current	V _{fh} =5V	—	330	430	μA
	V _{fh}	fh switching voltage		0.4V _{REF}	0.5V _{REF}	0.6V _{REF}	V

Note 1. Output must not be reversed with input of 0.

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

EXPLANATION OF TERMINALS

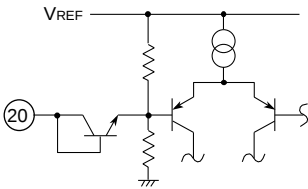
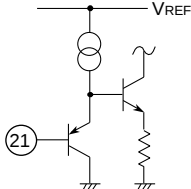
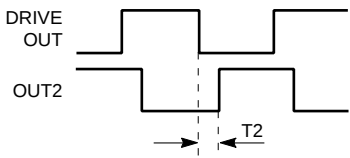
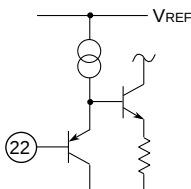
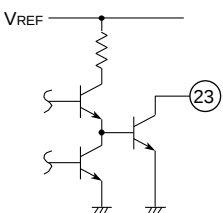
Pin No.	Symbol	Function and peripheral circuit of pins
①	GND	GND
②	VREF	5.0V reference voltage External load of about 5mA can be taken out. 
③	Tin	Trigger input Read at the rising edge  
④	Delay Adj	Delay adjustment Delay of read trigger signal Vdelay : 0 to 3.0V Tdelay : 1μ to 10μsec 
⑤ ⑱	CAGC1 CAGC2	AGC capacitance Connects capacitance between each pin and GND and sets up AGC sensitivity 

EXPLANATION OF TERMINALS (Cont.)

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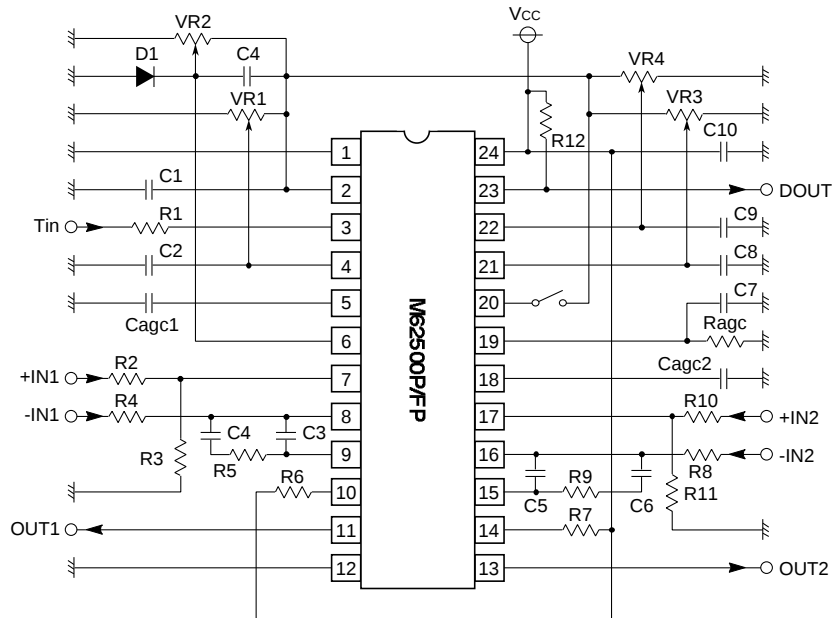
SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

EXPLANATION OF TERMINALS (Cont.)

Pin No.	Symbol	Function and peripheral circuit of pins
⑳	fh/2fh	Double speed switch Switches frequency of OUT2 and drive output to the double frequency. OPEN, GND → fh VREF → 2fh 
㉑	Duty Adj	Duty adjustment of drive output 
㉒	Phase Adj	Phase adjustment of drive output against OUT2 (T2)  
㉓	DRIVE OUTPUT	Open collector output 
㉔	Vcc	Supply terminal

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

APPLICATION EXAMPLE



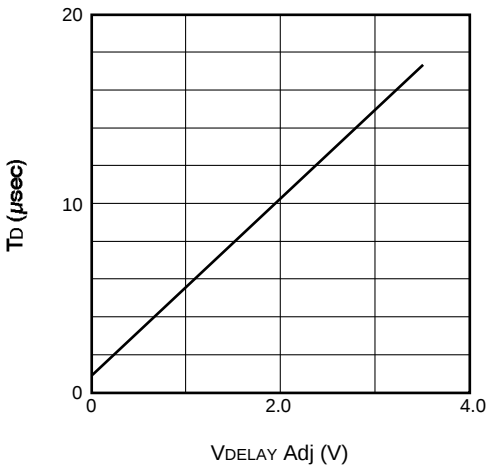
C1, C10	: Is required for stabilization of Vcc and VREF. Is normally set to tens of μF to hundreds of μF .	R2, R3, R10, R11	: A gain setup constant of error Amp. To assure the stability of feedback, R4 and R8 shall be set to several kW to tens of kW to set the gain to approx. 20dB to 40dB with $f=1$ kHz. If the gain is too low, jitter may take place. It is therefore recommended to set C3 and C5 to tens of pF to hundreds of pF, C4 and C6 to thousands of pF to tens of thousands of pF, and R5 and R9 to tens of kW to hundreds of kW.
VR 1, 2, 3, 4	: Is determined taking into account the load capability of VREF. (External load capability of approx. 5mA) Shall be normally set to approx. 10kW.	R4, R5, R8, R9	
C2, C8, C9	: Is added to high impedance pin of voltage control for improvement in noise margin. Depends on the device installation environment. Shall be normally set to approx. 0.1 μF .	C3, C4, C5, C6	
C4, D1	: Is added for the execution of software start. Set a time constant, taking into account the set value of VR2.	C7	: If f to be input into Tin suddenly changes, addition of C7 shortens non-control time of Dout (output of "H"). As a capacitance value, it is recommended to adopt 2.2 μF . In the case of adding C7, however, $Cagc2 \geq 0.68\mu\text{F}$ is recommended.
R1	: Is added to reduce interference by Tin and outputs. With VIN=approx. 2.5V to 5V, the resistance value of approx. 22kW is recommended.	R6, R7	: Current limit resistance of OUT1/2. Is normally set to several W. Insertion of direct limit resistance into OUT1/2 pin is also effective.
Cagc 1, 2	: Capacitance necessary for stabilization of AGC. As the capacitance is larger, the stability is larger, but the characteristic of answering becomes worse. The capacitance value of 1 μF is recommended.	R12	: Pull-up resistance of DOUT output. DOUT is an open collector output and requires R12. Is normally set to several kW.
		Ragc	: Resistance for setting AGC on the OUT2 side. Is set with $Ragc=27\text{kW}$.

* Note: To reduce interference in the signal system, pins ① GND and ⑫ P.GND shall be grounded at a point in the power supply block.

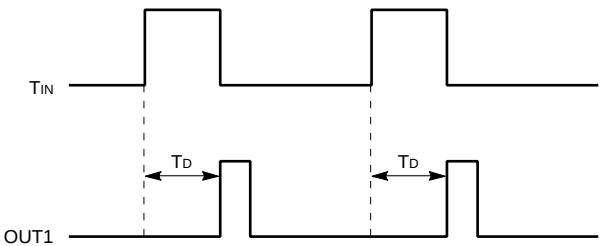
SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

SETUP OF VOLTAGE CONTROL BLOCK

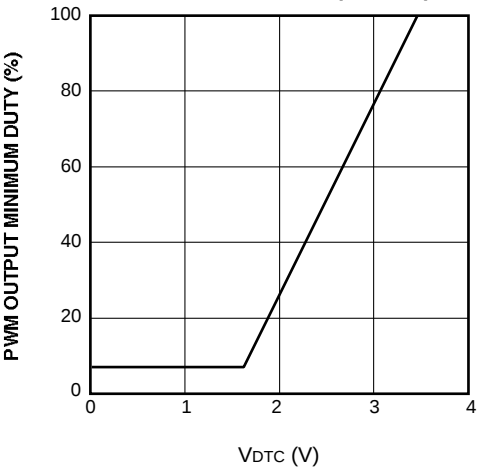
T_D vs. V_{DELAY Adj} CHARACTERISTICS (f=40kHz)



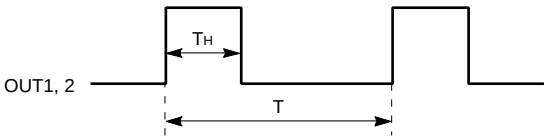
Applying a voltage to the DELAY Adj pin can control the delay time of OUT1 to T_{IN}.



PWM OUTPUT MINIMUM DUTY vs. V_{DTC} CHARACTERISTICS (f=40kHz)



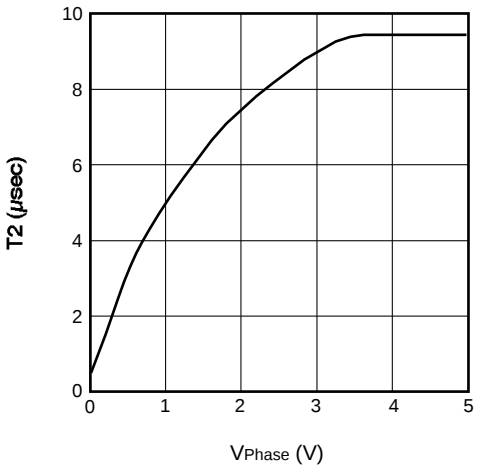
Applying a voltage to the DTC pin can control the dead time of PWM output.



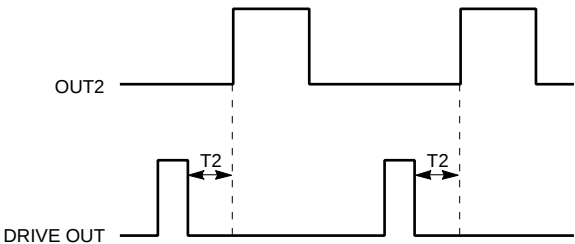
PWM output minimum duty

$$T_{DUTY} = \frac{T_H}{T} \times 100 (\%)$$

T₂ vs. V_{Phase} CHARACTERISTICS (f=40kHz)

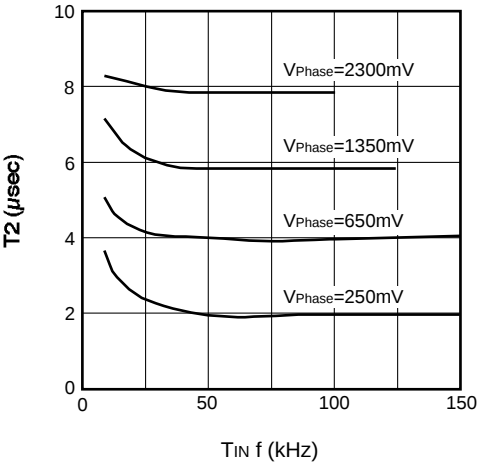


Applying a voltage to the Phase Adj pin can control a leading time of drive output to OUT2.

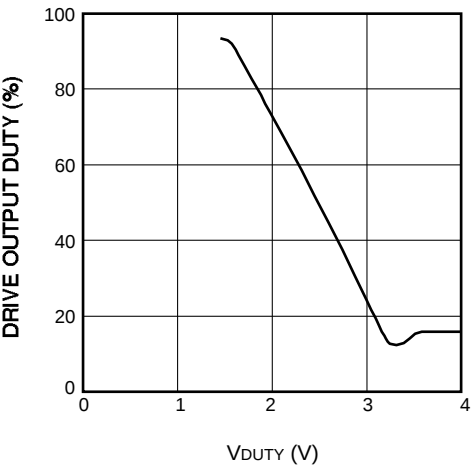


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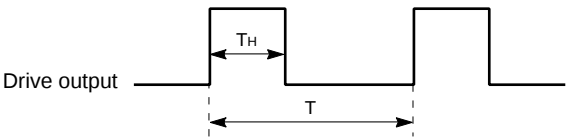
T2 vs. f CHARACTERISTICS



DRIVE OUTPUT DUTY vs. V_{DUTY} CHARACTERISTICS (f=40kHz)



Applying a voltage to the DUTY Adj pin can control drive output duty.

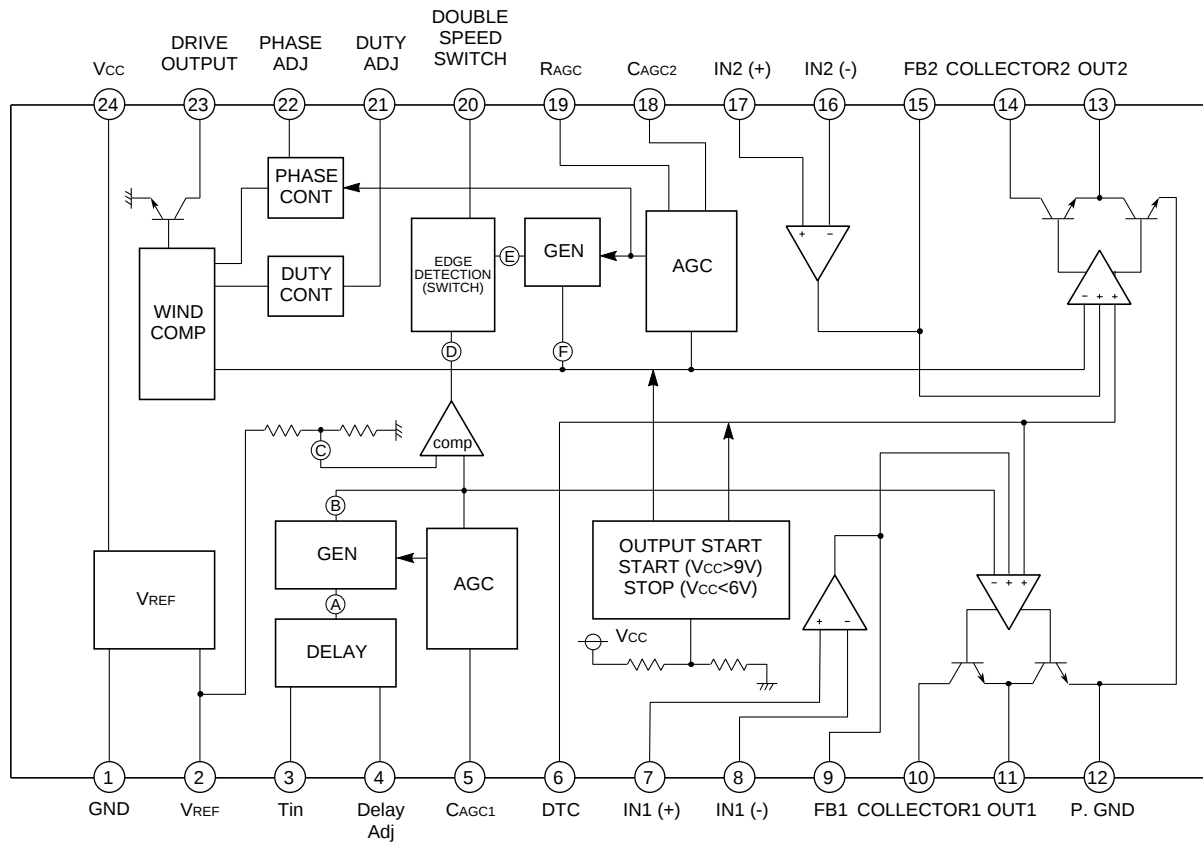


Drive output duty

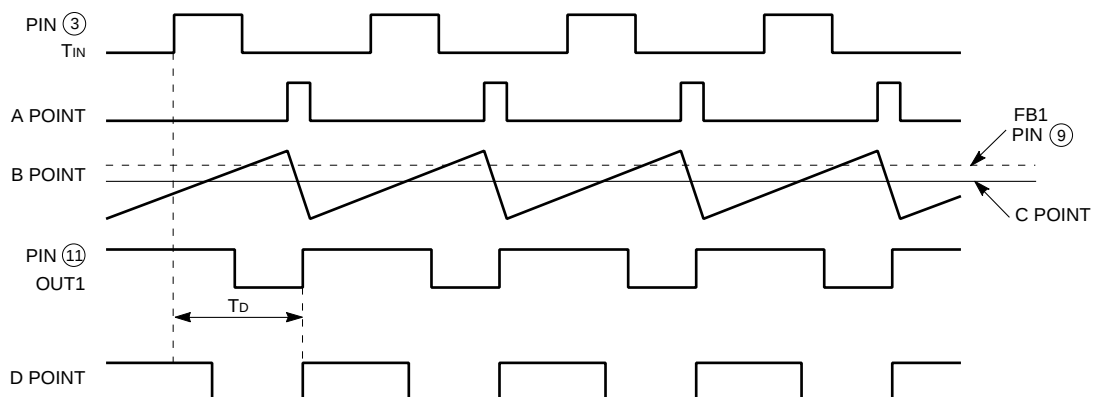
$$T_{DUTY} = \frac{T_H}{T} \times 100 (\%)$$

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

TIME CHART

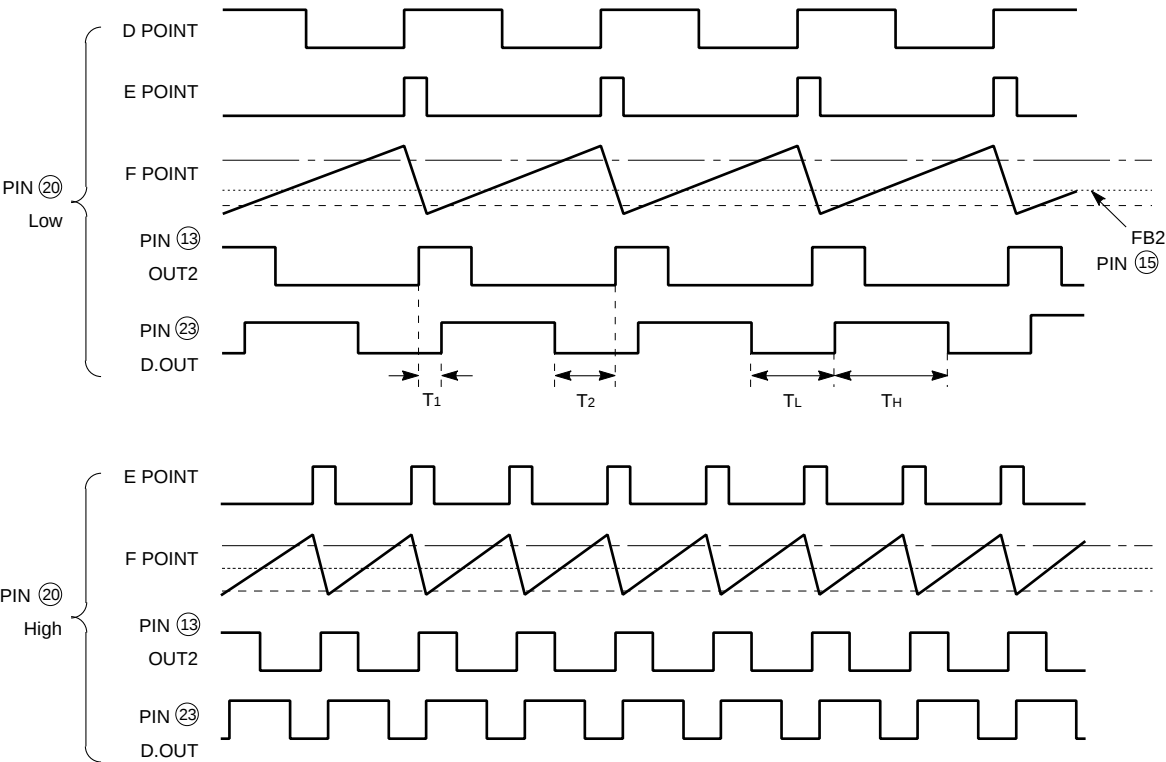


PIN WAVE



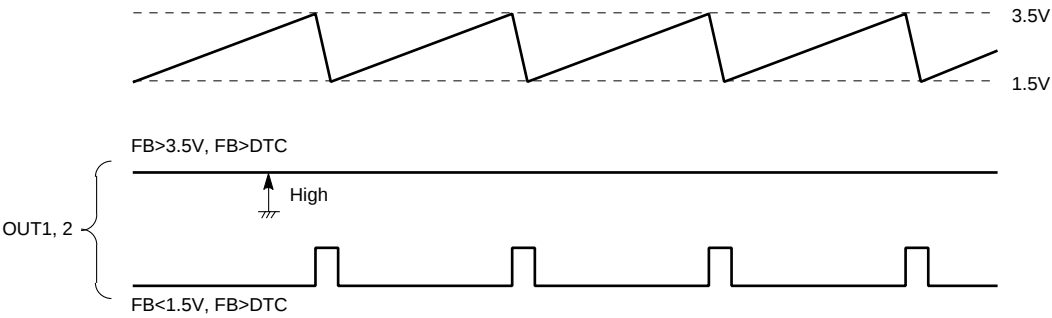
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PIN WAVE (Cont.)



PWM OUT NON-CONTROL STATUS

With trigger input at pin 3



Without trigger at pin 3 (in case of GND)

