Integrated Device Technology, Inc.

3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

IDT74FCT163601/A
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

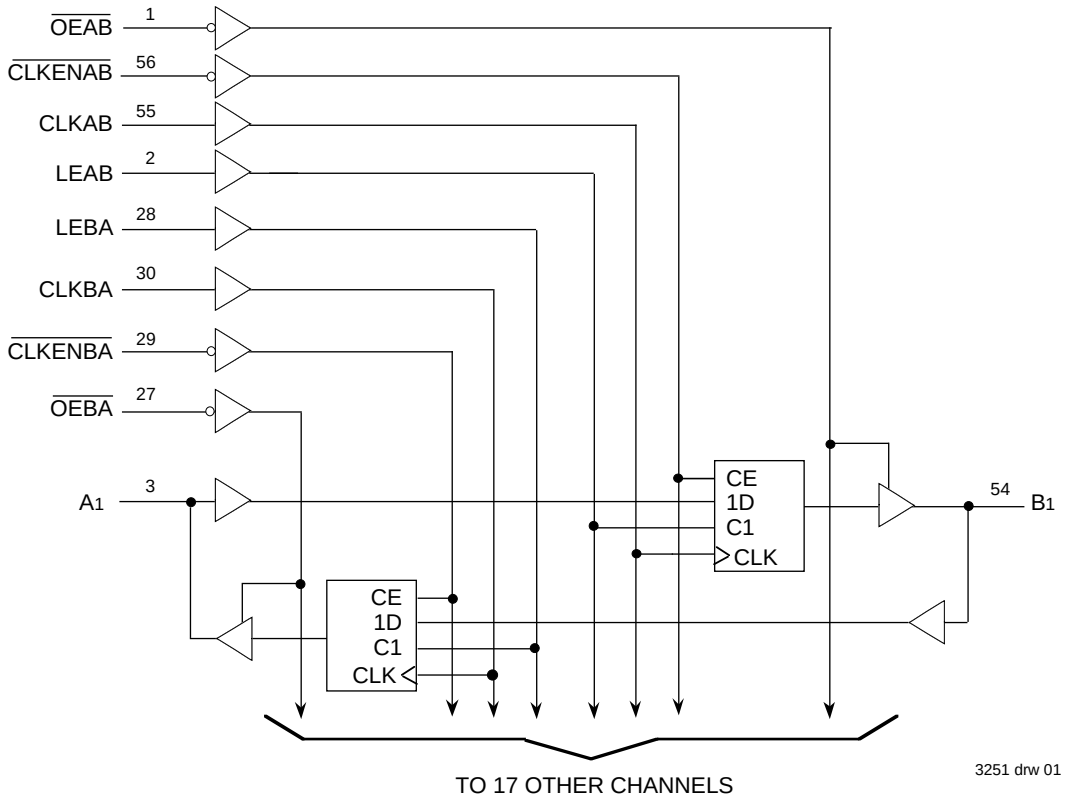
The FCT163601/A 18-bit registered transceiver is built using advanced dual metal CMOS technology. These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

The FCT163601 has series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

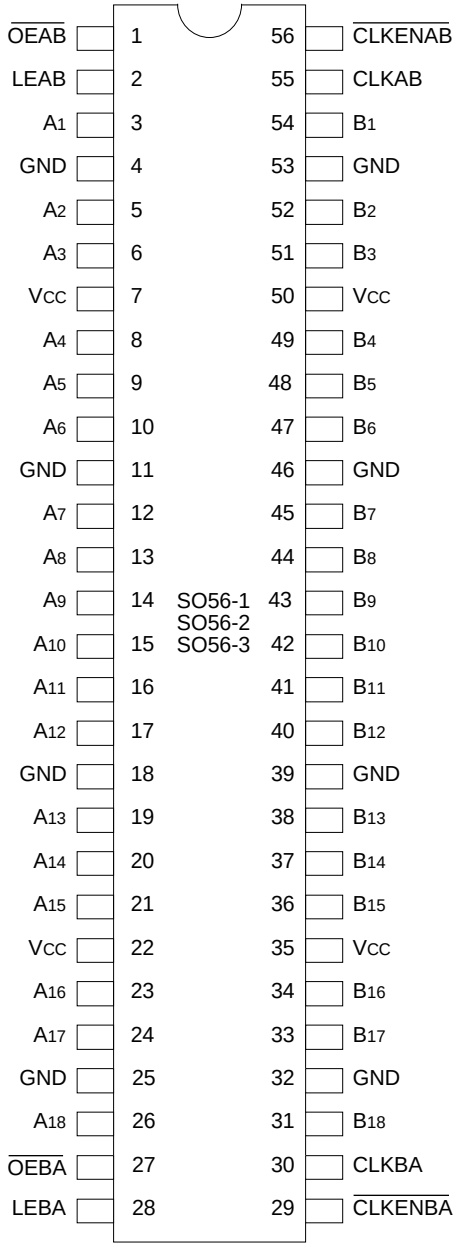
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATIONS



SSOP
TSSOP/TVSOP
TOP VIEW

3251 drw 02

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
$\overline{CLKENAB}$	A to B Clock Enable Input (Active LOW)
$\overline{CLKENBA}$	B to A Clock Enable Input (Active LOW)

3251 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 3251 lnk 04
1. This parameter is measured at characterization but not tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	mA

NOTES: 3251 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

FUNCTION TABLE(1,4)

Inputs					Outputs
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B0(2)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B0(2)
L	L	L	H	X	B0(3)

NOTES: 3251 tbl 02
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	10	µA

NOTES:

3251 lnk 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = V_{CC} - 0.6V$[3]		—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OEAB}$ = V_{CC} $\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (CLKBA) 50% Duty Cycle $\overline{OEAB}$ = V_{CC} $\overline{OEBA}$ = GND LEBA = GND $\overline{CLKENBA}$ = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	0.6	1.0	mA
			$V_{IN} = V_{CC} - 0.6$ V_{IN} = GND	—	0.6	1.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz (CLKBA) 50% Duty Cycle $\overline{OEAB}$ = V_{CC} $\overline{OEBA}$ = GND LEBA = GND $\overline{CLKENBA}$ = GND Eighteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	3.0	5.0[5]	
			$V_{IN} = V_{CC} - 0.6$ V_{IN} = GND	—	3.0	5.3[5]	

3251 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Condition[1]	FCT163601		FCT163601A		Unit
				Min.[2]	Max.	Min.[2]	Max.	
f_{MAX}	CLKAB or CLKBA frequency[4]		C_L = 50pF	—	100	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Bx to Ax		R_L = 500Ω	1.5	6.5	1.5	5.5	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	7.2	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	7.3	1.5	6.3	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx			1.5	7.5	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx			1.5	6.5	1.5	5.2	ns
t_{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA			4.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	ns
t_{SU}	Set-up Time HIGH or LOW	Clock LOW		2.5	—	2.5	—	ns
	Ax to LEAB, Bx to LEBA	Clock HIGH		2.0	—	2.0	—	ns
t_{SU}	Set-up Time, $\overline{CLKEN}$ to CLK			3.0	—	2.5	—	ns
t_H	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.0	—	ns
t_H	Hold Time, $\overline{CKLEN}$ after CLK			0	—	0	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[4]			3.0	—	2.5	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[4]			3.0	—	3.0	—	ns
$t_{SK}(o)$	Output Skew[3]			—	0.5	—	0.5	ns

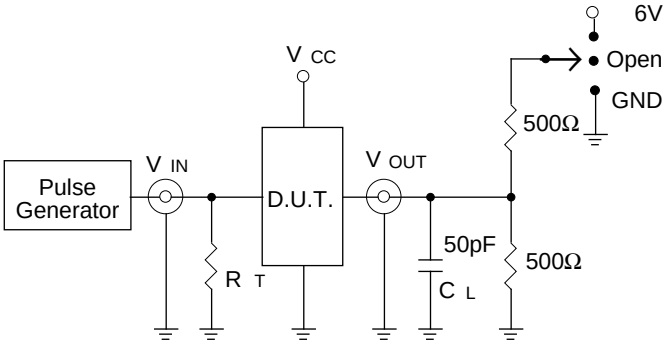
NOTES:

3251 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3251 lnk 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

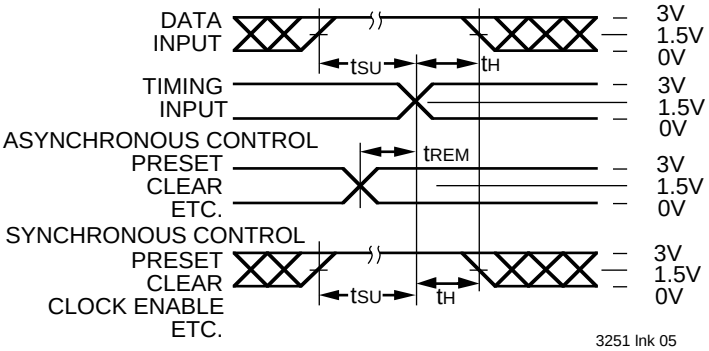
3251 tbl 08

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

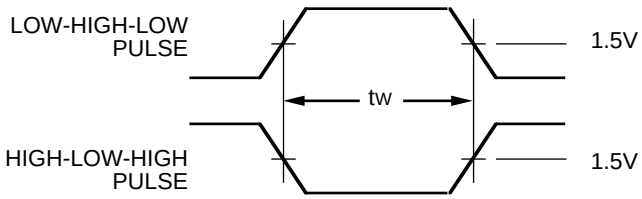
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



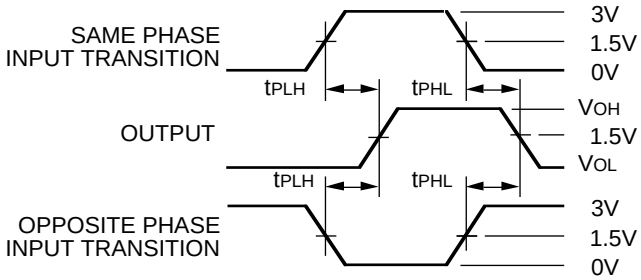
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PULSE WIDTH



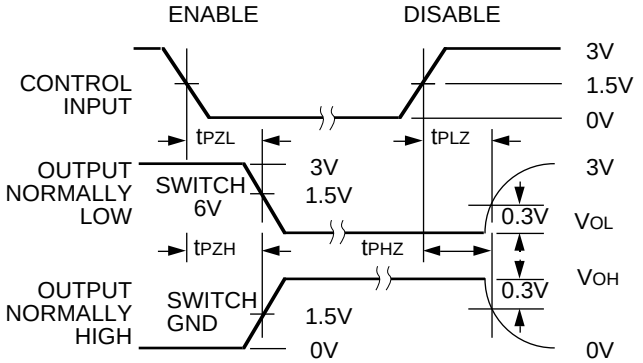
3251 lnk 06

PROPAGATION DELAY



3251 lnk 07

ENABLE AND DISABLE TIMES



3251 lnk 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION

