DS96F172MQML,DS96F174MQML

DS96F172MQML/DS96F174MQML EIA-485/EIA-422 Quad Differential Drivers



Literature Number: SNOSAS8

National Semiconductor

DS96F172MQML/ DS96F174MQML

April 28, 2011

EIA-485/EIA-422 Quad Differential Drivers

General Description

The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA-485 Standards. The DS96F172 and the DS96F174 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F172 and DS96F174 to operate at higher speeds while minimizing power consumption.

The DS96F172 and the DS96F174 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

Features

- Meets EIA-485 and EIA-422 standards
- Monotonic differential output switching
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7.0V to +12V
- Operates from single +5.0V supply
- Reduced power consumption
- Thermal shutdown protection
- DS96F172 and DS96F174 are lead and function compatible with the SN75172/174 or the AM26LS31/ MC3487

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS96F172ME/883	5962-9076501M2A	E20A	20LD Leadless Chip Carrier
DS96F172MJ/883	5962-9076501MEA	J16A	16LD Ceramic Dip
DS96F174ME/883	5962-9076502M2A	E20A	20LD Leadless Chip Carrier
DS96F174MJ/883	5962-9076502MEA	J16A	16LD Ceramic Dip
DS96F174MJ-QMLV	5962-9076502VEA	J16A	16LD Ceramic Dip

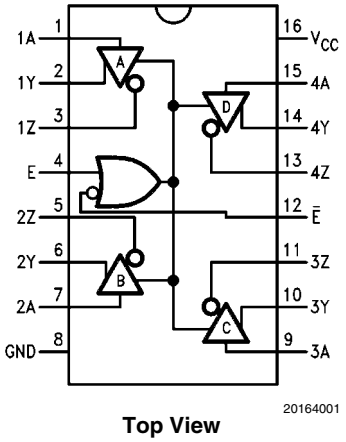
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Connection Diagrams

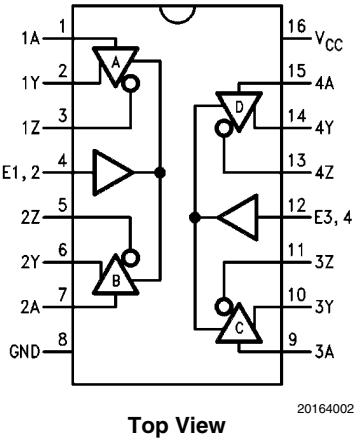
16-Lead Ceramic Dual-In-Line Package (NS Package Number J16A)

DS96F172



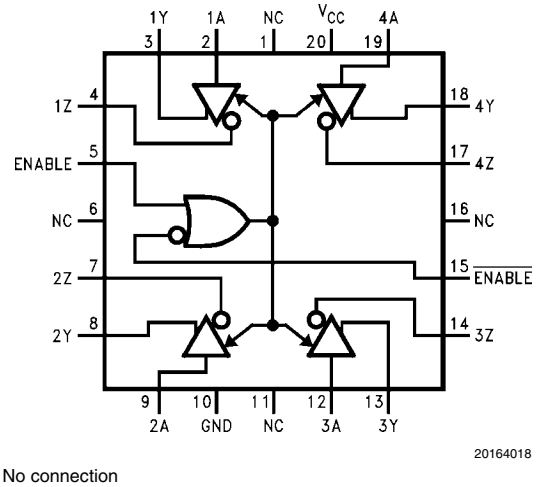
Top View

DS96F174



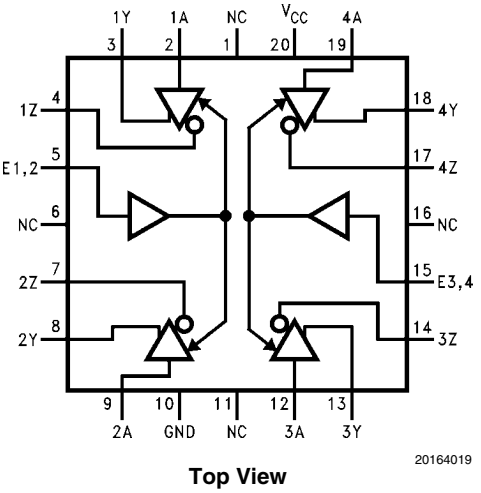
Top View

20-Lead Ceramic Leadless Chip Carrier (NS Package Number E20A)



NC = No connection

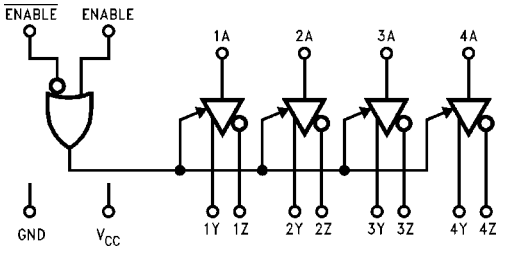
Top View



Top View

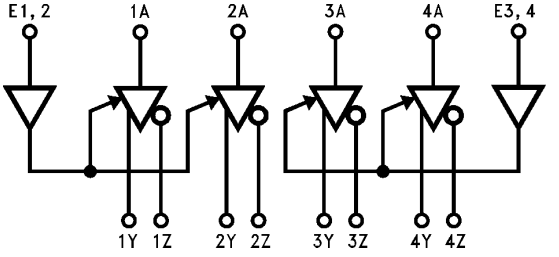
Logic Diagrams

DS96F172



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DS96F174



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Function Tables

DS96F172

(Each Driver)

Input	Enable		Outputs	
A	**E**	**$\overline{E}$**	**Y**	**Z**
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96F174

Input	Enable	Outputs	
A	**E**	**Y**	**Z**
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

Absolute Maximum Ratings (*Note 1*)

Storage Temperature Range (T_{Stg})	$-65°C \leq T_A \leq +175°C$
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation at 25°C (*Note 2*)	
Ceramic LCC (E)	2,000 mW
Ceramic DIP (J)	1,800 mW
Ceramic Flatpak (W)	1,000 mW
Supply Voltage	7.0V
Enable Input Voltage	5.5V

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Common Mode Output Voltage (V_{OC})	−7.0	+12.0	V
Output Current High (I_{OH})		−60	mA
Output Current Low (I_{OL})		60	mA
Operating Temperature (T_A)	−55	+125	°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS96F172/DS96F174 Electrical Characteristics

AC/DC Parameters (*Note 5*)

The following conditions apply, unless otherwise specified.

DC: V_{CC} = 5.5V

AC: V_{CC} = 5.0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IL}	Logical 0 Input Voltage				0.8	V	1
					0.7	V	2, 3
V_{IH}	Logical 1 Input Voltage			2.0		V	1, 2, 3
V_{IC}	Input Clamp Voltage	I = -18mA		-1.5		V	1, 2, 3
V_{OD1}	Differential Output Voltage	I_O = 0mA			6.0	V	1, 2, 3
V_{OD2}	Differential Output Voltage	V_{CC} = 4.5V, R_L = 54Ω *Figure 1*		1.5		V	1, 2
			(*Note 3*)	1.2		V	3
V_{OD2}	Differential Output Voltage	V_{CC} = 4.5V, R_L = 100Ω *Figure 1*		2.0		V	1, 2, 3
ΔV_{OD1}	Change In Magnitude of V_{OD2}	V_{CC} = 4.5V, R_L = 54Ω	(*Note 6*)	-200	200	mV	1, 2
			(*Note 3*, *Note 6*)	-400	400	mV	3
ΔV_{OD2}	Change In Magnitude of V_{OD2}	V_{CC} = 4.5V, R_L = 100Ω	(*Note 6*)	-200	200	mV	1, 2
			(*Note 3*, *Note 6*)	-400	400	mV	3
V_{OC}	Common Mode Output Voltage	R_L = 54Ω *Figure 1*			3.0	V	1, 2, 3
V_{OC}	Common Mode Output Voltage	R_L = 100Ω *Figure 1*			3.0	V	1, 2, 3
ΔV_{OC}	Change in Magnitude of V_{OC}	V_{CC} = 4.5V, R_L = 54Ω *Figure 1*	(*Note 6*)	-200	200	mV	1, 2, 3
ΔV_{OC}	Change in Magnitude of V_{OC}	V_{CC} = 4.5V, R_L = 100Ω *Figure 1*	(*Note 7*)	-200	200	mV	1, 2, 3
I_O	Output Current With Power Off	V_{CC} = 0V, V_O = -7V to 12V		-50	50	µA	1, 2, 3
I_{OZ}	High Impedance State Output Current	V_O = -7V to 12V		-50	50	µA	1, 2, 3
I_{IH}	Logical 1 Input Current	V_I = 2.4V			20	µA	1, 2, 3
I_{IL}	Logical 0 Input Current	V_I = 0.4V		-50		µA	1, 2, 3
I_{CC}	Supply Current	Outputs Enabled			50	mA	1, 2, 3
I_{CCX}	Supply Current	Outputs Disabled			30	mA	1, 2, 3
I_{OS1}	Short Circuit Output Current	V_O = -7V	(*Note 4*)	-250		mA	1, 2, 3
I_{OS2}	Short Circuit Output Current	V_O = 0V	(*Note 4*)	-150		mA	1, 2, 3
I_{OS3}	Short Circuit Output Current	V_O = V_{CC}	(*Note 4*)		150	mA	1, 2, 3
I_{OS4}	Short Circuit Output Current	V_O = 12V	(*Note 4*)		250	mA	1, 2, 3
t_{PLH}	Propagation Delay Lo to Hi level	R_L = 27Ω, C_L = 15pF *Figure 4*			25	ns	10, 11
					16	ns	9
t_{PHL}	Propagation Delay Hi to Low Level	R_L = 27Ω, C_L = 15pF *Figure 4*			25	ns	10, 11
					16	ns	9
SKEW	Output to Output Delay Time	R_L = 60Ω			10	ns	10, 11
					4	ns	9
t_{LZ}	Output Disable Time From Low Level	R_L = 110Ω, C_L = 50pF *Figure 6*			40	ns	10, 11
					25	ns	9

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{HZ}	Output Disable Time From High Level	R_L = 110Ω, C_L = 50pF *Figure 5*			80	ns	10, 11
					30	ns	9
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, C_L = 50pF *Figure 6*			100	ns	10, 11
					40	ns	9
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, C_L = 50pF *Figure 4*			40	ns	10, 11
					32	ns	9
t_{DD}	Differential Output Delay Time	R_L = 60Ω, C_L = 15pF *Figure 3*			30	ns	10, 11
					22	ns	9
t_{TD}	Differential Output Transition Time	R_L = 60Ω, C_L = 15pF *Figure 3*			40	ns	10, 11
					22	ns	9

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Above T_A = 25°C, derate “E” package 13.3, “J” package 12.5, “W” package 7.1 mW/°C

Note 3: −55°C limit exceeds EIA standard RS−485 specification

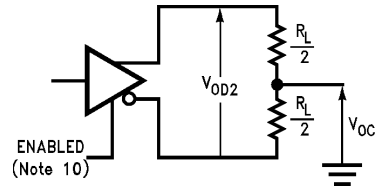
Note 4: 0.2µF cap is connected between the output and Gnd to reduce oscillation.

Note 5: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 6: $\Delta|V_{OD}|$ is the change in magnitude of V_{OD}, that occurs when the input is changed between high and low levels.

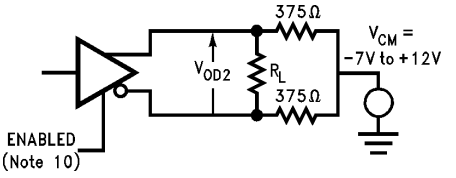
Note 7: $\Delta|V_{OC}|$ is the change in magnitude of the V_{OC} that occurs when the input is changed between high and low levels.

Parameter Measurement Information



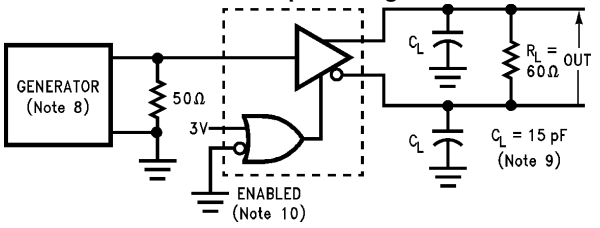
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FIGURE 1. Differential and Common Mode Output Voltage

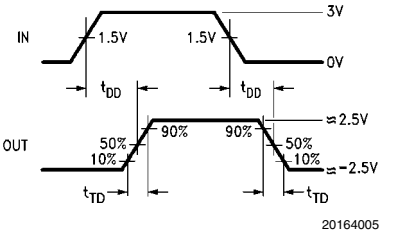


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FIGURE 2. Differential Output Voltage with Varying Common Mode Voltage

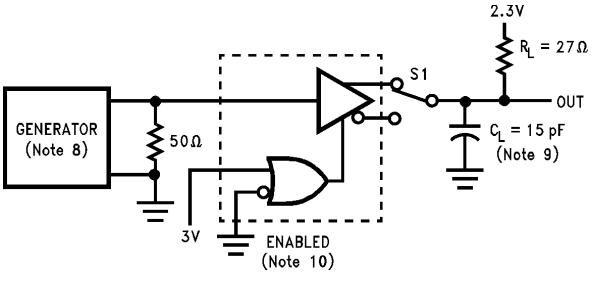


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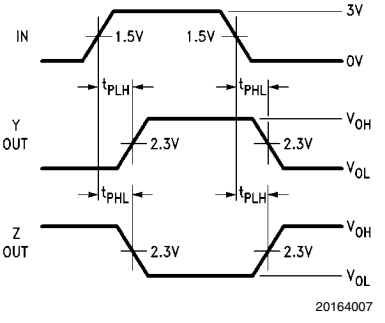


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FIGURE 3. Differential Output Delay and Transition Times

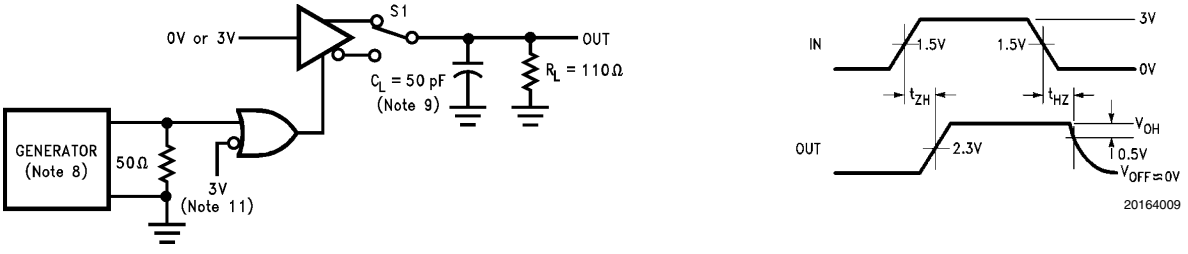


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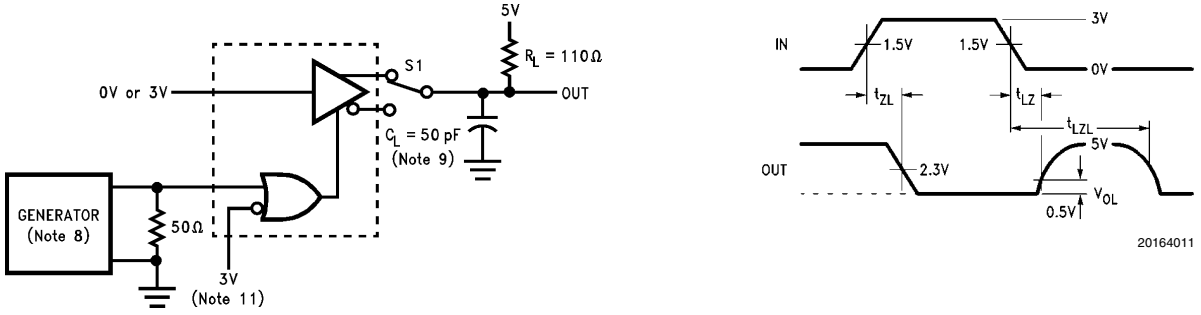
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FIGURE 4. Propagation Delay Times



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FIGURE 5. t_{ZH} and t_{HZ}



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FIGURE 6. t_{ZL}, t_{LZ}, t_{LZL}

Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns, Z_O = 50Ω.

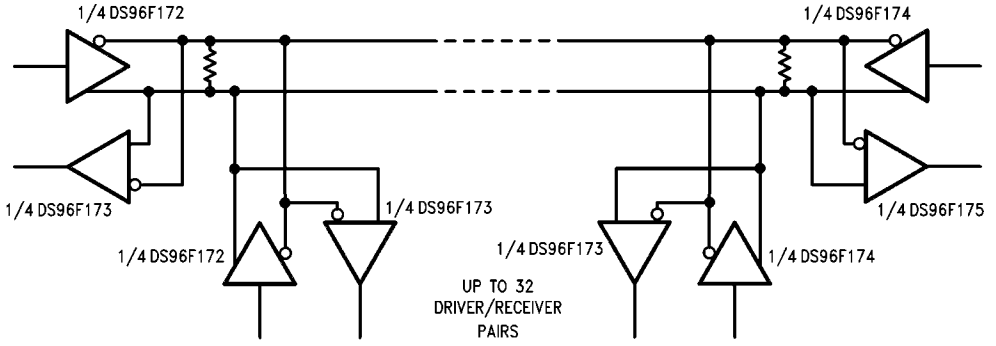
Note 9: C_L includes probe and jig capacitance.

Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Note 11: To test the active low Enable $\overline{E}$ of DS96F172 ground $\overline{E}$ and apply an inverted waveform to $\overline{E}$. DS96F174 has active high Enable only.

Note 12: For more information see Application Bulletin, Contact Product Marketing.

Typical Application



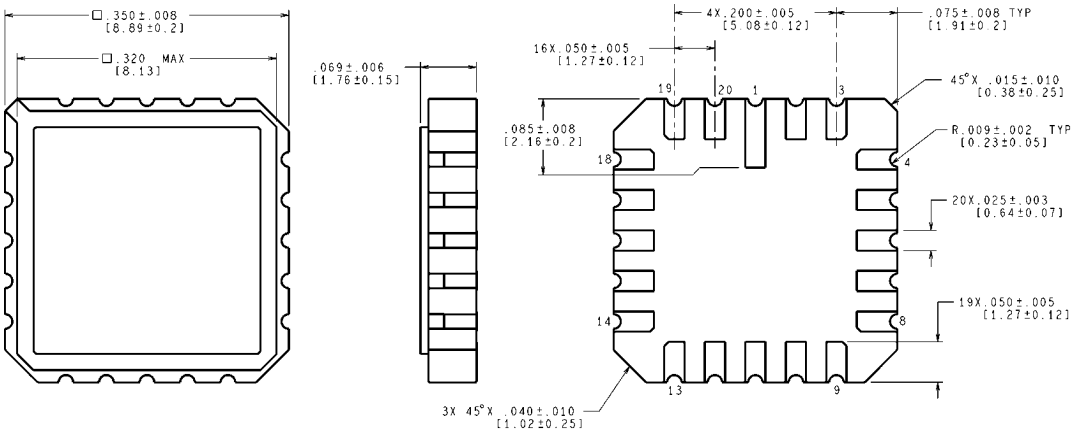
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The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

Revision History

Released	Revision	Section	Changes
8–Apr-11	A	New Release, Corporate format	2 MDS data sheets converted into one Corp. data sheet format. MNDS96F172M-X Rev 1A0 & MNDS96F174M-X Rev 1B0 will be archived.

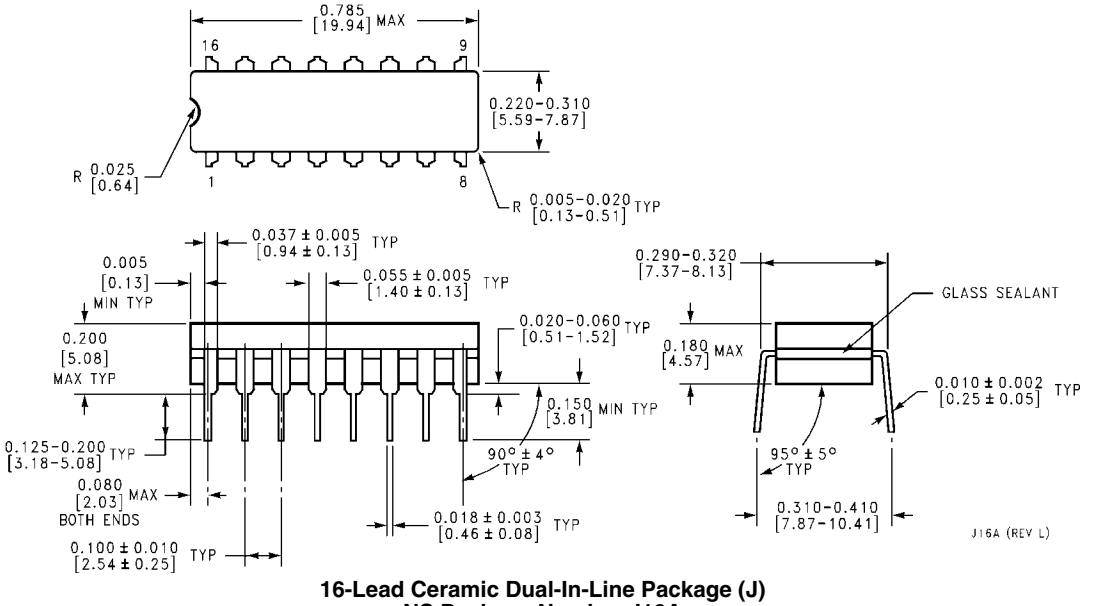
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

20-Lead Ceramic Leadless Chip Carrier (E)
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A

Notes

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