ACT2113

Rev 3, 23-May-12

18V/3A Step-Down DC/DC Converter

FEATURES

- 3A Output Current
- Wide 4.5V to 18V Operating Input Range
- Synchronous Buck Topology
- Integrated 85mΩ Power MOSFET Switches
- Output Adjustable from 0.923V to 12V
- Up to 95% Efficiency
- Stable with Low ESR Ceramic Output Capacitors
- Internal Soft Start
- 3mA Low Standby Input Current
- High Light Load Efficiency
- Cycle-by-Cycle Over Current Limit
- Input Under Voltage Lockout
- Hiccup Protection at Short Circuit and Over Current
- Frequency Fold Back Protection
- Low Power Dissipation at Over Current and Short Circuit

GENERAL DESCRIPTION

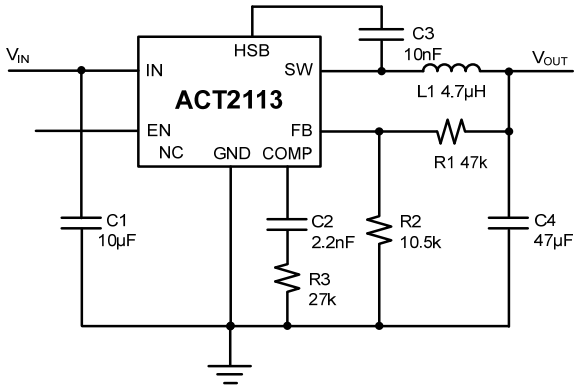
ACT2113 is a monolithic synchronous buck regulator. The device integrates two 85mΩ MOSFETs, and provides 3A of continuous load current over a wide input voltage of 4.5V to 18V. Current mode control provides fast transient response and cycle-by-cycle current limit. Hiccup at short circuit reduces IC temperatures.

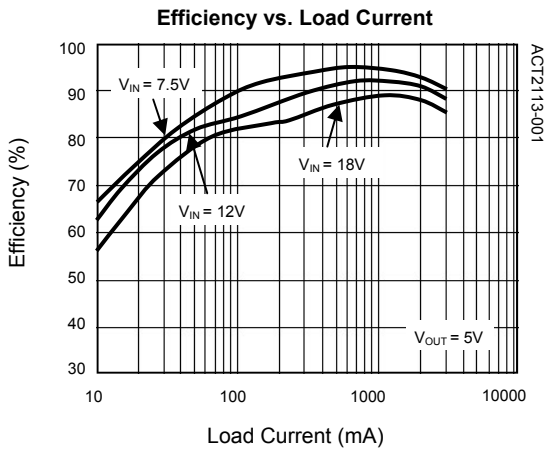
An internal soft-start prevents inrush current at turn-on, and in shutdown mode the supply current drops to 10μA. Pulse-skipping mode at light load reduces standby power down to 3mA.

This device, available in an 8-pin SOP-8EP package, provides a very compact solution with minimal external components.

APPLICATIONS

- LCD-TV
- Set-top Box
- Distributed Power Systems
- Networking Systems



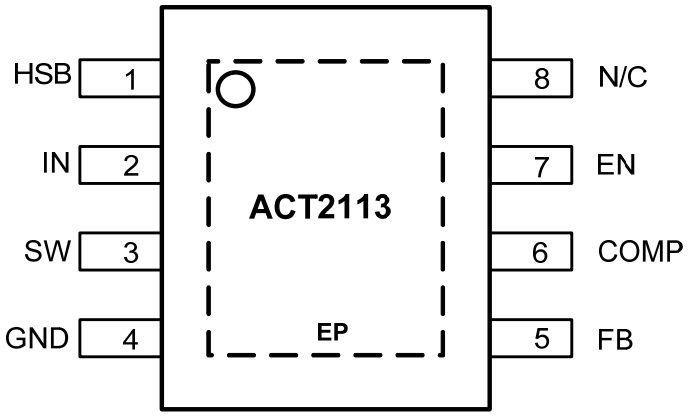


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ORDERING INFORMATION

PART NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT2113YH-T	-40°C to 85°C	SOP-8EP	8	TAPE & REEL

PIN CONFIGURATION



SOP-8EP

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	HSB	High-Side Bias Input. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 10nF or greater capacitor between HSB and SW pins.
2	IN	Input Supply. Bypass this pin to GND with a low ESR capacitor. Drive IN with a 4.5V to 18V power source. See *Input Capacitor* in the *Application Information* section.
3	SW	Switch Output. Connect this pin to the switching end of the external inductor. Note that a capacitor is required from SW to HSB to power the high-side switch.
4	GND	Ground.
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.923V. See *Setting the Output Voltage*.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. See *Compensation Components.*
7	EN	Enable Input. When higher than 2.5V, this pin turns the IC on. When lower than 2.3V, this pin turns IC off. When left unconnected, EN is pulled up to logic HIGH with a 2μA pull-up current. EN is a digital input that turns the regulator on or off.
8	N/C	Not connected.

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ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to + 20	V
SW to GND	-1 to VIN + 1	V
HSB to GND	V_{SW} - 0.3 to V_{SW} + 6	V
FB, EN, COMP to GND	-0.3 to + 6	V
Continuous SW Current	Internally limited	A
Junction to Ambient Thermal Resistance	46	˚C/W
Maximum Power Dissipation	0.76	W
Operating Junction Temperature	-40 to 150	˚C
Storage Junction	-55 to 150	˚C
Lead Temperature (Soldering 10 sec.)	300	˚C

①: Do not exceed these limits to prevent damage to the device. Exposure to Absolute Maximum Rating conditions for long periods may affect device reliability.

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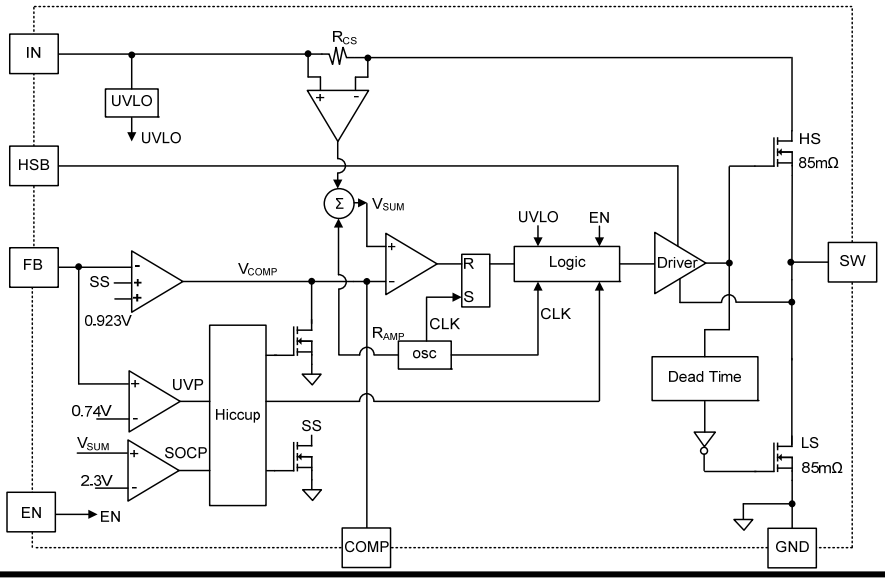
ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Shutdown Supply Current		V_{EN} = 0V		10	20	μA
Supply Current		V_{EN} = 3V, V_{FB} = 1.2V		0.75	1.1	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 18V	0.909	0.923	0.937	V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10μA		800		μA/V
High-Side Switch On Resistance	$R_{DS(ON)1}$			85		mΩ
Low-Side Switch On Resistance	$R_{DS(ON)2}$			85		mΩ
Upper Switch Current Limit		50% Duty Cycle		4.5		A
COMP to Current Sense Transconductance	G_{CS}			4.5		A/V
Oscillation Frequency	F_{sw}		460	510	570	kHz
Short Circuit Oscillation Frequency				160		kHz
Maximum Duty Cycle	D_{MAX}			88		%
EN Lockout Threshold Voltage			2.4	2.6	2.8	V
EN Lockout Hysteresis				75		mV
Input Under Voltage Lockout Threshold		Input Voltage Rising	4	4.2	4.4	V
Internal Soft Startup Time				2		ms
Hiccup Frequency at short circuit				26		Hz
Under Voltage Threshold				0.74		V
Thermal Shutdown				160		°C
Thermal Shutdown Hysteresis Window				30		°C

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FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As seen in Function Block Diagram, the ACT2113 is peak current mode controlled synchronous Buck converter. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off and the Low-Side Power Switch turns on. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to VSW + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.923V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output to keep the output voltage regulated. The Oscillator normally switches at 510kHz.

Pulse Skipping Mode

To decrease the power recycling at very light load, the low-side FET current is sensed to emulate a diode. When the low-side FET current decreases to zero, the FET is turned off to avoid negative inductor current. At no load and very light load, ACT2113 skips pulse automatically and thus achieve very high light load efficiency. With load increasing, ACT2113 goes into Discontinuous Current Mode (DCM) and then Continuous Current Mode (CCM).

Soft Startup

The ACT2113 builds in internal soft startup function. The internal FB reference voltage rises to steady state of 0.923V in 2ms to avoid inrush input current during startup.

Under Voltage Protection (UVP)

At output short circuit or over current, the FB voltage is usually pulled low. To protect the IC at over current and short circuit, the ACT2113 builds in Under Voltage Protection (UVP) function. When ACT2113 detects the FB voltage below 75% of the 0.923V reference, it pulls low COMP voltage and discharges internal soft-start capacitor and goes into hiccup mode. The IC restarts in 32ms after going into hiccup mode. If the short circuit or over current is clear, the IC restarts back to normal mode. The UVP is disabled for 6ms starting from startup. If the output is short at startup, the output voltage never rises to nominal voltage. During the 6ms period of time, the output current is limited by cycle-by-cycle current limit. With 32ms shutdown period, the average input and output current at short circuit is significantly reduced and the IC is more reliable.

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Secondary Over Current Protection (SOCP)

In normal operation, ACT2113 high-side FET current is protected by cycle-by-cycle current limit. In some fault conditions, the input current may run away. SOCP current limit is set 30% higher than cycle-by-cycle current limit, and once SOCP is triggered, ACT2113 goes into hiccup mode and reduce the power dissipation significantly.

Enable Pin

The ACT2113 has an enable input EN for turning the IC on or off. The EN pin contains a precision 2.5V comparator with 75mV hysteresis and a 1.3μA pull-up current source. The comparator can be used with a resistor divider from V_{IN} to program a startup voltage higher than the normal UVLO value. If left floating, the EN pin will be pulled up to roughly 5V by the internal 1.3μA current source. It can be driven from standard logic signals greater than 2.5V, or driven with open-drain logic to provide digital on/off control.

Thermal Shutdown

The ACT2113 disables switching when its junction temperature exceeds 160°C and resumes when the temperature has dropped by 30°C.

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APPLICATIONS INFORMATION

Output Voltage Setting

Figure 1:

Output Voltage Setting

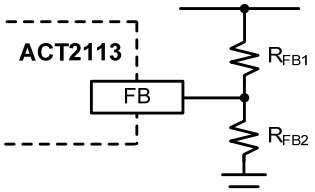


Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Typically, use $R_{FB2} \approx 10k\Omega$ and determine R_{FB1} from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.923\ V} - 1\right) \quad (1)$$

Table 1:

Recommended Resistance Values

V_{OUT}	R1	R2
5.0V	47kΩ	10.5kΩ
3.3V	27.4kΩ	10.5kΩ
2.5V	18kΩ	10.5kΩ
1.8V	10.2kΩ	10.5kΩ
1.2V	3.3kΩ	10.5kΩ
1.0V	1kΩ	10.5kΩ

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOADMAX} K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 20~40% to correspond to the peak-to-peak inductor ripple current being 20~40% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (3)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad (4)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (5)$$

L_{LIM} is the internal current limit, which is typically 4.5A, as shown in Electrical Characteristics Table.

Table 2:

Inductor Values Range and Typical Compensation

V_{OUT}	V_{IN}	L	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2}
5.0V	8V ~ 18V	4.7μH ~ 10μH	330μF/10V	25kΩ	2.2nF	220PF
			22μF/ Ceramic × 2	10kΩ	2.2nF	220PF
3.3V	6V ~ 18V	3.3μH ~ 8.2μH	330μF/10V	21kΩ	2.2nF	220PF
			22μF/ Ceramic × 2	8.2kΩ	2.2nF	220PF
1.8V	4.5V ~ 8V	2.2μH ~ 6.8μH	470μF/10V	12kΩ	4.7nF	220PF
			22μF/ Ceramic × 2	8.2kΩ	4.7nF	N/A
1.2V	4.5V ~ 6V	2μH ~ 6μH	470μF/10V	12kΩ	10nF	220PF
			22μF/ Ceramic × 2	8.2kΩ	10nF	N/A
1.0V	4.5V ~ 5.2V	1.5μH ~ 4.7μH	470μF/10V	10kΩ	10nF	220PF
			22μF/ Ceramic × 2	8.2kΩ	10nF	N/A

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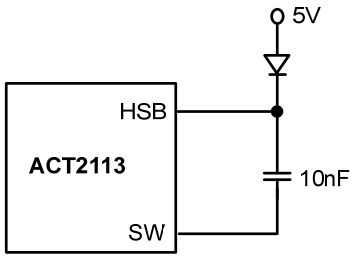
APPLICATIONS INFORMATION CONT'D

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54.

Figure 2:

External High Voltage Bias Diode



This diode is also recommended for high duty cycle operation and high output voltage applications.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1µF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{28 \times f_{SW}{}^2 L C_{OUT}} \quad (6)$$

where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about 22µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency.

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PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce both the AC loop and DC loop size. AC loop includes input cap, V_{IN} pin and V_{IN} ground pin, DC loop includes SW pin, inductor, output capacitor and ground pin.
2) Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND with vias or short and wide path.
3) Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity.
4) Use copper plane for power GND for best heat dissipation and noise immunity.
5) Place feedback resistor close to FB pin.
6) Use short trace connecting HSB-C_{HSB}-SW loop

Figure 3 shows an example of PCB layout.

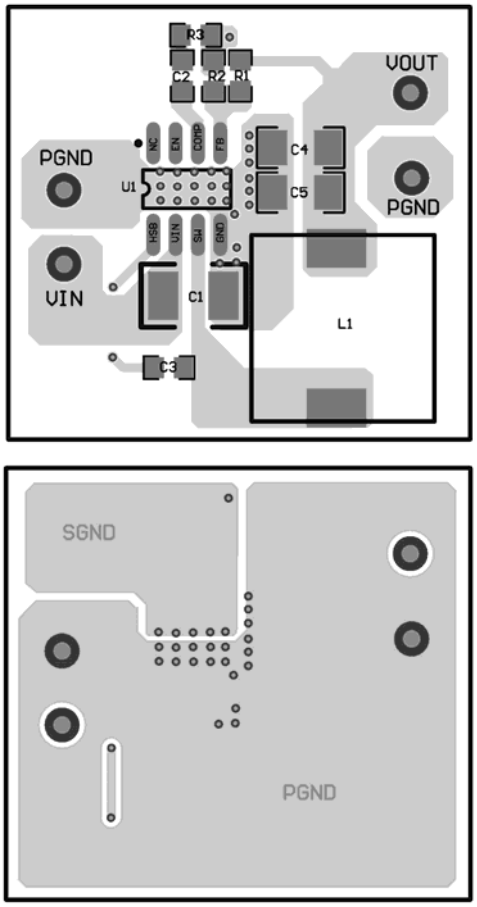


Figure 3: PCB Layout

Figure 4 and Figure 5 give two typical car charger application schematics and associated BOM list.

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Figure 4:
Typical Application Circuit for 1.8V/3A DC-DC Converter

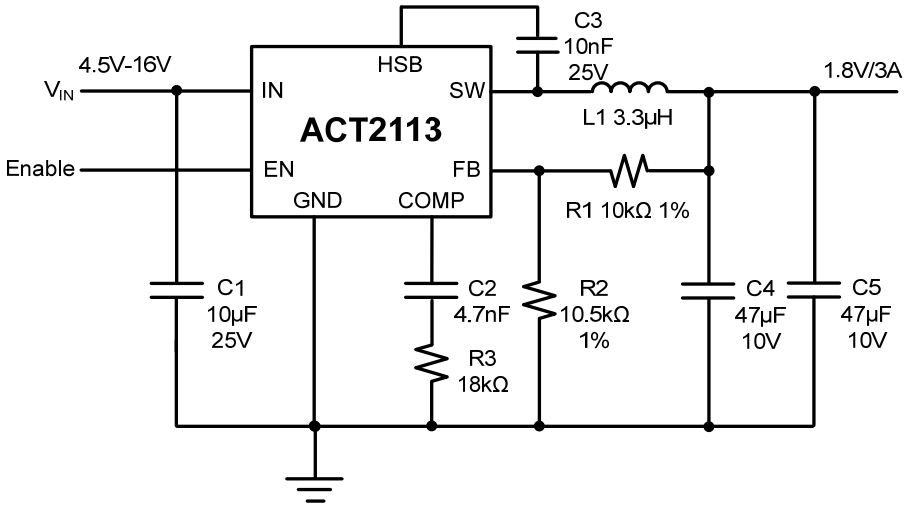


Table 3:
BOM List for 1.8V/3A DC-DC Converter

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT2113YH, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Ceramic, 10µF/25V, 1210, SMD	Murata, TDK	1
3	C2	Capacitor, Ceramic, 4.7nF/6.3V, 0603, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 10nF/25V, 0603, SMD	Murata, TDK	1
5	C4,C5	Capacitor, Ceramic, 47µF/10V, 1206, SMD	Murata, TDK	2
6	L1	Inductor, 3.3µH, 4A, 20%, SMD	Tyco Electronics	1
7	R1	Chip Resistor, 10kΩ, 0603, 1%	Murata, TDK	1
8	R2	Chip Resistor, 10.5kΩ, 0603, 1%	Murata, TDK	1
9	R3	Chip Resistor, 18kΩ, 0603, 5%	Murata, TDK	1

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Figure 5:
Typical Application Circuit for 5V/3A DC-DC Converter

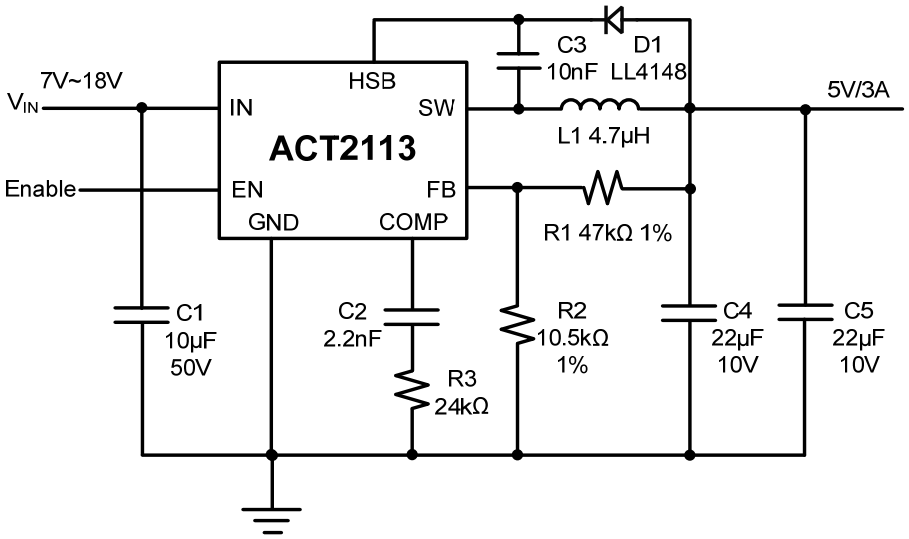


Table 4:
BOM List for 5V/3A DC-DC Converter

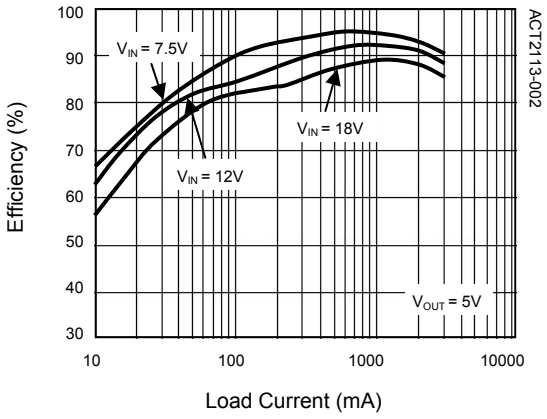
ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT2113YH, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Ceramic, 10μF/50V, 1210, SMD	Murata, TDK	1
3	C2	Capacitor, Ceramic, 2.2nF/6.3V, 0603, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 10nF/50V, 0603, SMD	Murata, TDK	1
5	C4,C5	Capacitor, Ceramic, 22μF/10V, 1206, SMD	Murata, TDK	2
6	L1	Inductor, 4.7μH, 4A, 20%	Sumida	1
7	D1	Diode, 75V/150mA, LL4148	Good-ARK	1
8	R1	Chip Resistor, 47kΩ, 0603, 1%	Murata, TDK	1
9	R2	Chip Resistor, 10.5kΩ, 0603, 1%	Murata, TDK	1
10	R3	Chip Resistor, 24kΩ, 0603, 5%	Murata, TDK	1

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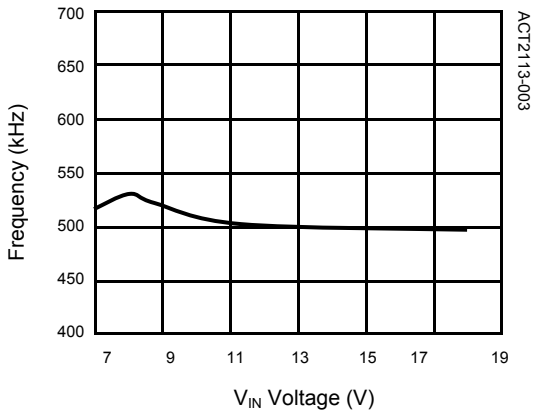
TYPICAL PERFORMANCE CHARACTERISTICS

($L = 4.7\mu H$, $C_{IN} = 100\mu F$, $C_{OUT} = 330\mu F$, $Ta = 25°C$, $R_{COMP} = 27k$, $C_{COMP1} = 2.2nF$, $C_{COMP2} = N/C$)

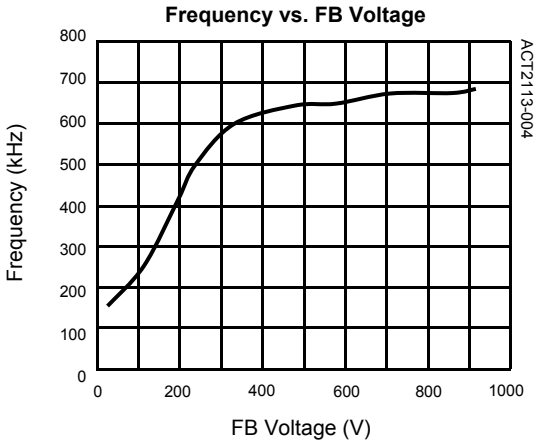
Efficiency vs. Load Current



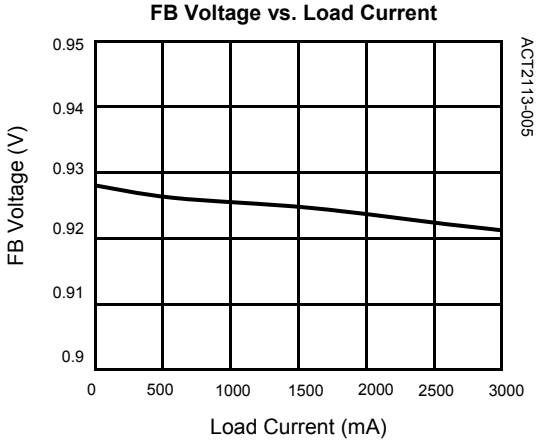
Frequency vs. V_{IN}



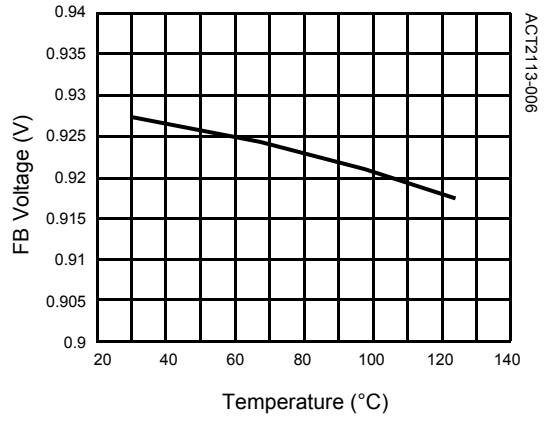
Frequency vs. FB Voltage



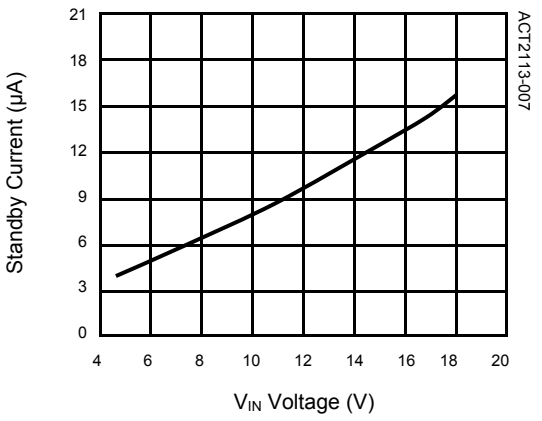
FB Voltage vs. Load Current



FB Voltage vs. IC Temperature



Shutdown Current vs. V_{IN}

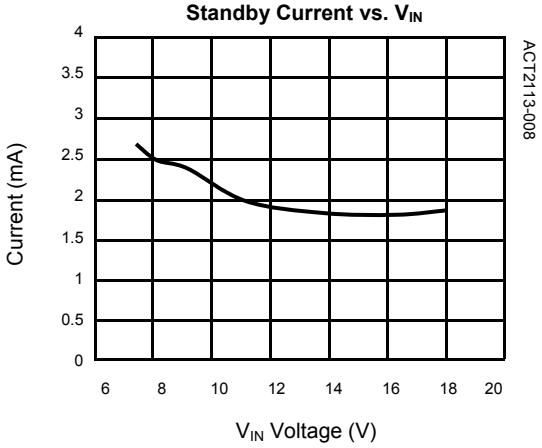


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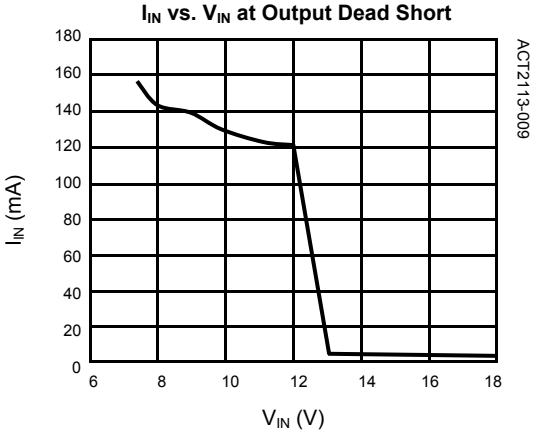
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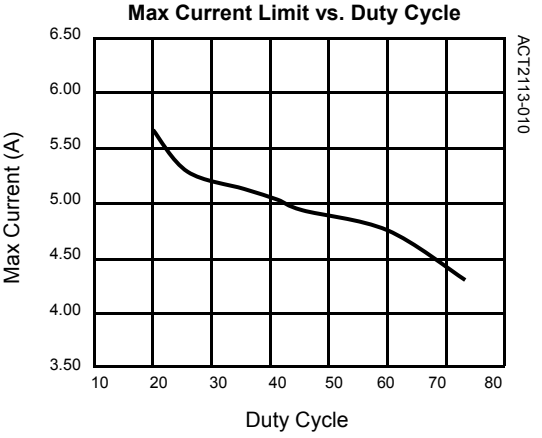
Standby Current vs. V_{IN}



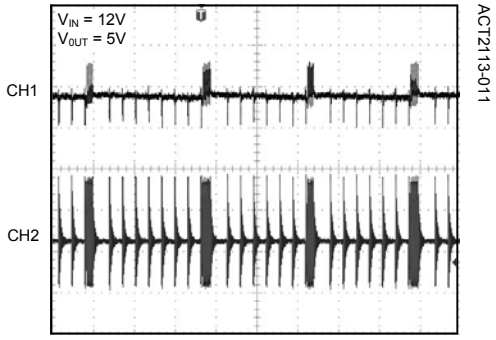
I_{IN} vs. V_{IN} at Output Dead Short



Max Current Limit vs. Duty Cycle

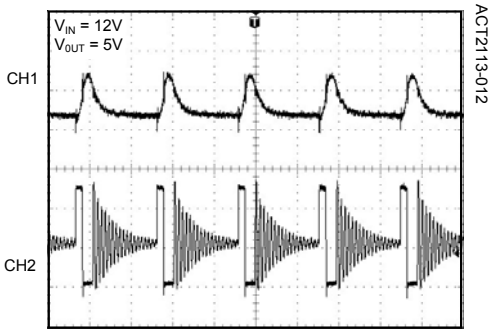


No Load Operation



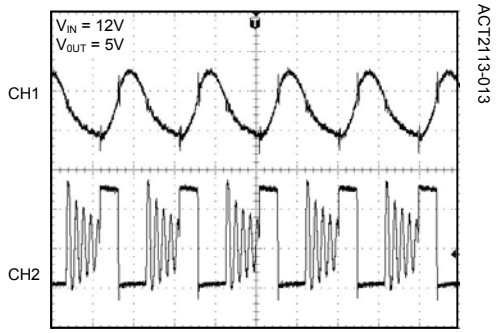
CH1: V_{RIPPLE}, 20mV/div
CH2: SW, 5V/div
TIME: 40μs/div

50mA Load Operation



CH1: V_{RIPPLE}, 20mV/div
CH2: SW, 5V/div
TIME: 2μs/div

200mA Load Operation



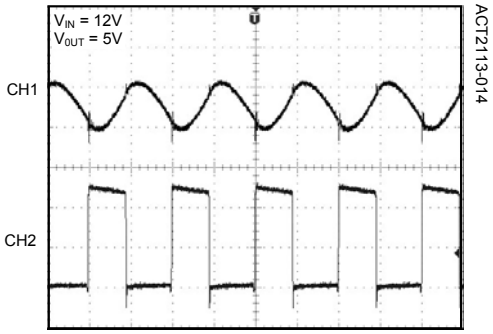
CH1: V_{RIPPLE}, 20mV/div
CH2: SW, 5V/div
TIME: 1μs/div

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TYPICAL PERFORMANCE CHARACTERISTICS

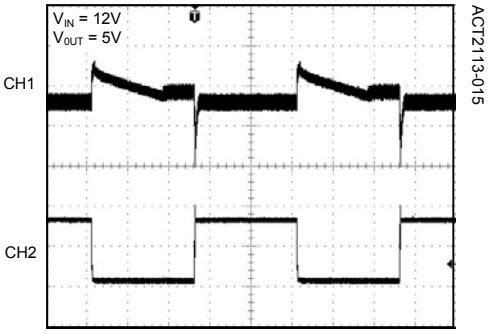
($L = 4.7\mu H$, $C_{IN} = 100\mu F$, $C_{OUT} = 330\mu F$, Ta = 25°C, $R_{COMP} = 27k$, $C_{COMP1} = 2.2nF$, $C_{COMP2} = N/C$)

3A Load Operation



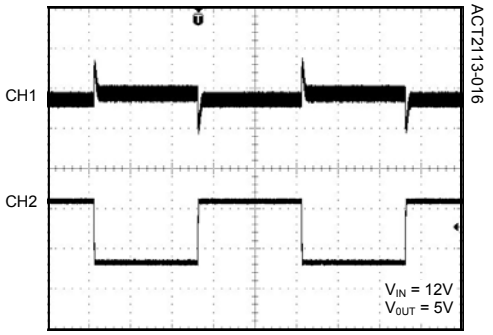
CH1: V_{RIPPLE}, 50mV/div
CH2: SW, 5V/div
TIME: 1μs/div

Load Transient (0A~1.5A)



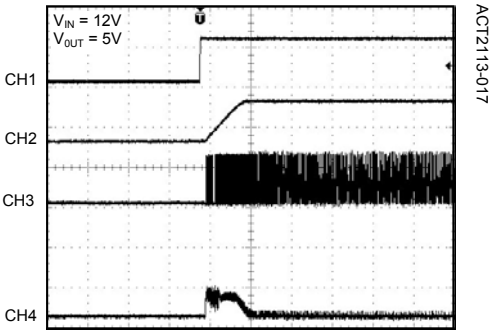
CH1: V_{OUT}, 100mV/div
CH2: I_{LOAD}, 1A/div
TIME: 2ms//div

Load Transient (1.5A~3A)



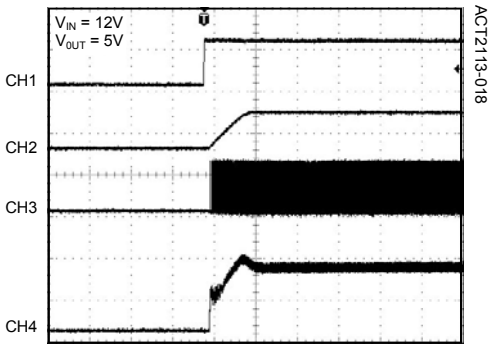
CH1: V_{OUT}, 100mV/div
CH2: I_{LOAD}, 1A/div
TIME: 2ms//div

Start Up with V_{IN} (Load 0A)



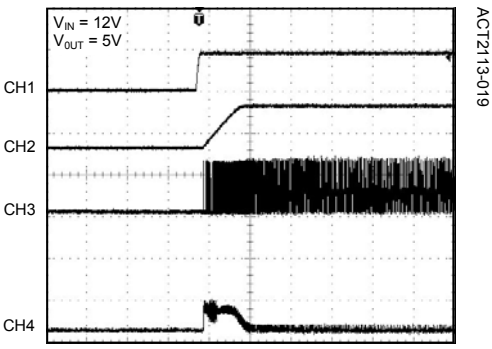
CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 5V/div
CH3: SW, 10V/div
CH4: I_L, 2A/div
TIME: 2ms/div

Start Up with V_{IN} (Load 3A)



CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 5V/div
CH3: SW, 10V/div
CH4: I_L, 2A/div
TIME: 2ms/div

Start Up with EN (Load 0A)



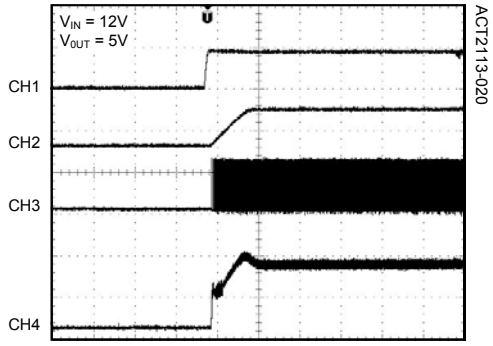
CH1: EN, 5V/div
CH2: V_{OUT}, 5V/div
CH3: SW, 10V/div
CH4: I_L, 2A/div
TIME: 2ms/div

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TYPICAL PERFORMANCE CHARACTERISTICS

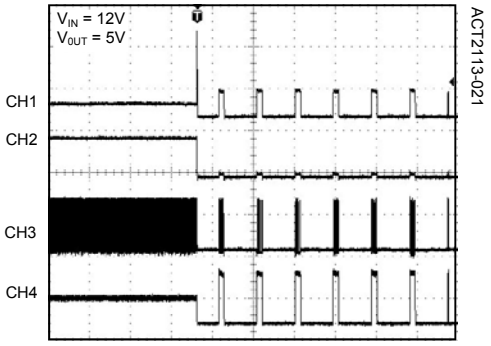
($L = 4.7\mu H$, $C_{IN} = 100\mu F$, $C_{OUT} = 330\mu F$, $Ta = 25°C$, $R_{COMP} = 27k$, $C_{COMP1} = 2.2nF$, $C_{COMP2} = N/C$)

Start Up with EN (Load 3A)



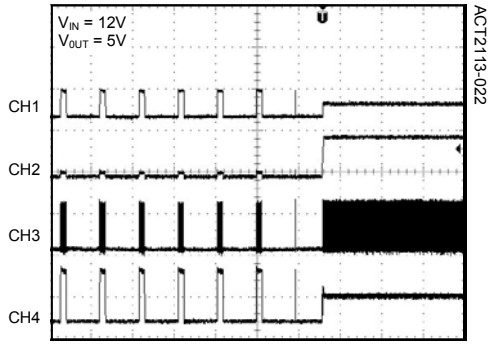
CH1: EN, 5V/div
CH2: V_{OUT}, 5V/div
CH3: SW, 10V/div
CH4: I_L, 2A/div
TIME: 2ms/div

Short Circuit



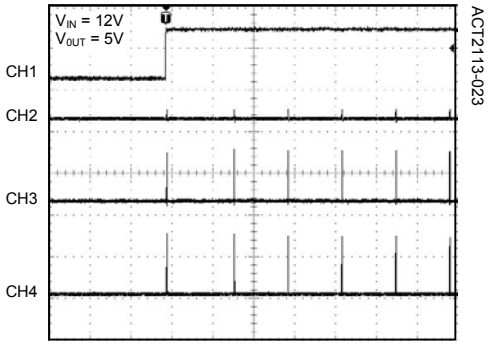
CH1: I_{OUT}, 10A/div
CH2: V_{OUT}, 5V/div
CH3: SW, 10V/div
CH4: I_L, 5A/div
TIME: 40ms/div

Short Circuit Recovery



CH1: I_{OUT}, 5A/div
CH2: V_{OUT}, 5V/div
CH3: SW, 10V/div
CH4: I_L, 5A/div
TIME: 40ms/div

Start Up with Output Dead Short

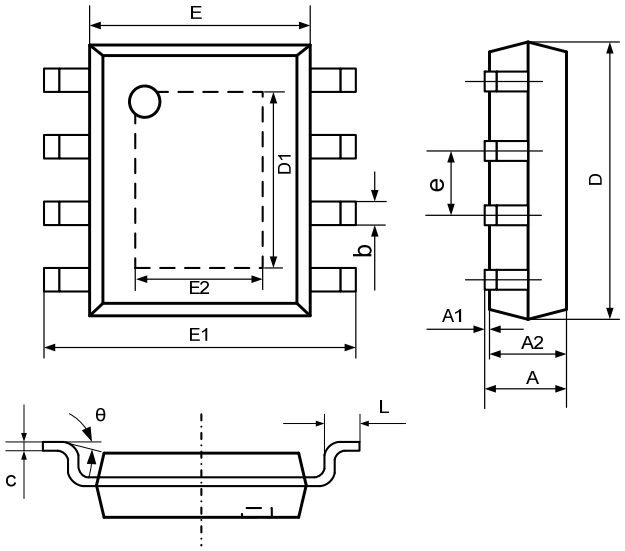


CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 5V/div
CH3: SW, 10V/div
CH4: I_L, 5A/div
TIME: 20ms/div

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PACKAGE OUTLINE

SOP-8EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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