USB CHARGER OVP SWITCH WITH ESD FOR V_{BUS_CON} PIN

Check for Samples: TPD1S414

FEATURES

- **Input DC Voltage Protection at V_{BUS_CON} up to 30 V**
- **Low R_{ON} nFET Switch Supports Host and Charging Mode**
- **Withstands up to 100V Open Circuit Surge Voltage (per IEC61000-4-5)**
- **Internal 15 ms Startup Delay**
- **Internal 30 ms Soft-start Delay to Minimize the USB Inrush Current**
- **ESD Performance V_{BUS_CON}**
  - **±15 kV Contact Discharge (IEC 61000-4-2)**
  - **±15 kV Air Gap Discharge (IEC 61000-4-2)**
- **Integrated Input Enable and Status Output Signal**
- **Thermal Shutdown Feature**
- **Space Saving WCSP Package (1.4 mm x 1.89 mm)**

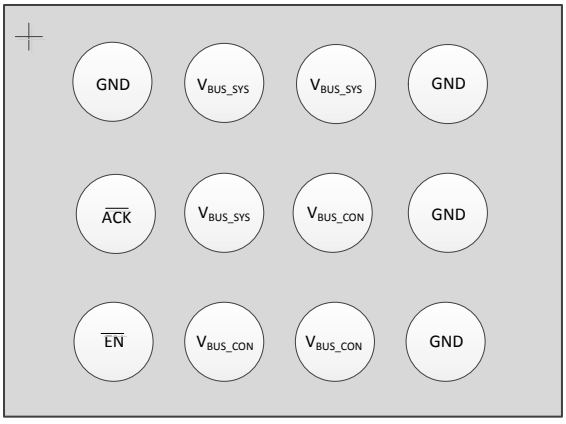
APPLICATIONS

- **Cell Phones**
- **eBook**
- **Portable Media Players**

DESCRIPTION

The TPD1S414 is a single-chip solution for USB connector's V_{BUS} line protection. The bi-directional nFET switch ensures safe current flow in both charging and host mode while protecting the internal system circuits from any over-voltage conditions at the V_{BUS_CON} pin. On the V_{BUS_CON} pin, this device can handle overvoltage protection up to 30 V. After the $\overline{EN}$ pin toggles low, the TPD1S414 waits 20 ms before turning ON the nFET through a soft start delay. $\overline{ACK}$ pin indicates the FET is completely turned ON.

YZ PACKAGE
(TOP VIEW - SEE THROUGH)



12-YZ Pin Mapping

	1	2	3	4
A	GND	V_{BUS_SYS}	V_{BUS_SYS}	GND
B	$\overline{ACK}$	V_{BUS_SYS}	V_{BUS_CON}	GND
C	$\overline{EN}$	V_{BUS_CON}	V_{BUS_CON}	GND

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM

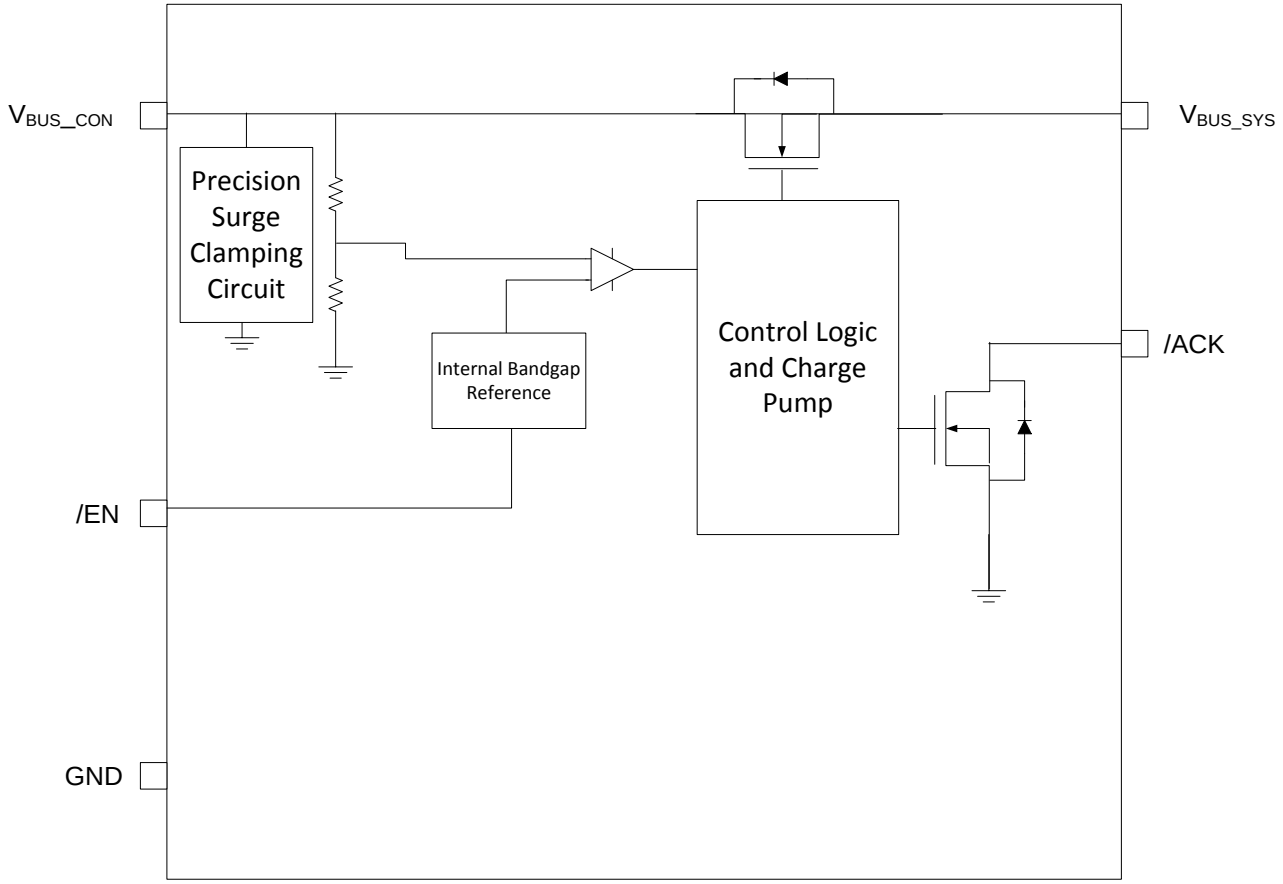


Table 1. DEVICE OPERATION

Voltage Condition			Current Condition		
V_{BUS_CON}	V_{BUS_SYS}	$\overline{EN}$	Current Flow	Comment	$\overline{ACK}$ Pin
X	$<V_{BUS_CON}$	High	No Flow	Switch off	High-Z
X	$>V_{BUS_CON}$	High	V_{BUS_SYS} to V_{BUS_CON}	Switch off, current flows through the body diode	High-Z
<OVP	$<V_{BUS_CON}$	Low	V_{BUS_CON} to V_{BUS_SYS}	Current flows through the switch, normal device charging mode	Low
<OVP	$>V_{BUS_CON}$	Low	V_{BUS_SYS} to V_{BUS_CON}	Current flows through the switch, normal host mode	Low
>OVP	$<V_{BUS_CON}$	Low	No Flow	Switch off due to OVP	High-Z
>OVP	$>V_{BUS_CON}$	Low	V_{BUS_SYS} to V_{BUS_CON}	Switch off, current flows through the body diode	High-Z
X	X	X	No Flow/ Current thru Body Diode	THERMAL SHUTDOWN CONDITION	High-Z
$<V_{UVLO}$	$<V_{BUS_CON}$	Low	No Flow	Low Voltage is cut-off from the system	High-Z

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PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
$\overline{ACK}$	B1	O	Open-Drain Acknowledge pin. See the Device Operation section.
$\overline{EN}$	C1	I	Enable Active-Low Input. Drive $\overline{EN}$ low to enable the switch. Drive $\overline{EN}$ high to disable the switch.
V_{BUS_CON}	C3, C2, B3	I/O	Connect to USB connector V_{BUS_CON}; IEC61000-4-2 ESD protection IEC61000-4-5 Surge protection
V_{BUS_SYS}	A3, A2, B2	I/O	Connect to internal V_{BUS} plane
GND	A1, A4, B4, C4	Ground	Connect to PCB ground plane

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage from USB connector, V_{BUS_CON}		–0.3	30	V
Internal Supply DC voltage Rail on the PCB, V_{BUS_SYS}		–0.5	7	V
Voltage on Input pin ($\overline{EN}$). V_{EN}		–0.5	7	V
Voltage on $\overline{ACK}$ pin		–0.5	7	V
Storage temperature range, T_{STG}		–40	150	°C
Operating Free Air Temperature, T_A		–40	85	°C
IEC 61000-4-2 Contact Discharge	V_{BUS_CON} pin		±15	kV
IEC 61000-4-2 Air-gap Discharge	V_{BUS_CON} pin		±15	kV
Human-Body Model	ALL Pins		±2	kV
IEC 61000-4-5 Peak Pulse Current (t_p = 8/20 µs)	V_{BUS_CON} pin		21	A
IEC 61000-4-5 Peak Pulse Power (t_p = 8/20 µs)	V_{BUS_CON} pin		700	W
IEC 61000-4-5 Open circuit voltage (t_p = 1.2/50 µs)	V_{BUS_CON} pin		100	V
Output load capacitance, C_{LOAD}	V_{BUS_SYS} pin	0.1	50	µF
Input capacitance, C_{ON}	V_{BUS_CON} pin	0.1	50	µF

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL INFORMATION

THERMAL METRIC (1)		YZ 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	89	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	0.6	
θ_{JB}	Junction-to-board thermal resistance	16.3	
ψ_{JT}	Junction-to-top characterization parameter	2.7	
ψ_{JB}	Junction-to-board characterization parameter	16.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector				5.9	V
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB				5.9	V
C_{LOAD}	Output load capacitance	V_{BUS_SYS} pin		2.2		µF
C_{IN}	Input capacitance	V_{BUS_CON} pin		1		µF
R_{PULLUP}	Pull up resistor	$\overline{ACK}$ pin		4.3	100	kΩ
I_{VBUS}	Continuous current on V_{BUS_CON} and V_{BUS_SYS} pins	V_{BUS_CON} V_{BUS_SYS}			3.5	A
I_{DIODE}	Continuous current through the FET body diode				1	A

SUPPLY CURRENT CONSUMPTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS_SLEEP}	V_{BUS_CON} Operating Current Consumption	Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5 V, $\overline{EN}$ =5V		30	70	µA
I_{VBUS}		Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5 V, $\overline{EN}$ 0 V and no load		175	373	µA
I_{VBUS_SYS}	V_{BUS_CON} Operating Current Consumption	Measured at V_{BUS_SYS} pin, V_{BUS_SYS} = 5 V, $\overline{EN}$ = 0 V and V_{BUS_CON} = Hi Z		175	373	µA
I_{HOST_LEAK}	Host Mode Leakage current	Measured at V_{BUS_SYS}. V_{BUS_CON} = Hi Z, $\overline{EN}$ = 5 V, V_{BUS_SYS} = 5V	90		200	µA

ELECTRICAL CHARACTERISTICS ($\overline{EN}$, $\overline{ACK}$ PINS)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage, $\overline{EN}$		1.2		6	V
V_{IL}	Low-level input voltage, $\overline{EN}$				0.8	V
I_{IL}	Input Leakage Current $\overline{EN}$	V_I = 3.3 V			1	µA
V_{OL}	Low-level output voltage, $\overline{ACK}$	I_{OL} = 3 mA			0.4	V

ELECTRICAL CHARACTERISTICS (OVP CIRCUIT)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP_RISING}	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} increasing from 5 V	6	6.2	6.4	V
V_{HYS_OVP}	Hysteresis on OVP, V_{BUS_CON}	V_{BUS_CON} decreasing from 7 V to 5 V		50		mV
$V_{OVP_FALLING}$	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} decreasing from 7 V to 5 V	5.93		6.37	V
V_{UVLO}	Input under voltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 0 V to 5 V	3.1	3.3	3.5	V
V_{HYS_UVLO}	Hysteresis on UVLO, V_{BUS_CON}	Difference between rising and falling UVLO thresholds		100		mV
$V_{UVLO_FALLING}$	Input under voltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 5 V to 0 V	3	3.2	3.4	V
V_{UVLO_SYS}	V_{BUS_SYS} under voltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0 V to 5 V	3.1	3.6	4.3	V

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ELECTRICAL CHARACTERISTICS (OVP CIRCUIT) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS_UVLO_SYS}$	V_{BUS_SYS} UVLO Hysteresis, V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}		480		mV
$V_{UVLO_SYS_FALL}$	V_{BUS_SYS} undervoltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 7 V to 5 V	3	3.2	3.4	V

THERMAL SHUTDOWN FEATURE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHDN}	Thermal Shutdown	Junction temperature		145		°C
	Thermal-Shutdown Hysteresis	Junction temperature		35		°C

SWITCHING CHARACTERISTICS (nFET)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Switch ON Resistance	V_{BUS_CON} = 5 V, I_{OUT} = 1 A, T_A = 25°C		39	50	mΩ

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DELAY}	USB Charging Turn-ON Delay	Measured from $\overline{EN}$ asserted LOW to nFET beginning to Turn ON(1) excluding soft-start time		20		ms
t_{SS}	USB Charging rise time (Soft Start Delay)	Measure from V_{BUS_SYS} rises above 25% (with 1 MΩ load/ NO C_{LOAD}) until $\overline{ACK}$ goes Low (10%)		25		ms
t_{OFF_DELAY}	USB Charging Turn-OFF time	Measured from $\overline{EN}$ asserted High to V_{BUS_SYS} falling to 10% with R_{LOAD} = 10 Ω and No C_{LOAD} on V_{BUS_SYS}		4		µs
Over Voltage Protection						
$t_{OVP_response}$	OVP Response time	Measured from OVP Condition to FET Turn OFF(1)(2). V_{BUS_CON} rises at 1V / 100ns			100	ns
t_{OVP_Recov}	Recovery Time	Measured from OVP Clear to FET Turn ON(1)(3)		20		ms

(1) Shown in TIMING DIAGRAM Plots
(2) Parameters provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) Excludes soft start time

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TYPICAL CHARACTERISTICS

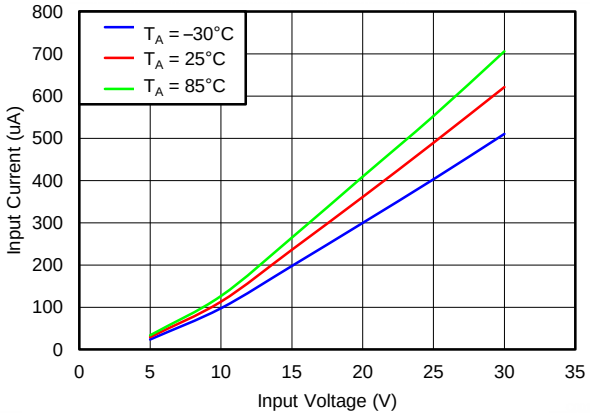


Figure 1. Input Supply Current vs. Supply Voltage

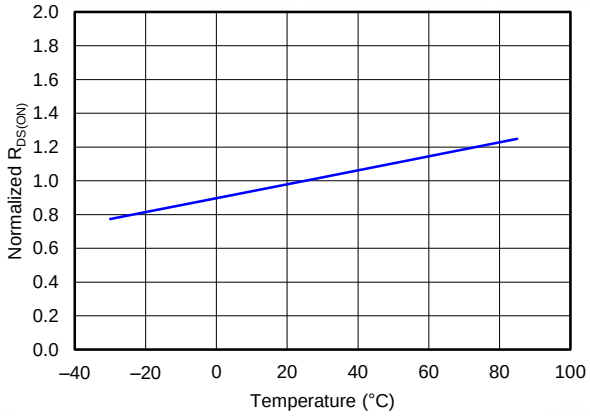


Figure 2. Normalized $R_{DS(ON)}$ vs. Temperature

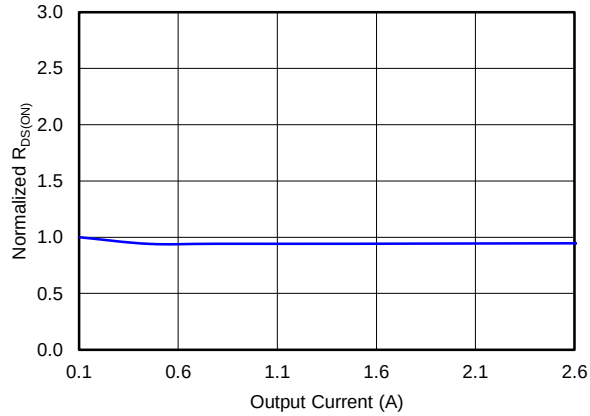


Figure 3. Normalized $R_{DS(ON)}$ vs. Output Current

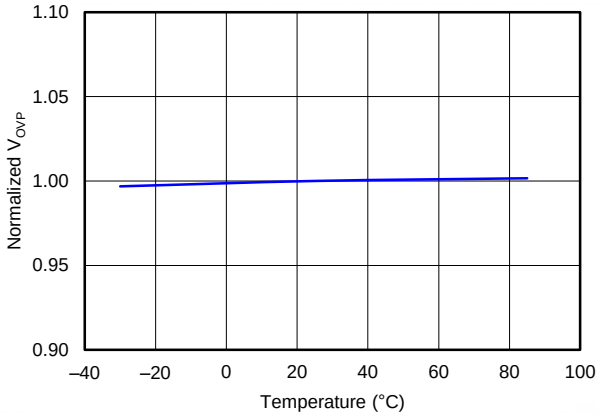


Figure 4. Normalized V_{OVP}

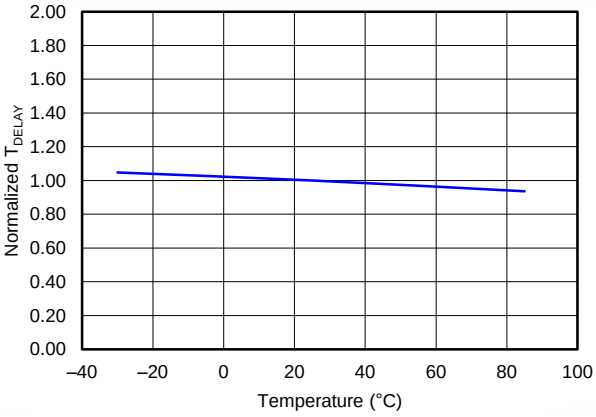


Figure 5. Normalized T_{DELAY}

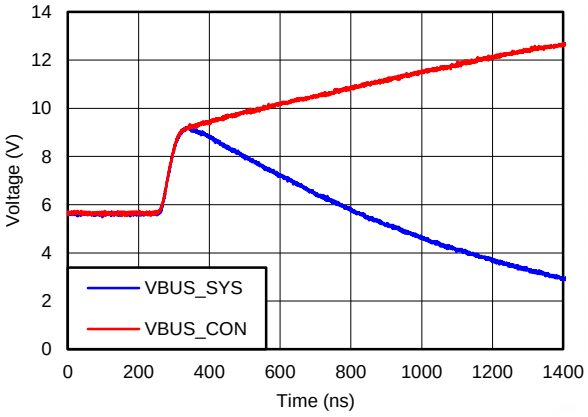


Figure 6. V_{OVP} Response Time

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TYPICAL CHARACTERISTICS (continued)

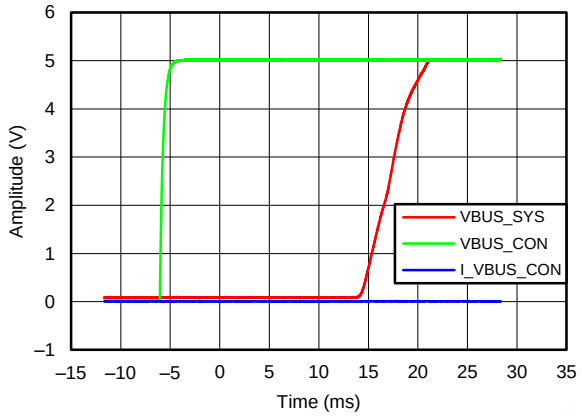


Figure 7. Power Up With 2.2 µF on V_{BUS_SYS}

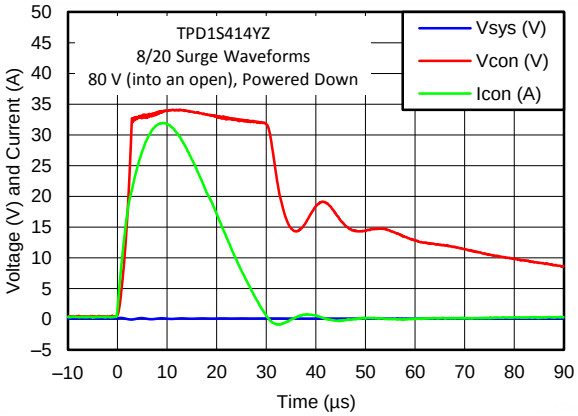


Figure 8. Response to a 100-V Surge

DEVICE INFORMATION

DEVICE OPERATION

The TPD1S414 provides a single-chip ESD protection, surge protection and over voltage protection solution for portable USB charging and Host interfaces. It offers over voltage protection at the V_{BUS_CON} pin up to 30 V. The TPD1S414 also provides a $\overline{ACK}$ pin that indicates to the system if a fault condition has occurred. The TPD1S414 offers an ESD clamp and a Surge Clamp for V_{BUS_CON} pin, thus eliminating the need for external TVS clamp circuits in the application.

The TPD1S414 has an internal oscillator and charge pump that controls the turn-on of the internal nFET switch. The internal oscillator controls the timers that enable the charge pump and resets the open-drain $\overline{ACK}$ output. If V_{BUS_CON} is less than V_{OVP}, the internal charge pump is enabled. After a 15 ms internal delay, the charge-pump starts-up, turns on the internal nFET switch through a soft start. Once the nFET is completely turned ON, TPD1S414 asserts $\overline{ACK}$ pin LOW. At any time, if V_{BUS_CON} rises above V_{OVP}, the $\overline{ACK}$ pin is in High-Z and is pulled HIGH through external resistors. The nFET switch is turned OFF.

OVP OPERATION

When the V_{BUS_CON} voltage rises above V_{OVP}, the internal nFET switch is turned OFF, removing power from the system. The response is rapid, with the FET switch turning off in less than 100 ns. The $\overline{ACK}$ pin is set to High-Z when an overvoltage condition is detected and the nFET is turned OFF. This pin can be pulled up through external resistors to indicate a OVP condition. When the V_{BUS_CON} voltage returns below $V_{OVP} – V_{HYS-OVP}$, the nFET switch is turned on again after the internal delay of tO_{VP_Recov}. This delay time ensures that the V_{BUS_CON} supply has stabilized before turning the switch back on. After t_{OVP_Recov}, the TPD1S414 turns ON the nFET through a soft start to ensure that the USB Inrush current compliance is met. When the OVP condition is cleared and the nFET is completely turned ON, the $\overline{ACK}$ is reset LOW.

TIMING DIAGRAMS

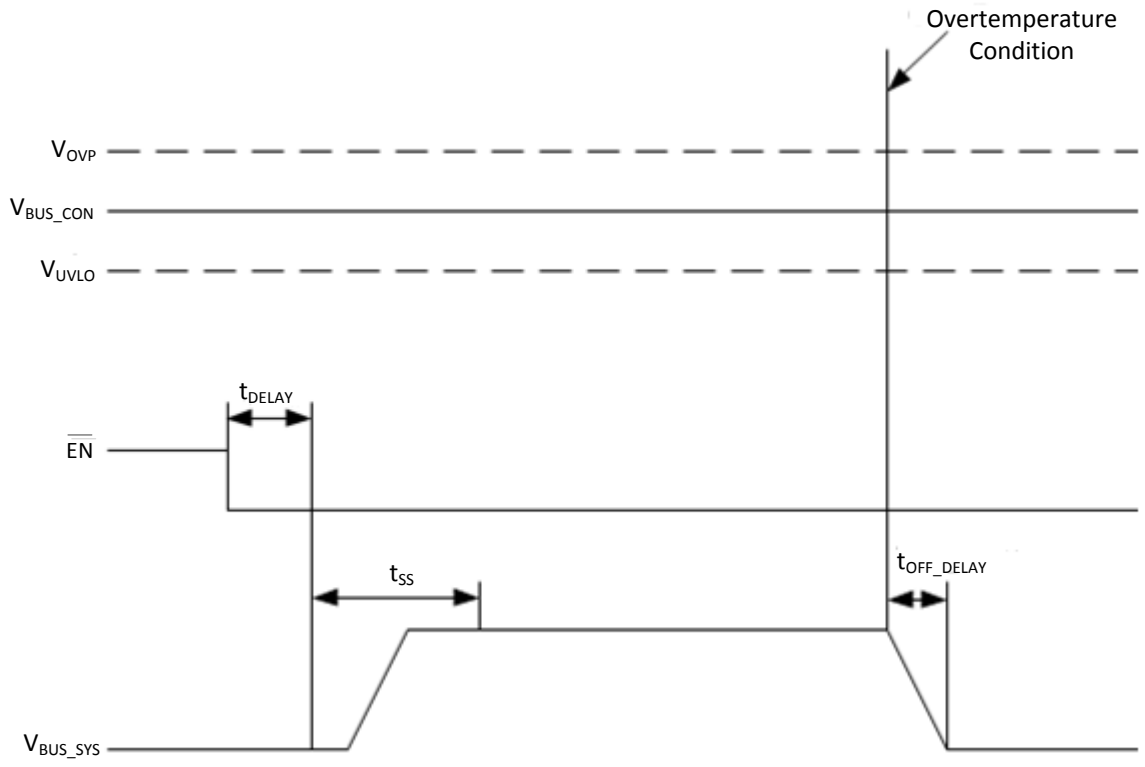


Figure 9. Thermal Shutdown Operation

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APPLICATION INFORMATION

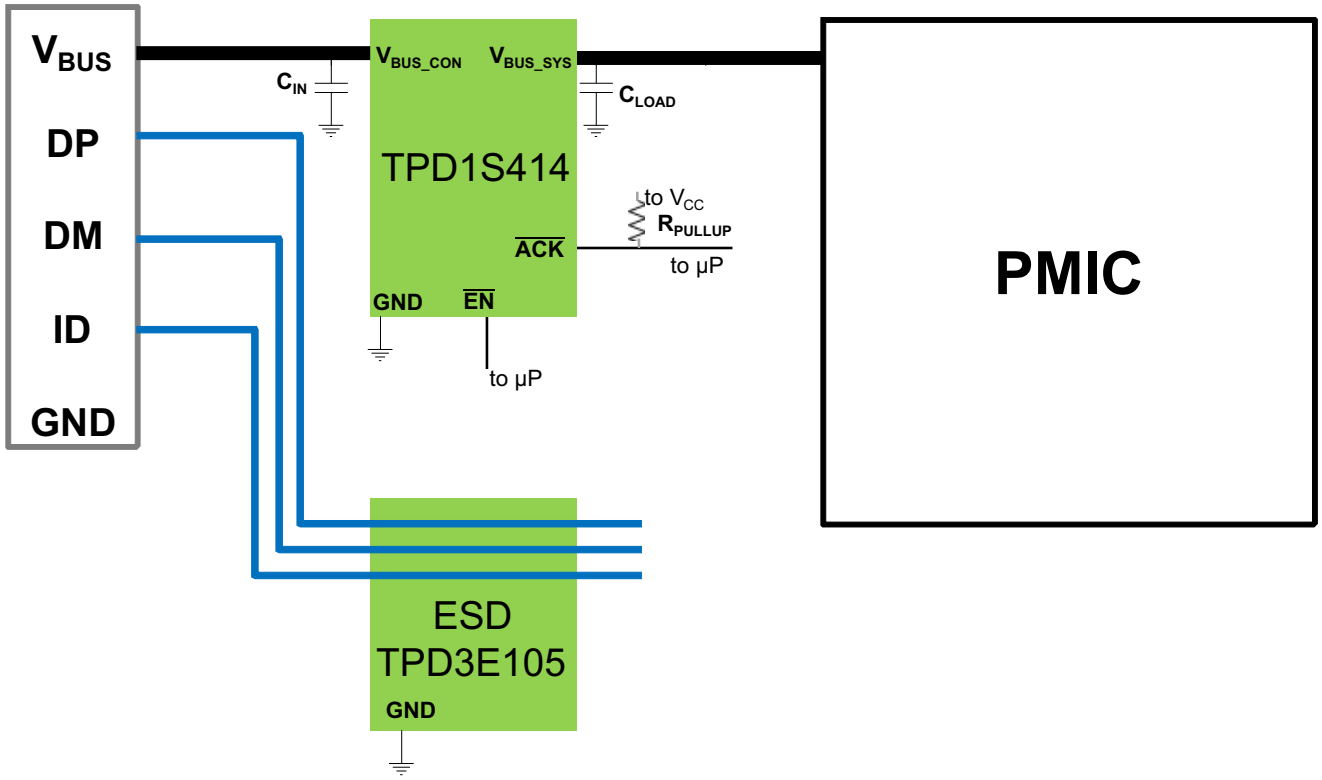


Figure 10. Typical Application Configuration for TPD1S414

The IEC 61000-4-5 standard specifies the lightning and industrial surge model. Power lines like the V_{BUS} line on the USB port is subject to switching and lightning transients. Power supply switching transients can enter the system due to capacitor bank switching on the rail, minor load switching on the system and various system faults like arcing to the grounding system of the installation. Direct lightning to the outer installations cause an over voltage condition on the V_{BUS} line. In the event of an over voltage condition, the OVP block of the Processor or the protection circuitry turns off isolating the system from these transients. Abruptly turning off the Load, causes a further ripple due to the inductive nature of the charging cable. End systems require protection against these transients. These transients have greater energy than the ESD events. Systems cannot be protected from these transients using simple ESD diodes. The TPD1S414 has a precision trigger and precision clamping circuit that ensures a DC tolerance of 30 V while suppressing surge voltage up to 100V under 35 V.

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BOARD LAYOUT

TPD1S414 can be routed in a single layer PCB. PCB traces to V_{BUS_SYS}, V_{BUS_CON}, and GND can be routed in the fashion shown in Figure 11.

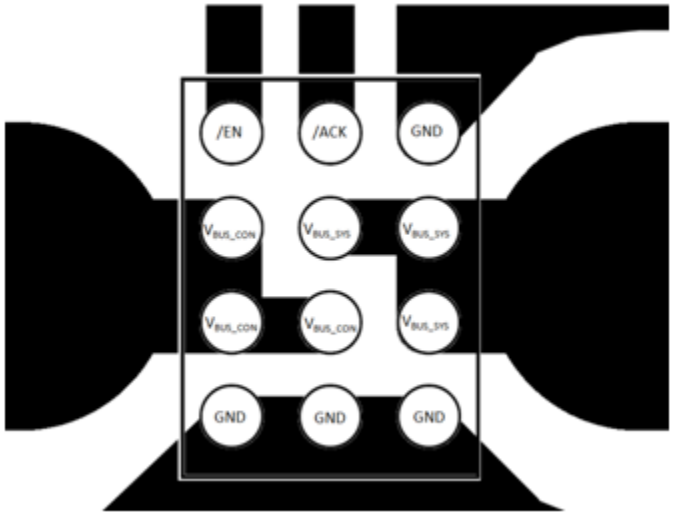


Figure 11. V_{BUS_SYS}, V_{BUS_CON}, and GND pins tied together

Tying V_{BUS_SYS}, V_{BUS_CON}, and GND pins respectively together provides lower resistance connectivity between the USB connector and the PMIC. For this example, the trace widths to V_{BUS_SYS}, V_{BUS_CON} are 25 mils (0.635 mm) under TPD1S414. There are no VIAs required within the SMD pads in this design. Stitching VIAs for GND can be placed near the component instead.

The decoupling capacitors per the recommended operating settings should be placed as close as possible to the TPD1S414. There should be a short path from the device ground pins to the system ground plane. This ensures best protection under ESD and surge transients.

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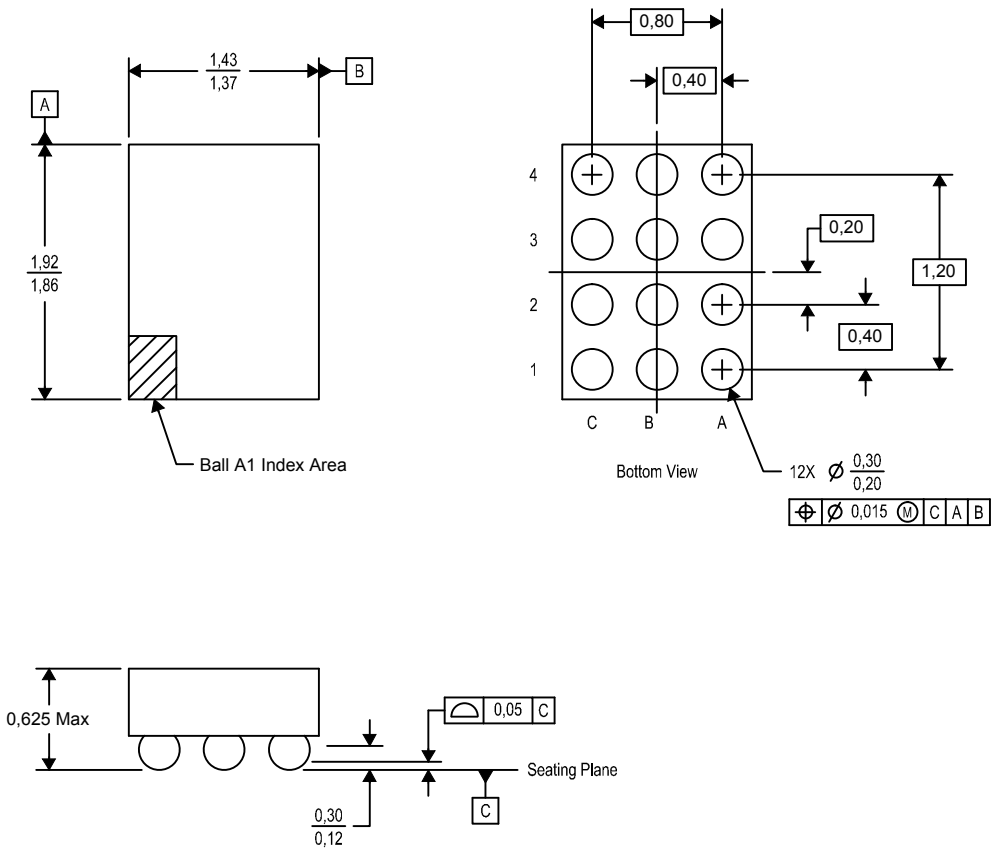
REVISION HISTORY

Changes from Original (October 2013) to Revision A **Page**

- Changed text in the DESCRIPTION From: TPD1S414 waits 15 ms before turning ON the nFET To: TPD1S414 waits 20 ms before turning ON the nFET 1
- Deleted Peak input current on V_{BUS_CON} pin, I_{BUS} from the ABSOLUTE MAXIMUM RATINGS table 3
- Deleted Continuous forward current through the FET body diode, I_{DIODE} from the ABSOLUTE MAXIMUM RATINGS table 3
- Added Voltage on $\overline{ACK}$ pin to the ABSOLUTE MAXIMUM RATINGS table 3
- Added values to the THERMAL INFORMATION table 3
- Added Continuous current on V_{BUS_CON} and V_{BUS_SYS} pins to the RECOMMENDED OPERATING CONDITIONS table 4
- Added Continuous forward current through the FET body diode, I_{DIODE} to the RECOMMENDED OPERATING CONDITIONS table 4
- Changed the I_{HOST_LEAK} MAX value From: 160 To: 200 µA in the SUPPLY CURRENT CONSUMPTION table 4
- Changed horizontal axis labeling on Figure 6 6
- Deleted graphs: Enabling the Load Switch, Connecting V_{BUS_CON}, and OVP Operation from the TIMING DIAGRAMS section 8
- Changed Figure 10 9
- Added text to the APPLICATION INFORMATION section 9

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TPD1S414 (R-XBGA-N12) DIE-SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree package configuration.

NanoFree is a trademark of Texas Instruments.

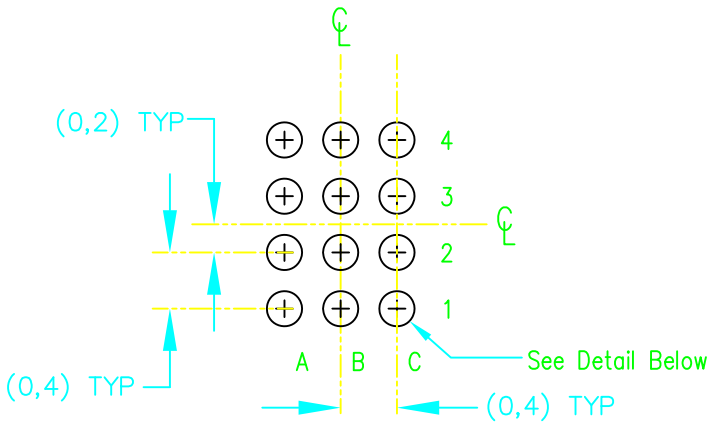
SCALE	SIZE		REV	SHEET

YZ (R-DSBGA-N12)

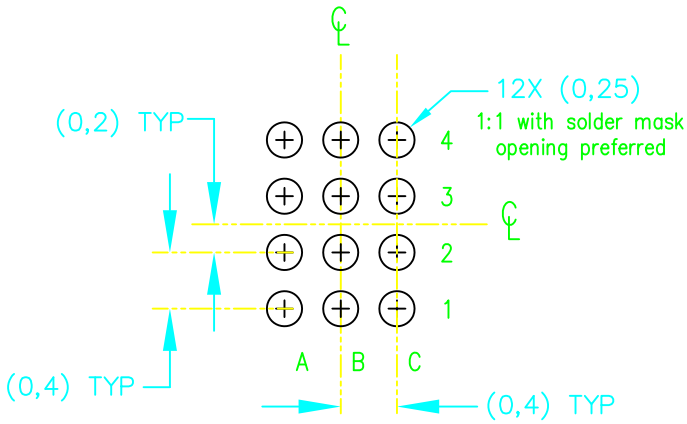
(Pb–Free Solder Spheres)

DIE-SIZE BALL GRID ARRAY

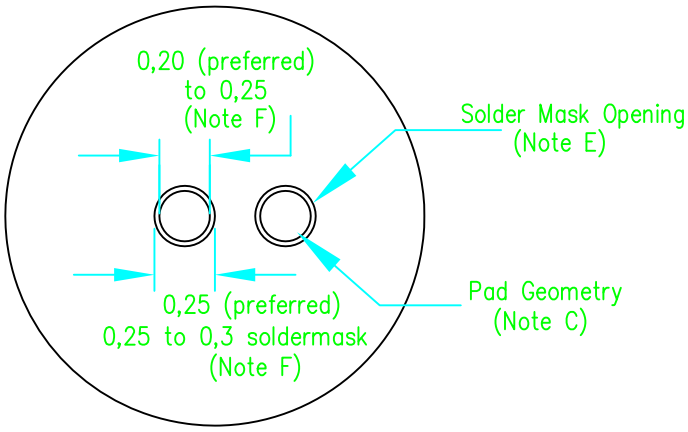
Example Board Layout
(Note C)

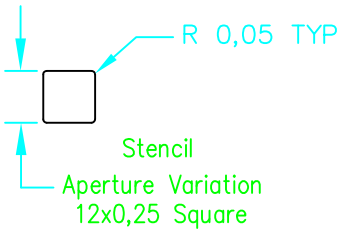


Example Stencil Design
0.100 Thick Stencil
(Note D, G)



Non Solder Mask Defined Pad
(Note F, G)





10/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Wafer Chip Scale Packages, Texas Instruments Literature No. SBVA017 and also the Product Data Sheet for specific thermal information, via requirements, and recommended routing guidelines. These documents are available at www.ti.com <http://www.ti.com>.
G. Placement force during assembly must be kept below 30g per solder sphere.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1S414YZR	ACTIVE	DSBGA	YZ	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH414	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

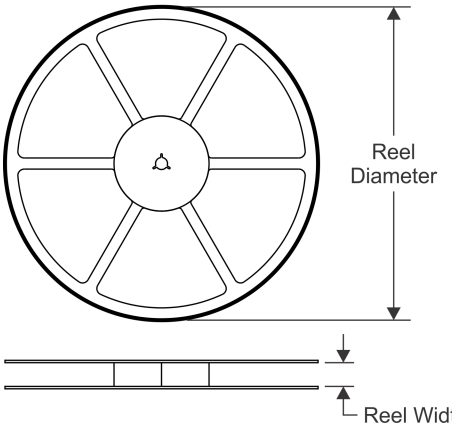
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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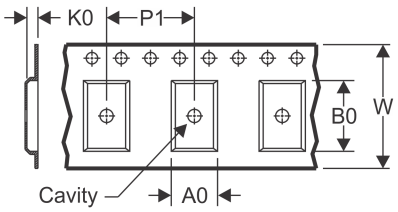
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

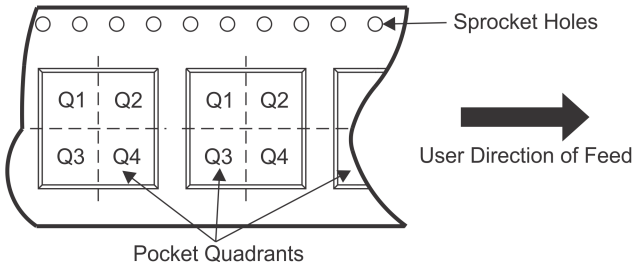


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

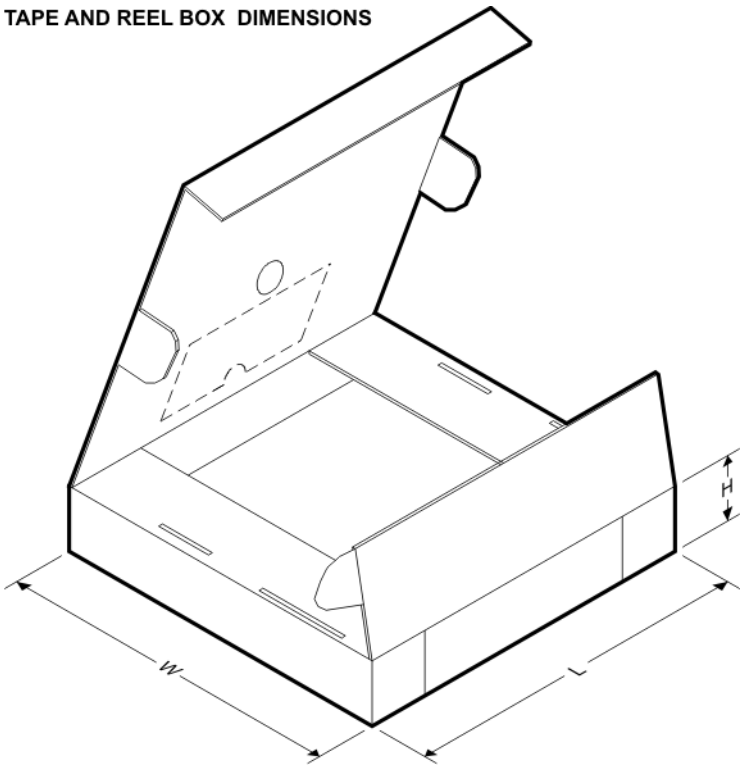
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1S414YZR	DSBGA	YZ	12	3000	178.0	9.2	1.49	1.99	0.75	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1S414YZR	DSBGA	YZ	12	3000	220.0	220.0	35.0

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